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A VT-INSENSITIVE CRYSTAL-LESS CMOS RELAXATION OSCILLATOR WITH MOS PROCESS COMPENSATION IN 0.18 μM TECHNOLOGY

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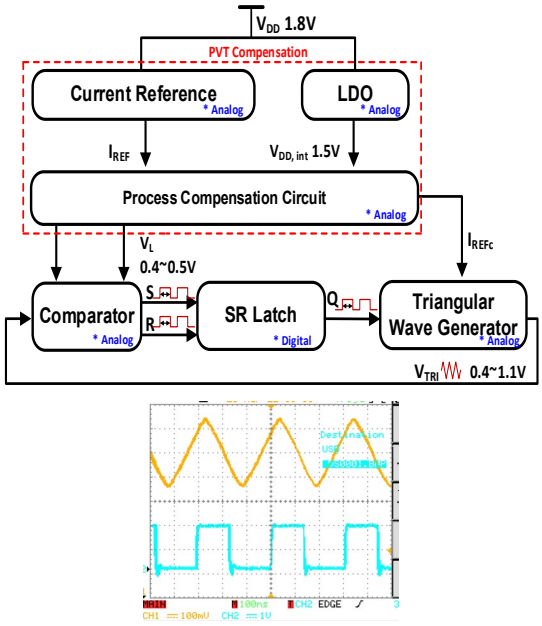
Graphical abstract



Abstract

An on-chip crystal-less relaxation oscillator is presented in this work. It exhibits a self-biased current reference to reduce the overall supply voltage sensitivity in which the input current is made to directly depend on the output current of the current source itself instead of having an input current connected directly to the supply voltage. The temperature compensation is achieved from bipolar bandgap topology in order to take advantage of summing the proportional-to-absolute-temperature (PTAT) current and the complementary-to-absolute-temperature (CTAT) current. Through carefully sized output transistors, a drain current IREF is generated to charge and discharge the oscillating capacitor. This design demonstrates a simple compensation technique that achieves a frequency variation of less than ±1% with a supply voltage of 1.8V input at normal temperature. A linear regulation performance achieves less than ±1% over supply voltage that ranges from 1.62V to 1.98V. A temperature coefficient less than 200ppm/°C is achieved over the temperature range of -10 to 120°C. The whole chip occupies 0.57mm2 (753.3 µm x 753.3 µm) and consumes 700 µW. This oscillator has been designed and analyzed with 0.18µm 1p6m TSMC CMOS process, intended to serve as a clock generator of power electronic systems to improve worst-case power efficiency.

Keywords: Current reference, crystal-less oscillator, MOS-process compensation, temperature coefficient, voltage-temperature insensitive.

1.0 INTRODUCTION

Clock signal generators are widely used in many applications such as in measurements, instruments and switching power converters. In switching power converters such as in the field of DC-DC converters, the clock signal is essential, because it synchronizes signals and timing relationship. The output frequency of the clock must be constant and tolerant to environmental variations. Crystal oscillators are exceptionally stable not only in phase noise and jitters but also have remarkable performance under the range of process, supply voltage and temperature (PVT) conditions. However, their incompatibility with on-chip integration increases their volume and leads to high cost. So, the challenge is in designing CMOS crystal-less clock generators that deliver stable frequency, while accommodating variations across PVTs. Several oscillators have been studied as clock sources in on-chip applications due to their compatibility with the standard CMOS process and ability to obtain stable clock signals. A low voltage current generator without any external component is used to reduce its power consumption [1] however, its oscillation frequency is low. On the other hand, the work in [2] [22] presents a ring oscillator that adjusts the delay time of each stage by controlling the compensation current through proper bias voltage. Moreover, reference [3][21] use an integrated error feedback (IEF) for comparators and two types of resistors with opposite first-order temperature coefficients (TCs) to increase the frequency to tens of megahertz and maintain frequency even with voltage and temperature variations while To keep the output frequency stable during temperature drifts, duty-cycled digital frequency-locked loops disable energy-hungry components and reactivate them

periodically [12]. For high temperature application, reference [4] improve the temperature sensitivity by putting in parallel the MIM capacitor with accumulation-mode varactor (nMOScap) and by adjusting the quantity of the contacts of the resistor layout. DOIng so, adjusts the negative TC to cancel the positive TC of the resistor core. Another temperature compensation technique is introduced in [16][17][18]. Moreover, in [5]it uses digital feedback loop to tune loop delay to adjust the output frequency. Except for [2], the other works mentioned above use RC relaxation oscillator, and they almost focus only on temperature compensation. Therefore, this work will be more comprehensive since the oscillator designed here is supply voltage and temperature (PVT) insensitive. This paper describes a crystal-less CMOS relaxation oscillator imbedded with self-biased bipolar bandgap topology is presented. Proper sizing and design optimization allows to produce an output current and voltage reference to the triangular wave generator that is nearly independent of temperature and supply voltage. Moreover, simple compensation technique is introduced to maintain low sensitivity to MOS process corner variation.

The proposed relaxation oscillator with compensation circuit is shown and discussed in Section 2.0. The performance together with simulation results is presented in Section 3.0. And finally, Section 4.0 provides the overall research efforts and draws concluding remarks.

2.0 METHODOLOGY

Figure 1 shows the block diagram of the proposed oscillator with process compensation circuit. The main building blocks include a current reference, an LDO, process compensation circuit, comparators, SR latch and triangular wave generator.

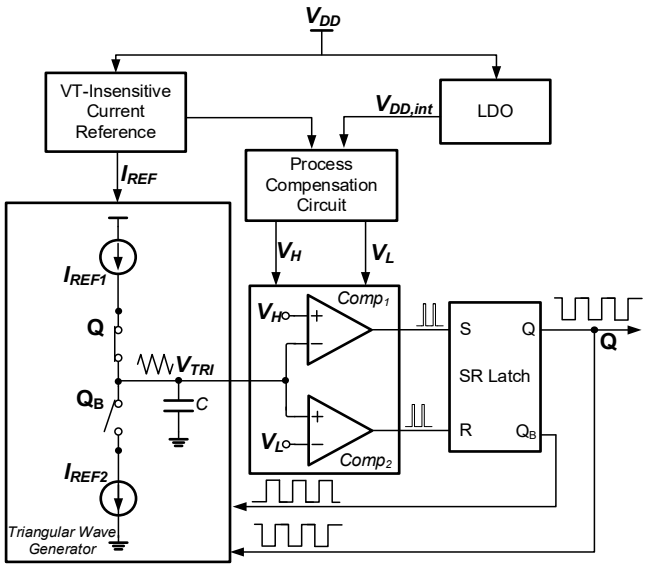


Figure 1 Block diagram of the proposed relaxation oscillator

A VT-insensitive current generator is realized by using a self-biased current source. The generated current is used to provide bias current I_{REF} to charge and discharge the internal timing capacitor of the triangular wave generator. An LDO is employed to help regulate supply voltage *VDD* variation. The variable voltages, V_H and V_L, are provided from the same current reference through a simple compensation circuit. The comparators, *Comp1* and *Comp2*, are used to compare the generated variable voltages with the voltage across the internal timing capacitor, V_{TRI}. Moreover, the internal timing capacitor is charged and discharged through a charge pump between the threshold voltages V_H and V_L by the two matched current sources I_{REF1} and I_{REF2}. The SR latch is used to store the respective states of the comparators, *Comp1* and *Comp2*, when the triangular waveform, V_{TRI}, crosses the threshold voltages, V_H and V_L. The output Q of the SR latch will then generate the output voltage with the desired output frequency. The proposed relaxation oscillator can generate two output signals, one with a triangular (sawtooth) wave, V_{TRI}, and the other one with a square wave, Q or QB, at the same oscillation frequency. Conventionally, signals Q and QB, directly controls the switching action of charge pump.

Ideally, the oscillation period is proportional to capacitor value, voltage difference and inversely proportional to capacitor current, I_{REF}. During charging and discharging of the capacitor, each oscillation period is expressed below:

$$T_{charge} = \frac{C(V_H - V_L)}{I_{REF}} \quad (1)$$

$$T_{discharge} = \frac{C(V_H - V_L)}{I_{REF}} \quad (2)$$

where *C* is the internal timing capacitor of the triangular wave generator. The comparators and the SR latch can cause delay time much less than parasitic capacitance, Cp does. Delay time, t_d can be written as:

$$t_d \approx \frac{C_p(V_H - V_L)}{I_{REF}} \quad (3)$$

However, in practice, comparators and SR latch switch delays, parasitic capacitance (C_p) and offset voltages are added to the output period and the total oscillation period for one cycle can be expressed as:

$$T_{OSC} = \frac{(C+C_p)(V_H - V_L)+V_{OFF1}}{I_{REF1}} + \frac{(C+C_p)(V_H - V_L)+V_{OFF2}}{I_{REF2}} + 2t_d \quad (4)$$

where I_{REF1} and I_{REF2} governs the periodic switching action, $(V_H\text{-}V_L)$ is the threshold voltage difference, V_{OFF1} and V_{OFF2} are comparator offset voltages, $(C+C_p)$ is the timing capacitor with parasitic capacitance and td is delay induced by the parasitic capacitance, comparators and SR latch. According to (1), V_{OFF1} and V_{OFF2} can be neglected if the comparator provides a high gain while the delay time td can be reduced by using a sufficiently large timing capacitor or small bias current to ignore its effect. Moreover, the delay caused by the comparator and the SR latch is much smaller than the oscillation period, which can also be ignored. Neglecting the parasitic capacitance, delay time and offset voltage, oscillation frequency only depends on I_{REF}, *C* and voltage difference of V_H and V_L. The frequency can be approximated to:

$$f_{OSC} = \frac{I_{REF}}{2C(V_H - V_L)} \quad (5)$$

Among the most critical aspects of the proposed oscillator design is the generation of the reference current, which must be less sensitive to process variation. Moreover, the level of supply voltage and temperature independence of f_{OSC} strongly depends upon the current and voltage references. Thus, the focus of this

design is on the robust reference generator circuit.

2.1 Current Reference

A current reference implemented with two BJTs with the same current but different emitter area can produce the positive voltage reference coefficient (ΔV_{BE}) and the negative voltage reference coefficient (V_{BE2})[13][19]. By adjusting the ratio of the resistors R_1 and R_2, the positive and the negative temperature coefficient (TC) complement each other to be balanced and achieved a current which is insensitive to temperature. A proportional-to-the-absolute temperature (PTAT) current and complementary-to-the-absolute temperature (CTAT) current are generated from the same current source. Figure 2(a) shows PTAT equivalent circuit analyzed from thermal voltage (V_T) based current reference. A voltage across resistor R1 is generated from the difference of the two-emitter base voltages of Q_1 and Q_2. The emitter areas of these transistors differ by a factor of N. If $(W/L)_{P1} = (W/L)_{P3}$ and $(W/L)_{P2} = (W/L)_{P4}$, then M_{P1}(M_{P2}) and M_{P3}(M_{P4}) ideally carry equal currents.

Hence, the current in (6) can be generally called *proportional-to-the-absolute temperature* (PTAT), where $V_T = kT/q$ is the thermal voltage ($k = 1.38 \times 10^{-23}$ J/K is Boltzman's constant, T is the absolute temperature and $q = 1.6 \times 10^{-19}$ C is the electron charge), V_{EB1} and V_{EB2} are emitter-base voltage of Q_1 and Q_2, respectively. While in Figure 2(b), an equivalent circuit of *complementary-to-the-absolute temperature* (CTAT) analyzed from an emitter-voltage based current reference that forces the current to flow resistor, R_2. This leads to a current in (7) as negative temperature- dependent or CTAT.

$$I_{PTAT} = \frac{V_{BE2}-V_{BE1}}{R_1} \approx \frac{\Delta V_{BE}}{R_1} \approx \frac{V_T \ln N}{R_1} \quad (6)$$

$$I_{CTAT} = \frac{V_{BE2}}{R_2} \quad (7)$$

The generated I_{PTAT} and I_{CTAT} currents are subsequently mirrored through M_{P5}-M_{P6} and M_{P8}, respectively and added together to produce an output current I_{REF} as expressed as:

$$I_{REF} = I_{PTAT} + I_{CTAT} = \left(\alpha \frac{V_T \ln N}{R_1} + \beta \frac{V_{BE2}}{R_2}\right) \quad (8)$$

where α is the multiple of M_{P5}-M_{P6} and β is the multiple of M_{P8}. For supply voltage variation, there is no term of the VDD, so the derivative of reference current with respect to VDD is zero. Thus, the reference current is insensitive to supply voltage. However, in (5), the factor of the voltage difference (V_H-V_L), will increase when the temperature rises due to. This makes the frequency to be directly proportional to temperature. Therefore, the current with positive TC is used to maintain the output frequency by changing the multiple of mirror current of the transistors M_{P5}-M_{P6} and M_{P8}.

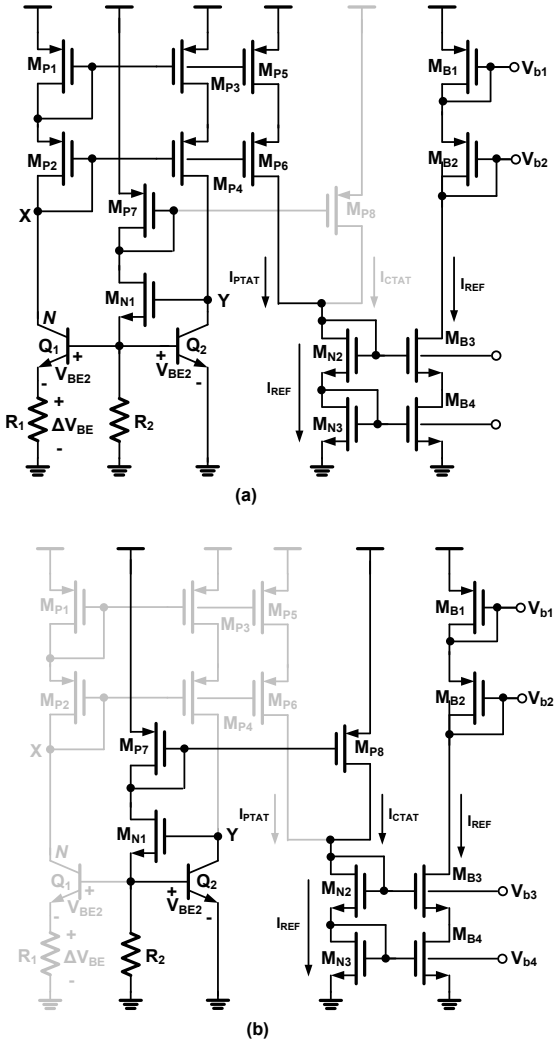


Figure 2 Current reference (a) PTAT (b) CTAT generation

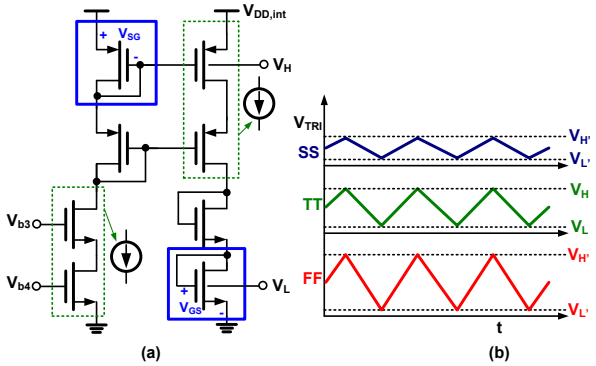


Figure 3 (a) process compensation circuit and (b) simplified process compensated frequency

2.2 Process Compensation Circuit

In previous works, the amplitude of the triangular wave (V_H-V_L) is constant when process, supply voltage and temperature vary, but the factor I_{REF} in (5) will change when process corners varies and the output frequency also vary significantly. In order to avoid this case, designing a variable (V_H-V_L) can balance the influence of I_{REF} as it varies in different corners and produce constant frequency. In

other words, the concept of this process compensation method is to produce larger (V_H-V_L) to match larger current at FF corner and to produce smaller (V_H-V_L) to match smaller current at SS corner.

Figure 3(a) shows the process compensation circuit that uses diode connected MOS to generate variable V_H and V_L. V_H and V_L can be expressed in (9) and (10), respectively, where V_{GS} for NMOS and V_{SG} for PMOS can both have the expression in (11).

$$V_H = V_{DD,int} - V_{SG} \tag{9}$$

$$V_L = V_{GS} \tag{10}$$

$$|V_{GS}| = \sqrt{\frac{2I_D L}{\mu C_{ox} W}} + |V_{TH}| \tag{11}$$

When MOS process corner varies, the parameters such as I_D, μ, Cox and V_{TH} will also vary significantly. At FF, V_{TH} largely decreased while I_D, μ and Cox increased. In order to make $|V_{GS}|$ reduced at FF, smaller I_D is used so that the effect on $|V_{GS}|$ can be ignored. Similarly, at SS, V_{TH} largely increased while I_D, μ and C_{ox} decreased. So, in order to make $|V_{GS}|$ increased at FF, larger I_D is used so that the effect on $|V_{GS}|$ can be neglected.

Voltage difference (V_H-V_L), can be obtained by substituting (11) to (9) and (10). When I_{REF} increases at FF corner and with smaller VGS and VSG, the voltage difference (V_H-V_L) also increases. On the other hand, when IREF decreases at SS corner and with larger VGS and VSG, the voltage difference (V_H-V_L) also decreases. The increase or decrease of both IREF and (V_H-V_L) during FF and SS, respectively, balance its effect during process corner variation and leads to maintain a constant oscillation frequency. Figure 3(b) shows the simplified response of the compensated oscillation frequency.

2.3 Low-Dropout Regulator (LDO)

The standard supply voltage V_{DD} has error between ±10%. This error largely influenced V_H to change during process corner variation. Hence, overall oscillation frequency will become unstable. To alleviate the problem, the traditional Low-Dropout Regulator (LDO) is implemented in Figure 4[6][20]. The error amplifier locks V_{FB} and V_{REF} which is the output of the bandgap voltage reference. The power MOS produces the internal supply voltage $V_{DD,int}$ of 1.5V by adjusting the ratio of R_A and R_B. A PVT insensitive $V_{DD,int}$ can be expressed as:

$$V_{DD,int} = \frac{(R_A+R_B)}{R_A} V_{FB} = \left(1 + \frac{R_B}{R_A}\right) V_{FB} \tag{12}$$

where V_{FB} almost equals to V_{REF} if the gain of the error amplifier is large enough.

2.4 Comparator and SR Latch

In Figure 5, the output of the comparators is fed to the SR latch to produce clock Q. The two comparators, *Comp1* and *Comp2*, are used to compare the voltage across the capacitor, V_{TRI}, with threshold voltages. When V_{TRI} becomes higher than V_H, the output S of the upper comparator, turns to high and then sets Q=1; when V_{TRI} becomes lower than V_L, the output R of the down comparator, turns to low and then resets Q=0. When V_{TRI} is between V_H and V_L, S and R are both zero, therefore, Q stays the

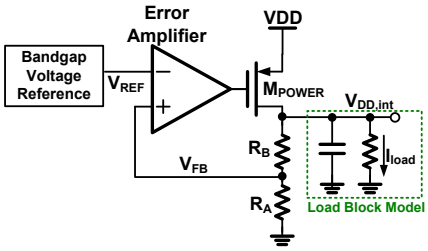


Figure 4 Traditional LDO

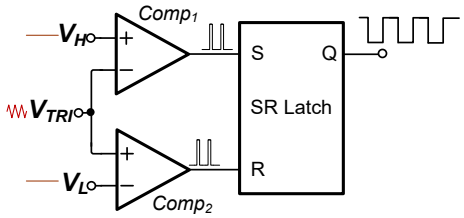


Figure 5 Comparators and SR Latch

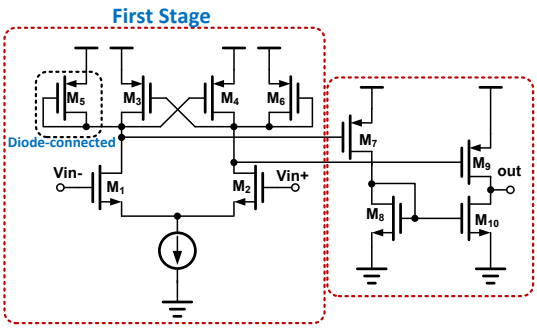


Figure 6 N-type input comparator

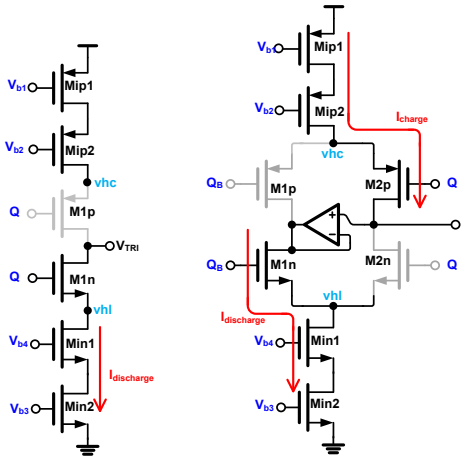


Figure 7 (a) Traditional (b) improved charge pump

same. Since the input common mode range (ICMR) of V_{TRI} that varies between 0.4 to 1.1V, the upper comparator, *Comp1*, is implemented by N-type input as shown in Figure 6[7]. Considering high gain and enough bandwidth of the comparator is necessary, a two-stage OP and diode-connected MOS in the first stage is used to allow fast switching action at high input voltage. For lower comparator, *Comp2*, a P-type input is implemented to

accommodate low input voltage.

2.5 Triangular Wave Generator

The triangular wave generator can be seen as a charge pump. For traditional charge pump in Figure 7(a), M1p and M1n are switches controlled by clock Q, while the other transistors mirror the current from the current reference. However, there is a problem called charge sharing. It is when the node vhc would accumulate charges to reach 1.5V when Q=1 during discharge time. The moment, when Q=0, during charge time, the node vlc would release charges to ground. During charging and discharging action, VDS is not enough for Mip1-Mip2 and Min1-Min2 respectively, which makes the said MOS to operate in linear region and have smaller current when switch just turns on. It takes a short time to make MOS in saturation. If the oscillation frequency increases, the effect of this short time becomes more serious, thus, V_{TRI} will be distorted.

In order to resolve this problem, the improved charge pump is carried out in Figure 7(b) [8]. With additional two pairs of switches, M2p and M2n, controlled by QB; and an additional unity-gain amplifier that provides an always turn on path for charging and discharging.

Based on (5), the factors that reacts with process, supply voltage and temperature variations are taken into account separately. It is evident that the current I_{REF} in (8) is process dependent caused by large variation induced by resistors. If matching errors are neglected, I_{REF} is the same current that flows in the drain of the diode-connected MOS is transformed to generate V_H and V_L. When I_{REF} varies, variable (V_H-V_L) by diode-connected MOS is generated to balance the oscillation frequency. Table 1 shows how the parameters change in different corners. The larger the current IREF, matches larger (V_H-TV_L) at FF corner; while the nominal current I_{REF}, matches middle (V_H-V_L) at TT corner. Lastly, the smaller current IREF, matches smaller (V_H-V_L) at TT corner. Therefore, the sensitivity of the oscillation frequency to process variation is due to μ, C_{ox}, V_{TH} and to the accuracy of the internal timing capacitor, which has a deviation smaller than that of a resistor.

For supply voltage variation, I_{REF} remains constant due to circuit structure. For the capacitor, an accumulation-mode varactor (nMOScap) is used. Since nMOScap is voltage dependent which is the same with (V_H-V_L), an LDO is added to make (V_H-V_L) and C both constant when supply voltage change. Thus, all frequency factors don't change with the supply voltage, so the oscillation frequency would remain stable.

For temperature variation, the variable (V_H-V_L) produced by diode-connected MOS has positive TC while C has almost same capacitance value. By adjusting the TC of I_{REF} by changing the multiples α and β in (8) to be positive TC, temperature variation of (V_H-V_L) is compensated. I_{REF} with proper TC is still insensitive to supply voltage and still compensates the process variation normally, which means it can be insensitive to PVT at the same time.

3.0 RESULTS AND DISCUSSION

The proposed oscillator is designed and implemented in a 0.18µm CMOS process technology and its chip microphotograph is shown in Figure 8. The overall chip area is 753.3 µm x 753.3 µm and with power consumption of 700 µW. The designed oscillator can output both triangular wave and square wave signals with the same output frequency as depicted in Figure 9. Figure 10 shows the output oscillation frequency under supply voltage variation of ±10%. Three chips were measured with variation of the oscillation frequency error is below 1.5%. Figure 11 shows the output frequency of the oscillator at 1.8V supply voltage as temperature varies with the range of -20˚C to 120˚C. TCs can be obtained with (13). The best-case TC is 168.8 ppm/˚C which is in TT corner and VDD=1.8V while the worst- case TC is 168.8 ppm/˚C which is in SS corner and VDD=1.62V.

$$TC_{f_{TRI}} = \frac{1}{f_{TRI}} \frac{\partial f_{TRI}}{\partial T} \quad (13)$$

Table 1 Relative parameter values in different corners

Corners	Parameters					
	µ	C_{ox}	$\|V_{TH}\|$	$\|V_{GS}\|$	V_H-V_L	I_{REF}
FF	Max	Max	Min	Min	Max	Max
TT	Mid	Mid	Mid	Mid	Mid	Mid
SS	Min	Min	Max	Max	Min	Min

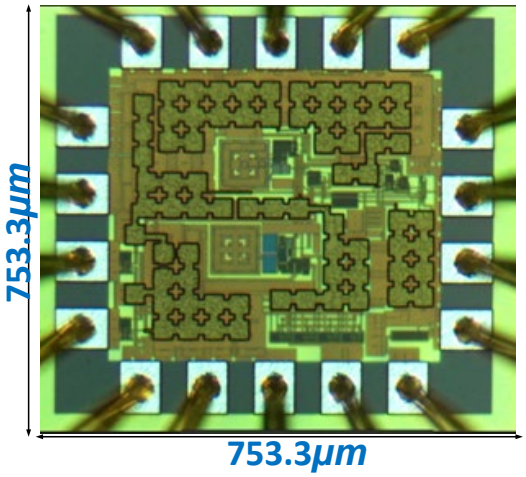


Figure 8 Chip microphotograph

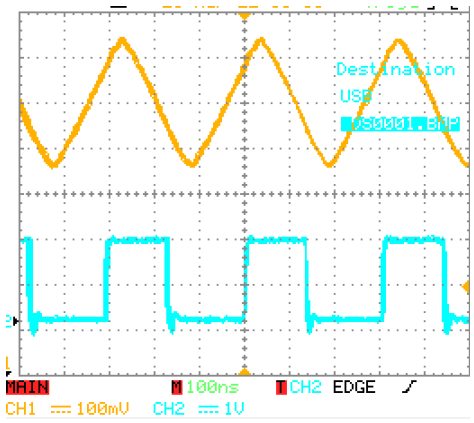


Figure 9 Output frequency: triangular wave and square wave signal

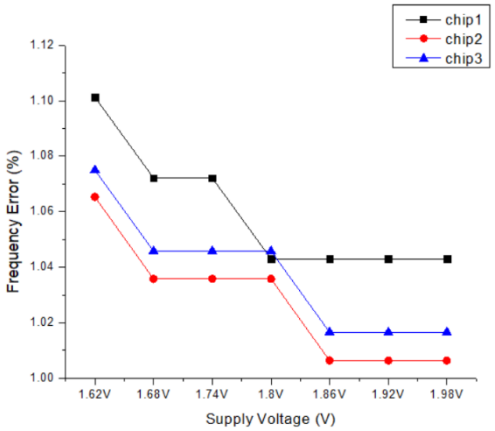


Figure 10 Frequency error across supply voltage

Table 2 Comparison table with previous works

Reference	[1] ISCAS	[2] JSSC	[3] TCASII	[4] TCASI	[5] TCASI	[9] JSSC	[11] ICTA	This Work
Year	2007	2006	2017	2013	2013	2016	2022	2023
Technology (nm)	350	250	90	130	180	65	180	180
Supply Voltage (V)	1	2.4	0.8	2.5	0.9	1.0	0.8	1.8
Frequency (Hz)	80K	7M	51.3M	1M	12.77M	18.5k	121k	3.05M
Temp. Range (°C)	0~80	-40~125	-20~100	25~200	-30~120	-40~90	-20~100	-20~120
Temp. Coeff. (%)	±3.368	0.78	0.13	1.89	0.46	±0.18	0.43	2.03
Temp. Coeff. (ppm/°C)	842	94.5	21.8	108	31	27	36.2	168.8
Voltage Range (V)	1.0~1.5	2.4-2.75	0.8~1.2	2~3	0.6~1.1	0.95~1.05	0.75~0.85	1.62~1.98
Frequency Variation with VDD (%)	-2.5	0.29	±1.32	±1.09	±0.5	<5	12.8	1.12
Process Sensitivity (%)	5.92	±2.64	Not Shown	Not Shown	Not Shown	±7	Not Shown	1.98
Power (µW)	1.14	1,500	18	428	56.2	0.130	0.120	700
Area (mm²)	0.24	1.6	0.027	0.007	0.012	0.032	Not Shown	0.57

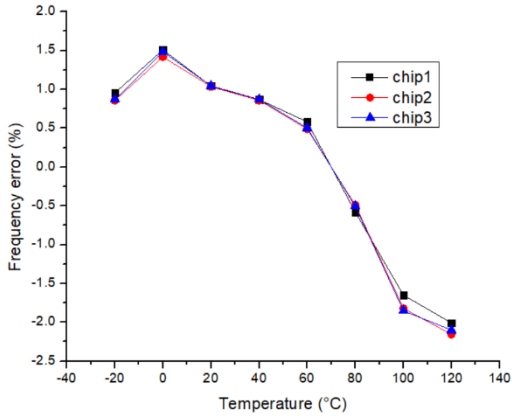


Figure 11 Frequency across temperature range

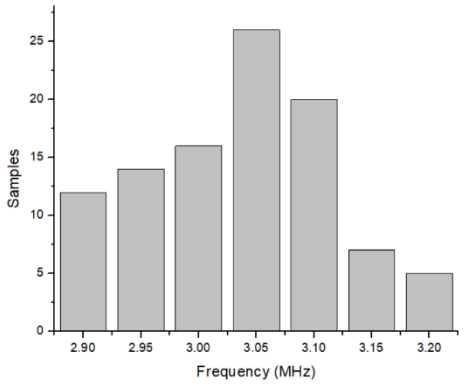


Figure 12 Histogram of the oscillation frequency for 100 runs of Monte Carlo

Figure 12 shows the histogram of Monte Carlo simulations in order to evaluate the sensitivity of the oscillation frequency to process variations. A mean oscillation frequency of 3.04 MHz and a standard deviation of 63.54 kHz is determined by the simulation, leading to a σ of about 2.09%, which is good enough for many applications, such as the clock generator for passive microwave transponders, where a 10% accuracy is typically acceptable [11].

Table 2 shows that the circuit's sensitivity to process variation is acceptable for several applications. The proposed oscillator achieves PVT insensitivity, which the other research papers seldom do. Reference [2] is also PVT but dissipates more power. Architectures [9]-[10] have very low power dissipation low because they operate in subthreshold region which made their performance more sensitive to process and supply voltage. This work consumes 700 µW largely due to the operation of the amplifier in the voltage regulator and comparators that requires large current so as to maintain the overall circuit to operate in saturation region. Thus, it upholds its performance to help reduce its sensitivity to process corner variations.

4.0 CONCLUSIONS

In this paper, a VT- insensitive crystal-less relaxation oscillator implemented in 0.18µm standard CMOS process is presented. This design does not require any external components or trimmings and can therefore be fully integrated. In this work, process compensation was successfully implemented using simple circuit of diode-connected MOS to generate variable voltage difference (V_H-V_L). The constant VDD which was produced by an LDO can prevent the output frequency from varying when supply voltage varies ±10%. I_{REF} with proper TC, output frequency remains constant under temperature variation. This design is intended to serve as clock generator of power electronic systems to improve worst case power efficiency.

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Conflicts of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper

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