ASEAN Engineering Journal

Full Paper

DUAL-BAND RECTIFIER WITH WIDE DYNAMIC RANGE FOR RF ENERGY HARVESTING UTILIZING 2.4 GHZ AND 5 GHZ WI-FI FREQUENCY BAND

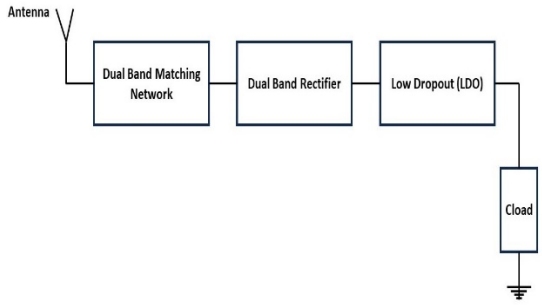
Kevin O. Maglinte*, Irish P. Maurin, Zyrick Mae G. Montalbo, Kent Neil Cris R. Pilar.

Department of Electronics Engineering, College of Engineering, Mindanao State University – Iligan Institute of Technology, Iligan City, Philippines

Article history
Received
17 January 2024
Received in revised form
27 July 2024
Accepted
8 August 2024
Published online
31 May 2025

*Corresponding author
kevin.maglinte@g.msuiit.edu.ph

Graphical abstract



Abstract

This study presents a dual-band rectifier that operates at 2.4 GHz and 5 GHz frequency bands with high peak PCE and wide dynamic range performance. The proposed design utilized a cross-coupled rectifier architecture with bulk-biasing. An L-matching network was inserted between the source port and the rectifier for maximum power transfer. A peak PCE of 74.93 % at -11 dBm input power was achieved at 2.4 GHz operating frequency. On the other hand, a peak PCE of 72.75 % at -11 dBm input power was achieved at 5 GHz operating frequency with a fixed 30 KΩ load. The design was optimized and offered a broad dynamic range of 12.74 dB and 10.28 dB for the 2.4 GHz and 5 GHz mode, respectively. The Vout measured for the 2.4 GHz was 1.05 V with -9 dBm input power, while for the 5 GHz, the Vout measured was 1.04 V at -4 dBm input power. The system was able to achieve 1 V at a sensitivity of -12.35 dBm and -11.52 dBm, for 2.4 GHz and 5 GHz respectively. Overall system integration at -1 dBm input power, the voltage output of the rectifier measured 1.47 V. On the other hand, the LDO measured a constant 1.2 V voltage output. The design was implemented in 65 nm CMOS process Technology.

Keywords: dual-band rectifier, RF energy harvesting, PCE, dynamic range, impedance matching network, LDO, CMOS

1.0 INTRODUCTION

The concept of harvesting energy from ambient sources has gained significant attention in recent years as a sustainable solution for powering low-power electronic devices. Researchers have explored various energy sources; and among these sources, Wi-Fi signals have emerged as a promising and widely available energy source. One must take into account the most important block of RF energy harvesting system, the rectifier. The RF-to-DC rectifier of a RF energy harvesting (RFEH) system is responsible for converting RF energy to DC voltage. Various challenges have been associated with rectifiers, such as nonlinearity, switching loss, conduction loss, minimum diode threshold voltage, and poor antenna gain in on-chip antennas (OCA) [1]. Overcoming these challenges requires careful selection of a compatible rectifier architecture and configuration based on the desired design specifications. Developing an efficient RF-to-DC converter architecture is particularly challenging due to the low power levels typically available in remote locations [2] The radiated power can vary unexpectedly based on factors like distance from the power source, transmission medium, and antenna orientation.

Furthermore, it is important to acknowledge that the ambient RF energy available in a single band is generally insufficient to power IoT devices having output voltage of 0.4 V at -10 dBm [3][4]. As a result, several studies have focused on RF rectifiers operating in multiple bands to increase the harvested power but multiband harvesting face limitations due to preference on simplicity [5] prompting for further studies. The objective of this study is to design a suitable rectifying system for energy harvesting in urban environments, specifically capturing the signals at both 2.4 GHz and 5 GHz frequencies of Wi-Fi. The aim is to achieve a high dynamic range and operate without the need for additional converter stages [6].

To ensure compatibility with various applications, it is crucial for these circuits to maintain the output voltage within a suitable range. Improving the power conversion efficiency which is the ratio of rectified power and RF input power, leads to a more efficient system. Certain architectures [7][8] were able to enhance the power conversion efficiency of the rectifying block but leakage currents on high input power were observed degrading the dynamic range. A need for studies on architecture that enhances the range of input power of energy harvesters is therefore observed.

In this study, improvement on the dynamic range of the rectifying block is focused. One of the challenges in RFEH is the varying power density of the RF environment. Maintaining a wide DR improves the reliability of an RFEH system in a highly dynamic RF environment. The low PCE at lower input power range is another challenge faced by previous rectifiers. Improving the PCE at low input power improves the dynamic range as it would allow the RFEH system to operate at a larger range of input power.

2.0 PROPOSED DESIGN

This work focuses on the design of a dual-band rectifier and utilizes the conventional the blocks of an RFEH as depicted in Figure 1. The blocks that are employed in this work are a matching network and the RF-to-DC rectifier. It is important to note that the DC voltage produced by the rectifier may exhibit variations or ripple due to fluctuations in the input power caused by the varying power density of the RF environment. A low-dropout voltage (LDO) regulator is integrated to address issue on fluctuations.

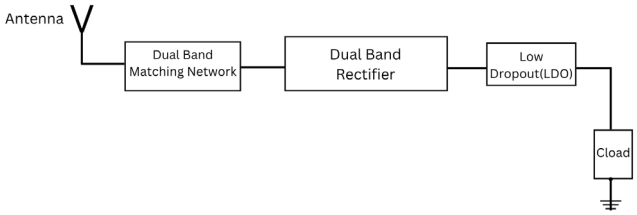


Figure 1 Block diagram of the dual-band RFEH

2.1 Impedance Matching Network

To implement a dual-band rectifier, a corresponding dual-band matching network is needed. The dual-band matching network topology that was utilized was an LCLC matching network based on [6]. The initial values for the components were calculated using equations 1-5 [10]. They were then fine-tuned to suit the two frequency bands. An off-chip balun was implemented to facilitate transfer from the single-ended block to the differential input rectifier. L1 and C1 are designed for low-band 2.4 GHz input impedance matching, and L2 and C2 are designed for high-band 5 GHz input impedance matching.

$$Q_S = Q_P = \sqrt{\frac{R_P}{R_S} - 1} \quad (1)$$

$$Q_S = \frac{X_S}{R_S} \quad (2)$$

$$Q_P = \frac{R_P}{X_P} \quad (3)$$

$$X_C = \frac{1}{2\pi FC} \quad (4)$$

$$X_L = 2\pi FL \quad (5)$$

Figure 2 shows the LCLC matching network in the testbench circuit.

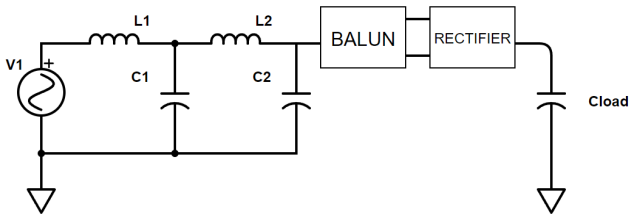


Figure 2 Testbench circuit for the dual-band matching network

2.2 RF-DC Rectifier

The RF-DC rectifier of the RF energy harvesting system is responsible for converting the RF energy to a usable DC voltage. Several parameters are used to determine the performance of the rectifier [9]. The power conversion efficiency (PCE) measures the ability of the rectifier to convert RF power to DC power and it is highly dependent on the architecture of the rectifying block. It is the ratio of the output DC power to the input RF power. PCE is given by the equation:

$$\text{PCE} = \frac{P_{out}}{P_{in}}\ x\ 100\% \quad (6)$$

Another parameter being considered in a rectifier is the dynamic range (DR) which defines the range of input power that the rectifier can maintain a high PCE. DR can be expressed as:

$$\text{DR (dB)} = P_{max}\,(dBm)\ - P_{max}\,(dBm) \quad (7)$$

where; Pmax and Pmin respectively denotes the maximum and minimum input power having a PCE > 80% of peak PCE.

In implementing the dual-band rectifier, the single-band operation of the rectifier for each of the frequency bands was first configured. A cross-coupled differential drive (CCDD) rectifier was adopted in this study as it consistently offers high PCE for low input power [11]-[13]. Several modifications of the CCDD architectures were tested to determine which would be most suitable for this study. Additionally, coupling capacitors were added in the input to improve the PCE of the rectifying block [14]. Iterative simulations were also done to determine the optimum sizes of the transistors as well as the number of stages to yield the desired PCE and DR. From the simulations, a two-stage rectifier was pursued in this study to attain the specified sensitivity.

In this study, a two-stage cross-coupled architecture for the RF-DC differential rectifier was adopted as it achieves a high PCE for the preliminary simulation for a single-band rectifier. The schematic design of the proposed rectifier architecture is shown in Figure 3.

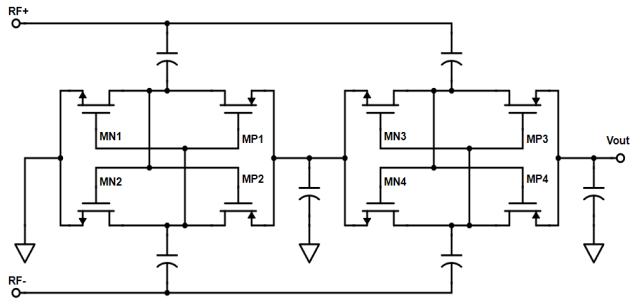


Figure 3 Schematic of the two-stage cross-coupled rectifier

2.3 Low-Dropout Regulator (LDO)

A Low-Dropout Regulator (LDO) is added to the whole system of the study. LDOs are commonly used to provide a stable and regulated output voltage despite fluctuations or variations in the input voltage [15]. The conventional LDO architecture, as depicted in Figure 4, employs an error amplifier, feedback loop, and pass transistor. The error amplifier compares the output voltage with a reference voltage, generating an error signal. This signal is fed back through a resistive network to the control mechanism of the LDO.

The pass transistor, based on the error signal, regulates the current flow from the input to the output of the LDO. This feedback control mechanism forms a closed-loop system that continuously compares the output voltage with the reference voltage and makes precise adjustments to counteract variations caused by changes in the input power from the rectifier [16]. Through this process, the LDO maintains a stable output voltage, compensating for load variations and ensuring that connected devices receive a consistent and reliable power supply.

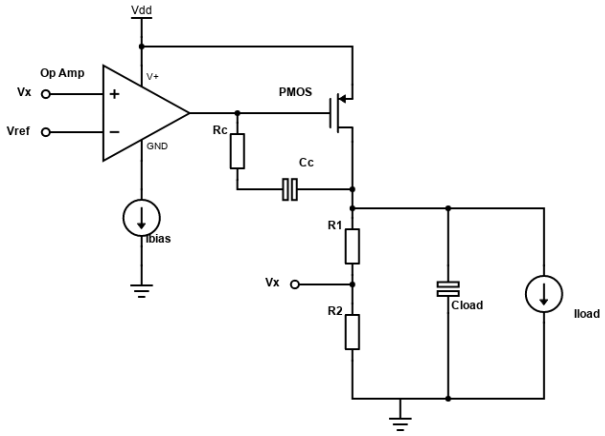


Figure 4 Schematic of LDO

3.0 SIMULATION RESULTS

The proposed design of the RFEH system was implemented and tested using Cadence Virtuoso in 65 nm CMOS technology. Parameters of the rectifier such as PCE, sensitivity, and dynamic range were determined from the simulations. The dynamic range is the range in which the performance of the rectifier is greater than 80 % of the maximum measured PCE. The line regulation and load regulation of the LDO were also simulated.

3.1 Single-band Operation

The rectifier was first tested with a single band matching network to determine the value for the active components to be used for the dual band matching network.

Figure 5 shows the results of the single-band operation of the PCE of the designed rectifier in a 2.4 GHz single band operation simulated at varying loads of 30 KΩ, 50 KΩ, 70 KΩ and 100 KΩ. The 2-stage rectifier with 30 KΩ load at 2.4 GHz band offers a peak PCE of 74.51% at -6 dBm input power. In contrast with the rest of the loading conditions of 50 KΩ, 70 KΩ and 100 KΩ, the peak PCE was measured at 76.01 % at -10 dBm, 76.79% at -13 dBm and 77.52% at -17 dBm respectively. The dynamic range for the different loading conditions were recorded as 14.29 dB, 13.58 dB, 12.91 dB, and 12.7 dB respectively.

On the other hand, Figure 6 shows the PCE of the designed rectifier in a 5 GHz single band operation was also simulated at varying load conditions. The 2-stage rectifier with 30 KΩ load at 5 GHz band offers a peak PCE of 73.13% at -10 dBm input power while the rest of the loading conditions of 50 KΩ, 70 KΩ and 100 KΩ, the peak PCE was measured at 75.28% at -14 dBm, 76.53% at -17 dBm and 77.41% at -19 dBm respectively. The dynamic range for the different loading conditions were recorded as 12.29 dB, 10.94 dB, 10.41 dB, and 10 dB respectively.

As observed from the results, as the load increased from 30 KΩ to 100 KΩ, the peak PCE also increased. However, the dynamic range decreased as the peak PCE and load increased.

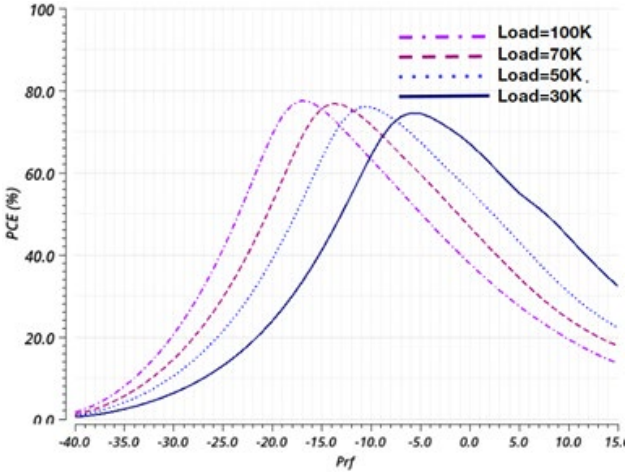


Figure 5 Effect of varying load resistance on PCE at 2.4 GHz

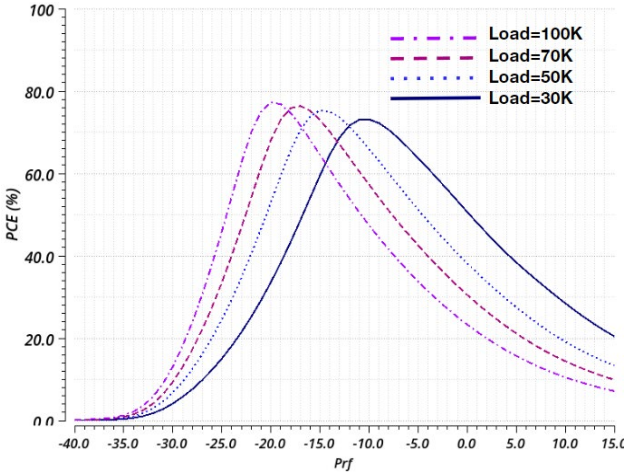


Figure 6 Effect of varying load resistance on PCE at 5 GHz

From this observation, a constant load resistance of 30K which presents the widest dynamic range was used during iterative simulations. Iterative simulations have been carried out to generate a parametric analysis to determine the optimum aspect ratio of the MOS. The peak PCE and dynamic range is directly related with each other as it both increases at the same time both depending on the channel length.

3.2 Dual-Band Operation

This section presents the performance of the dual-band operation of the designed rectifier evaluated in terms of its DR, PCE, sensitivity, voltage output, and reflection coefficient.

A peak PCE of the designed rectifier in a dual-band operating at 2.4 GHz achieved a peak PCE of 75.21% at -11 dBm while the dual-band operating at 5 GHz achieved a peak PCE of 72.9% at -11 dBm. 80% of the peak PCE for both operating frequencies is measured at around PCE > 60 %. Figure 7 shows that the design consistently offers a broad dynamic range of 12.44 dB and 10.74 dB for the 2.4 GHz and 5 GHz mode, respectively.

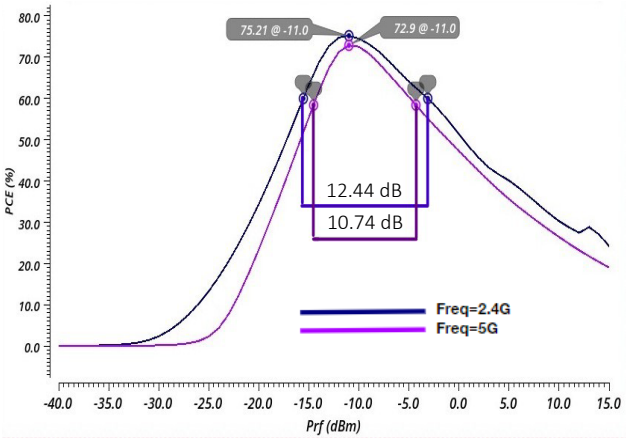


Figure 7 Dynamic range of dual-band rectifier with 30K load resistance

As observed for the dual-band operation, the dual-band rectifier showed a great result with high peak PCE, good sensitivity and wide DR. The result of having a wide dynamic range with a value of 12.44 dB and 10.74 dB for 2.4 GHz and 5 GHz respectively, means that the rectifier can operate at a wide range of input power.

The dual-band rectifier offers a sensitivity at 1 V of -12.4 dBm and -11.57 dBm for 2.4 GHz and 5 GHz input frequency respectively. The rectifier showed a great sensitivity at dual-band operation as shown in Figure 8.

The S11 reflection coefficient of the dual-band rectifier was also simulated. It is the ratio of reflected wave to the incident wave. The simulation for the reflection coefficient of the dual-band rectifier shows that the S11 value for 2.4 GHz input is at -10.72 dB and -15.38 dB. On the other hand, S11 for 5 GHz input is at -11.53 dB and -29.84 dB. Each plot shows that it is centered at 2.4 GHz and 5 GHz which is observed to be especially narrow as shown in Figure 9.

Table 1 shows the summary of the performance of the dual-band rectifier as well as its comparison to similar works.

3.3 LDO

The LDO has to be able to withstand sudden full range input supply voltage changes (1.3v - 1.4v). To determine the performance of the designed LDO, parameters such as line regulation, load regulation, and power supply rejection ratio (PSRR) were measured in several simulations.

The line regulation of the LDO is determined to be 1.186 mV/V, demonstrating its capability to maintain a stable output voltage even when subjected to sudden changes in the input supply voltage. This indicates that the LDO effectively regulates the output voltage to compensate for fluctuations in the input, ensuring consistent and reliable operation. On the other hand, the load regulation is measured to be 5.113 mV/mA, indicating the LDO's ability to maintain a stable output voltage in response to load current variations. Tables 2 and 3 summarizes the line regulation and load regulation of the LDO as well as its respective overshoot and undershoot.

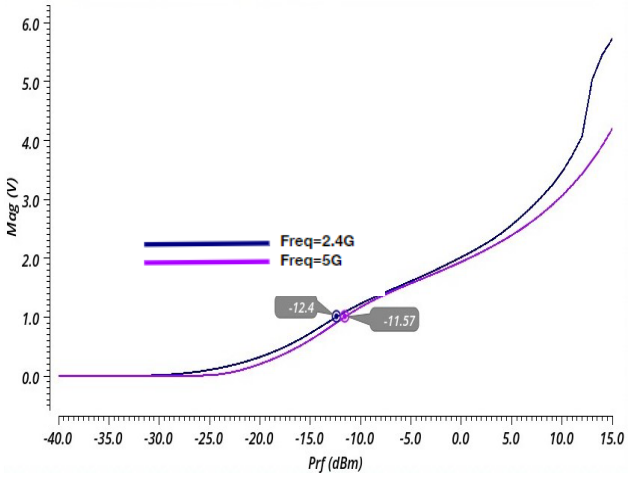


Figure 8 Dual-band rectifier sensitivity at 1V

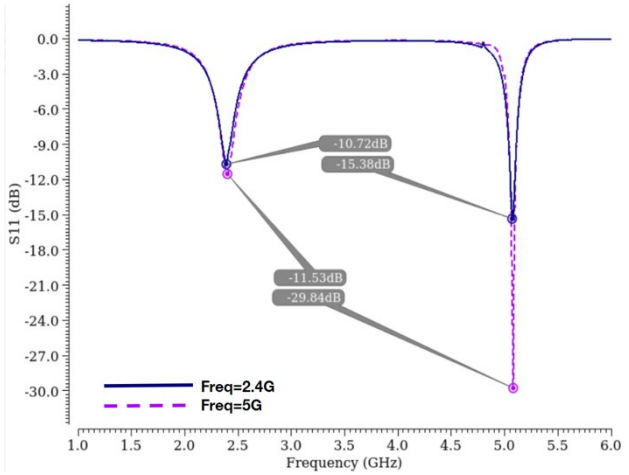


Figure 9 Reflection coefficient (S11) of the dual-band rectifier

Another parameter for LDO performance is the PSRR which is a measure of how well the LDO can reject variations or noise in the input power supply. Table 4 shows a summary of the PSRR at different frequencies. Values from Table 4 imply that the LDO's ability to reject power supply variations diminishes at higher frequencies, potentially leading to a less stable output voltage in the presence of noise or fluctuations in the input power supply

Table 1 Performance Summary and Comparison to Similar Works

Reference	Technology	Technique	Frequency (Hz)	Load (Ω)	Peak PCE @ Pin (dBm)	DR (dB)
[9]	180 nm	Reconfigurable and Adaptive Circuit	900 M 2.4 G 900 M+2.4 G	100 K	69.3 % @ -12 64 % @ -19 67.1 % @ -12	6 6 11
[13]	65 nm	Self-body Biasing	5.8 G	28.8 K	71.8% @ -12.5	N/A
[14]	130 nm	Gate-biasing scheme	900 M	100 K	83.7% @ -18.4[c] 80.3% @ –17[d]	8 7
[17]	180 nm	Adaptive circuit and self Vth cancellation	953 M	10 K	67.5% @ -12	7
[18]	PCB	Transmission lines for matching network	915 M[a] 2.45 G[a] 915 M[b] 2.45 G[b]	2.5 K	81.7% @ 12 73.1% @ 12 69.2% @ 0 64.1% @ -1	11 8 10 9.5
[19]	180 nm	Resistance Compression Network (RCN)	914 M 2.4 G	30 K	43.1% @-12 47.1% @ -6	10 6
[20]	65 nm	Dual-mode Feedback Circuit	433 M	100 K	86 % @ -19	10.1
This work	**65 nm**	**Self-body Biasing**	**2.4 G** **5 G**	**30 K**	**74.93% @ -11** **72.75% @ -11**	**12.74** **10.28**

[a]HSMS2862 Schottky diode; [b]SMS7630 Schottky diode; [c]SCC; [d]ICC

Table 2 Line Regulation Simulation Results

Line Regulation	Undershoot	Overshoot
1.186 mV/V	18 mV	32mV

Table 3 Load Regulation Simulation Results

Load Regulation	Undershoot	Overshoot
5.113 mV/mA	120.052 mV	90 mV

Table 4 PSRR Simulation Results

Frequency	1 kHz	10 kHz	100 kHz
I_{load} = 10 mA	-61.6153 dB	-53.488 dB	-34.289 dB

3.4 Overall System

This section presents the simulation results after integrating the dual-band rectifier along and the LDO. The integration of the LDO provides voltage regulation and stability to the system, ensuring a consistent and reliable power supply to the connected devices.

The dual-band rectifier with LDO as its load shows a peak PCE of 74.79 % at -8 dBm for 2.4 GHz and a peak PCE of 71.25 % at -3 dBm for 5 GHz. Using equation 6, 80% of the peak PCE for both operating frequencies is measured at around PCE > 60% and the design consistently offers a broad dynamic range. The dynamic range for the dual-band operation measured 14.16 dB, shown in Figure 10. As can be observed after the integration of the LDO, the dynamic range of the rectifier was still able to maintain a wide dynamic range for the two frequencies. Meanwhile, the extracted voltage for both input frequencies continue to increase at increasing input power. The LDO block begins regulating 1.2 V from the rectified voltage at input power of -7 dBm and -2 dBm for 2.4 GHz and 5 GHz input frequency respectively. Figure 11 shows the S11 plot after matching the source impedance which is viewed from the antenna side and the load impedance which is viewed from the LDO. Each plot shows that it is centered at 2.4 GHz and 5 GHz.

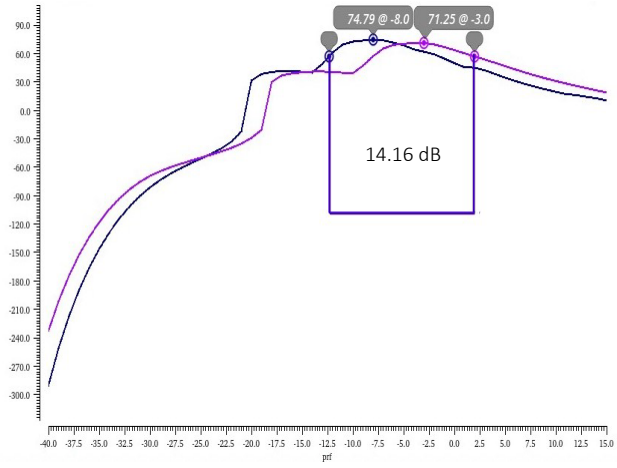


Figure 10 Dynamic range for dual-band operation

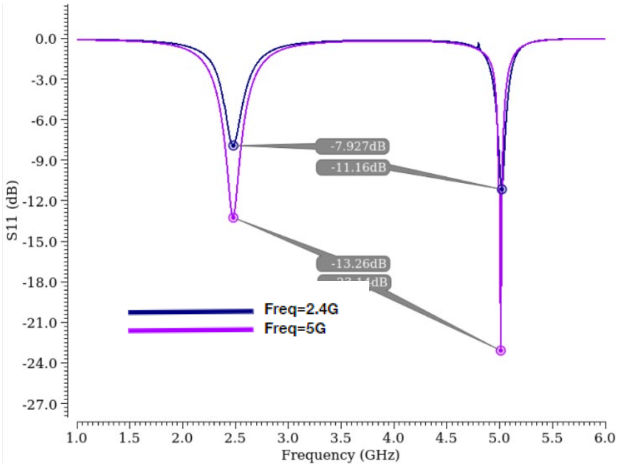


Figure 11 Reflection coefficient (S11) at different input frequency

The S11 for 2.4 GHz input is at -7.927 dB and -11.16 dB. A small spike can be noted for the 2.4 GHz input frequency. On the other hand, S11 for 5 GHz input is at -13.26 dB and -23.14 dB.

3.5 Layout And Post-Sim Results

This section presents the layout of the RFEH system and the post-sim results. The layout of the designed rectifier integrated with LDO, shown in Figure 12, was done through Cadence Virtuoso. The resulting layout of the rectifier and LDO has a dimension of 193.445nm x 178.955nm. The blocks were arranged to achieve a compact shape. The parasitic capacitances arising from the layout were extracted and were considered on the post-sim.

Prior to the layout, the system has a peak PCE of 74.79% at -8 dBm input power and 71.25% at -3 dBm input power for input frequency of 2.4 GHz and 5 GHz respectively with dynamic range of 14.16 dB. Accounting for the parasitic from layout, the observed peak PCE is 65.34% for 2.4 GHz input frequency and 55.56% for 5 GHz input frequency. The post-sim dynamic range is 16.66 dB. Moreover, the post-sim PCE shifted to the right with peak PCE at 0 dBm and 10 dBm for 2.4 GHz and 5 GHz respectively. The PCE of the system before and after the layout is summarized in Table V.

For the 2.4 GHz input frequency the rectifier is able to generate 1V at an input power of -9.73 dBm. The rectifier with input frequency of 5 GHz is able to generate 1V at an input power of -5.116 dB. The parasitic capacitances from the layout shifted the sensitivity of the rectifier to the right being able to generate 1V with an input power of 9.208 dB. Similarly, the post-sim sensitivity of the rectifier with 5 GHz input frequency shifted to the right generating 1V at input power 9.208 dB. The LDO is able to regulate 1.2V at an input power of -7 dBm for 2.4 GHz input frequency. For the 5 GHz input frequency, the LDO can output 1.2V beginning at -2 dBm. The post-sim result of the LDO performance also shifted to the right as it starts to output 1.2V at input power of 11 dBm for both frequencies.

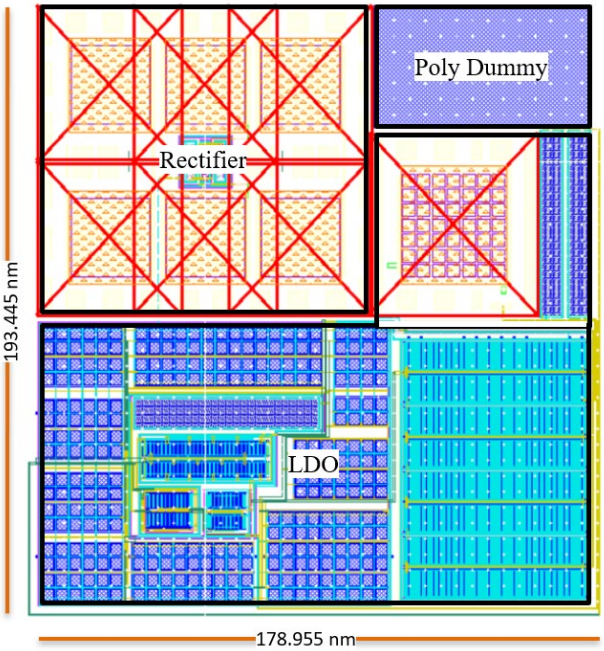


Figure 12 Overall system layout design

As for the reflection coefficient of the system, the system with input frequency of 2.4 GHz had a pre-sim reflection coefficient of -7.927 dB and -11.16 dB. The post-sim result yielded a reflection coefficient of -13.42 dB and -11.04 dB. For the 5 GHz input frequency, a reflection coefficient of -13.26 dB and -23.14 dB was observed on pre-sim. The post-sim reflection coefficient was observed to be -25.44 dB and -13.07 dB. Table V summarizes the performance of the proposed RFEH system before and after the layout.

4.0 CONCLUSION

This study was able to demonstrate a dual-band rectifier operating at 2.4 GHz and 5 GHz frequency band using 65 nm CMOS process Technology through self-biasing technique. The proposed system presents a dual-band rectifier circuit and matching network, as well as an LDO voltage regulator. The proposed system achieved a peak PCE of 74.79 % and 71.25 % at all target frequencies, with sensitivity at -12.45 dBm and -11.52 dBm for both frequencies in the pre-simulation. On the other hand, the post-simulation results garnered a PCE of around 66.48 % and 64.19 % with sensitivity of -12.49 dBm and -11.65 dBm respectively. The LDO regulator successfully maintains a stable output voltage of 1.2 V across different load conditions, demonstrating its effectiveness in voltage regulation and is similar with the findings of [12]. The voltage regulation of the LDO helps ensure a steady output despite variations on the RF signals. Each single-band operating frequency at 2.4 GHz and 5 GHz were able to obtain a high PCE greater than 60 % as well as a wide DR of 14.16 dB by using a two-stage CCDD rectifier architecture and additional coupling capacitors but the additional coupling capacitors led to a larger chip area. It is recommended for future works to work on a capacitorless architecture to save space. It is also recommended to employ

hybrid techniques to further extend the dynamic range and still account for a high PCE.

Acknowledgement

The authors would like to extend their gratitude to the Faculty of Electronics Engineering Department (DECE) at the Mindanao State University – Iligan Institute of Technology (MSU-IIT) and all who have contributed to the success of this study.

Conflicts of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper

References

[1] N. Weissman, S. Jameson and E. Socher, 2014. "W-Band CMOS on-chip energy harvester and rectenna," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), Tampa, FL, USA. 1-3, DOI: 10.1109/MWSYM.2014.6848243.

[2] A. Ray, A. De and T. K. Bhattacharyya, 2018. "2.45 GHz Energy Harvesting On-chip Rectenna in 0.18 µm RF CMOS Process," 2018 IEEE Indian Conference on Antennas and Propogation (InCAP), Hyderabad, India, 1-4, DOI: 10.1109/INCAP.2018.8770967.

[3] Moghaddam, A. K., Chuah, J. H., Ramiah, H., Ahmadian, J., Mak, P.-I., & Martins, R. P. 2017. A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy Harvesting Systems. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(4): 992-1002. DOI: https://doi.org/10.1109/TCSI.2016.2623821

[4] S. Suko et al., 2019. "5.8 GHz Near Field Power Harvesting Circuitry Implemented in 14 nm CMOS Technology," 2019 IEEE International Conference on RFID (RFID), Phoenix, AZ, USA, 1-6, DOI: 10.1109/RFID.2019.8719245.

[5] Muncuk, U., Alemdar, K., Sarode, J., & Chowdhury, K. 2018. Multi-band Ambient RF Energy Harvesting Circuit Design for Enabling Battery-less Sensors and IoTs. I*EEE Internet of Things Journal*, 5(4): 2700 - 2714. DOI: https://doi.org/10.1109/JIOT.2018.2813162

[6] Hu, T., Huang, M., Lu, Y., Zhang, X. Y., Maloberti, F., & Martins, R. P. 2021. A 2.4-GHz CMOS Differential Class-DE Rectifier With Coupled Inductors. *IEEE Transactions on Power Electronics*, *36*(9): 9864 - 9875. DOI: https://doi.org/ 10.1109/TPEL.2021.3061703

[7] A. N. Parks and J. R. Smith, 2014."Sifting through the airwaves: Efficient and scalable multiband RF harvesting," 2014 IEEE International Conference on RFID (IEEE RFID), Orlando, FL, USA, 74-81. DOI: 10.1109/RFID.2014.6810715.

[8] Li, C.-H., Yu, M.-C., & Lin, H.-J. 2017. A Compact 0.9-/2.6-GHz Dual-Band RF Energy Harvester Using SiP Technique. *IEEE Microwave and Wireless Components Letters*, *27*(7): 666 - 668. DOI: https://doi.org/10.1109/LMWC.2017.2711506

[9] Heo, B.-R., & Kwon, I. 2021. A Dual-Band Wide-Input-Range Adaptive CMOS RF–DC Converter for Ambient RF Energy Harvesting. *Sensors 2021*, *21*(22): 7483. DOI: https://doi.org/10.3390/s21227483

[10] Anchustegui-Echearte, Iker & Jiménez-López, D. & Gasulla, Manel & Giuppi, Francesco & Georgiadis, Apostolos. 2013. A high-efficiency matching technique for low power levels in RF harvesting. *Progress in Electromagnetics Research Symposium*. 1806-1810.

[11] Kotani, K., Sasaki, A., & Ito, T. 2009. High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs. *IEEE Journal of Solid-State Circuits*, *44*(11): 3011 - 3018. DOI: https://doi.org/10.1109/JSSC.2009.2028955

[12] Ouda, M., Arsalan, M., Marnat, L., Shamim, A., & Salama, K. 2013. 5.2-GHz RF Power Harvester in 0.18-/spl mu/m CMOS for Implantable Intraocular Pressure Monitoring. *IEEE Transactions on Microwave Theory and Techniques*, *61*(5): 2177 - 2184. DOI: https://doi.org/10.1109/TMTT.2013.2255621

[13] S. Haddadian and J. C. Scheytt, 2019. "A 5.8 GHz CMOS Analog Front-End Targeting RF Energy Harvesting for Microwave RFIDs with MIMO Reader," 2019 IEEE International Conference on RFID Technology and Applications (RFID-TA), Pisa, Italy, 1-5, DOI: 10.1109/RFID-TA.2019.8892037.

[14] Chong, G., Ramiah, H., Yin, J., Rajendran, J., Mak, P.-I., & Martins, R. 2019. A Wide-PCE-Dynamic-Range CMOS Cross- Coupled Differential-Drive Rectifier for Ambient RF Energy Harvesting. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *68*(6): 1743 - 1747. DOI: https://doi.org/ 10.1109/TCSII.2019.2937542

[15] Anticamara, J., Canto, I., Oling, E. 2022. *A low noise, capacitorless low dropout regulator using a 65NM technology*. Mindanao State University - Iligan Institute of Technology.

[16] Hora, J. A. & Vergara, T. L., 2020. High Stability Adaptive LDO using Dynamic Load Sensing for Low Power Management of Wireless Sensor Networks. In 2020 *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. 1-6. IEEE.

[17] Khan, D., Oh, S. J., Shehzad, K., Basim, M., Verma, D., Pu, Y. G., Lee, M., Hwang, K. C., Yang, Y., & Lee, K.-Y. 2020. An Efficient Reconfigurable RF-DC Converter with Wide Input Power Range for RF Energy Harvesting. *IEEE Access*, *8*: 79310-79318. IEEE Xplore. DOI: https://doi.org/10.1109/ACCESS.2020.2990662

[18] Liu, J., Huang, M., & Du, Z. 2020. Design of Compact Dual-Band RF Rectifiers for Wireless Power Transfer and Energy Harvesting. *IEEE Access*, *8*(5): 184901-184908. DOI: https://doi.org/ 10.1109/ACCESS.2020.3029603

[19] Nagaveni, S., Kaddi, P., Khandekar, A., & Dutta, A. 2020. Resistance Compression Dual-Band Differential CMOS RF Energy Harvester Under Modulated Signal Excitation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *67*(11): 4053 - 4062. DOI: https://doi.org/10.1109/TCSI.2020.3006156

[20] Almansouri, A., Kosel, J., & Salama, K. 2020. A Dual-Mode Nested Rectifier for Ambient Wireless Powering in CMOS Technology. *IEEE Transactions on Microwave Theory and Techniques*. *68*(5): 1754-1762. DOI: https://doi.org/10.1109/TMTT.2020.2970