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DESIGN AND COMPARATIVE ANALYSIS OF FINFET BASED 6 T AND 7T-SRAM CELLS FOR IN-MEMORY COMPUTING APPLICATIONS

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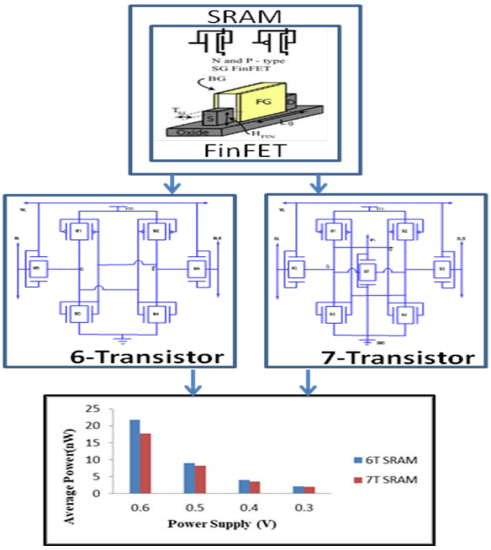
Graphical abstract



Abstract

Since memories are the core components of most digital systems, lowering their power usage can significantly affect the system's stability, performance, and efficiency. SRAM cells are suitable for embedded and portable electronics due to their lower leakage. FinFETs have demonstrated their potential as a low-power, high-performance option at lower technological nodes. One of the main priorities for designers working on semiconductor memories is low power consumption, which can be achieved by reducing transistor leakage current. This article design and compares the average power consumption and noise voltage of 6T as well as 7T SRAM cells using FinFET approach for In-memory computing applications. It has been found that the stability and power handling capacity of an SRAM cell constructed using 45 nm FinFET technology are improved. The proposed 7T FinFET SRAM reduces average power dissipation by approximately 12% and increases the average noise voltage by approx. 7% as compared to 6T SRAM cells. Cadence Virtuoso ADE is used for all designs and simulations.

Keywords: Average power dissipation, static noise margin, FinFET, SRAM, Multi-Gate Transistors, Memory Density

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1.0 INTRODUCTION

Nowadays, the most often employed electronic parts of a digital structure are semiconductor memory. A semiconductor-built memory makes it simple to retrieve data in any random way and from any position on the memory in a hurry. Semiconductor memories require a few nanoseconds to read or write data, making them significantly faster to access than other types of memories. At channel lengths less than 65 nm, CMOS technology is handling amazing jobs including threshold leakage current and gate-induced drain lowering, among others. [1]. Due to their increased gate control across the channel area, which lessens the impact of the drain-induced field into the channel area, multi-gate MOSFETs, like FinFETs, have a significant potential to overcome these restrictions. Due to its improved control across the channel and better flexibility in terms of channel gate, FinFET technology has the ability to completely swap CMOS technology in the most modern SRAM without sacrificing performance [2]. Also, in the sub-threshold region, FinFETs often have lower leakage currents than MOSFETs. As a result, new circuit topologies combined with an efficient FinFET-based smart embedded memory are being investigated for potential applications in the industry [3]. The supply voltage must drop as technology gets smaller in order to maintain dynamic power. The trends of SRAM density and projections is shown in Figure 1.

The general idea of In-Memory Computing model is an architecture where the data is loaded and processed in RAM in contrary to traditional disk-based storage systems eg. Hard-drives, SSD's, HDFS etc. During In-memory computing data processed directly within memory and demands high speed, power-efficient along with densely packed memory architectures [4]. This drastically improves the speed to fetch and process the data because memory access is orders of

magnitude faster than disk access. In-memory computing (IMC) has emerged as a promising alternative to address the von Neumann bottleneck.

IMC integrates computational capabilities directly within the memory array, minimizing data movement and significantly reducing energy consumption and latency. This approach allows for parallel data processing within the memory itself, leading to substantial performance gains for certain types of computations, particularly those involving matrix operations and neural networks. SRAM plays a crucial role in realizing IMC due to its speed, compatibility with standard CMOS processes, and ability to perform basic logic operations. FinFET-based SRAM is highly suitable for use in in-memory computing applications for the following reasons:

- Real-time spiking neural network operations in neuromorphic systems, which mimic the organic neural architecture of the brain, are facilitated by FinFET SRAM-based in-memory computing.
- Large scale data processing in-memory speeds up real-time analytics platforms, which gain from FinFET-based SRAM's fast, low-latency memory access.
- In-memory computing with in FinFET SRAM is the perfect solution for edge devices, which save power by processing data locally at faster speeds as opposed to sending them back to cloud data centers.
- In-memory computing with FinFET SRAM will enable faster handling of big data for AI/ML algorithms. AI models can be run more economically for inference and training workloads by reducing the latency in getting data from where it is stored to where it is processed.

The typical 6T SRAM cell is typically utilized in storage systems because it satisfies strict performance desires and has fairly straightforward operations read as well as write. A 6T SRAM cell uses two transistors for read and writes operations and stores one bit of data in two cross-coupled inverters that form a flip-flop latch). Word-lines are used to turn on access transistors, which make it easier for internal cell nodes to communicate with bit-lines, the cell's input/output ports. Careful transistor sizing is required for read and write stability. Double cross-coupled inverters in a 6T SRAM cell drive bit-lines high and low, respectively, during read operations, improving

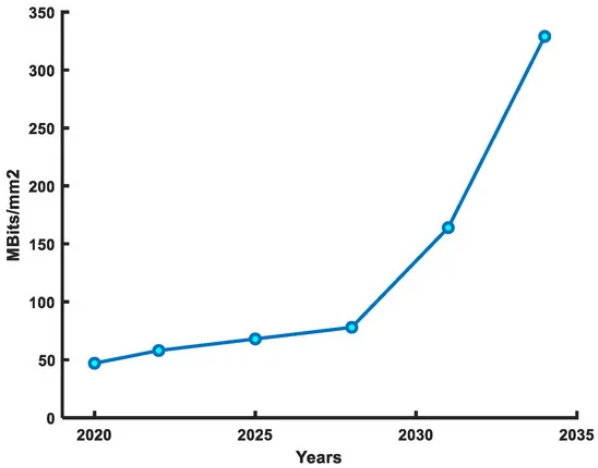

Figure 1 Roadmap of SRAM density improvement as per guideline IRDS-2022 [5]

SRAM bandwidth over DRAM. At appropriate technology nodes, CMOS, FinFET, and/or CNTFET devices may be used to create a 6T-SRAM cell [6-8]..

The 7T SRAM cell, with its additional transistor, offers enhanced read stability and the potential for more complex in-memory operations, but at the cost of increased area and power consumption. The design trade-offs between 6T and 7T SRAM cells are critical considerations for optimizing IMC architectures for specific applications. Furthermore, innovative circuit techniques and architectural modifications are being explored to enhance the computational capabilities of both 6T and 7T SRAM cells for IMC.

The innovation of this work lies in the comprehensive analysis and comparison of FinFET-based 6T and 7T SRAM cell designs specifically tailored for in-memory computing applications. While previous research has explored the individual characteristics of these cell types, a direct comparison focusing on their suitability for IMC, considering both performance and energy efficiency metrics, is lacking. This work aims to bridge this gap by providing a detailed evaluation of the two cell designs under identical operating conditions and with a focus on key IMC-related performance indicators. Furthermore, this analysis will explore novel design techniques to optimize the performance of both 6T and 7T SRAM cells for specific IMC tasks, such as vector-matrix multiplication, which is a fundamental operation in many machine learning algorithms. The current research landscape emphasizes the need for energy-efficient hardware accelerators for AI, making this analysis particularly timely and relevant [9-10].

The objective of this research is to analyze the design of FinFET-based 6T and 7T SRAM cells for in-memory computing applications and gives a comparison of power consumption and robust read/write processes for 6T and 7T FinFET SRAM on a 45 nm technology node.

The majority of current research focuses on improving SRAM cell performance in expressions of power consumption and logic level throughout the read and write cycles. However, in this case, SRAM cell stability, noise voltage is also examined and contrasted with current architectures. First, a 45 nm FinFET is used in the creation of a 7T SRAM cell. Its performance is then examined and contrasted with that of various SRAM cell topologies. Second, the stability, noise voltage of a 7T SRAM cell is analyzed and compared with read-write operations.

The comparative study of different types of SRAM cell having FinFET is examined on the basis of its various technologies, distinct features and utilized design approaches. A comparative study of different types of SRAM cell is shown in table 1[11].

Table 1 Comparative analysis of different types of SRAM cells having FinFETs.

S. No.	Year of Publication	Reference	Transistor utilized for SRAM	Explanations
1	2021	[12]	6 FinFET	Dynamic voltage is fed at body terminal
2	2017	[13]	7 FinFET	No need for RBL charging and supply of voltage is reducing.
3	2016	[14]	7 FinFET	Effective design solution for the NTV area which mix high performance with minimum energy utilization.
4	2015	[15]	7 FinFET	Read as well as write operation will be improved and minimize write time
5	2015	[16]	9 FinFET	Minimize power consumption to one third
6	2014	[17]	8 FinFET	Minimum Sub threshold swing utilizing Fin-FET design.
7	2013	[18]	10 FinFET	Stability upgrades by +ve feedback as well as back gate biasing

1.1 In-Memory Computing: A Paradigm Shift

In-memory computing (IMC) then presents itself as a viable solution to bypass the von Neumann bottleneck by a radical redesign of how calculations are conducted. Rather than shifting data to another processing unit, IMC executes calculations within the memory unit itself. This shifts the paradigm away from the necessity of constant data movement, greatly minimizing latency, power usage, and overall processing time. Through the inclusion of processing functions within the memory infrastructure, IMC makes it possible for huge parallelism and effective data processing [19-20].

The main benefit of IMC is its capacity to utilize the parallel nature of memory arrays. Through calculations in parallel within several memory cells, IMC can deliver a considerable acceleration of computation in relation to standard von Neumann computing systems. IMC also cuts down energy dissipation through minimal data movement, which accounts for a lot of power consumption in traditional systems. This renders IMC especially compelling for usage scenarios where energy consumption is crucial. IMC is extremely promising across a broad variety of applications such as machine learning, data analysis, and scientific computing. With the ability to process large volumes of data quickly and efficiently, IMC has the potential to speed up algorithm and application innovation in these domains.

1.2 Useful Terms

1.2.1 Area and Yield

The density and functionality of storage design are its most crucial characteristics. Ensuring a sufficient noise gap between outputs is crucial for maintaining functionality in large memory. By appropriately sizing the device, the noise margins can be decreased. The functionality can also be enhanced by choosing supply and threshold voltages. Transistor sizing reduces memory density as cell area grows [21].

1.2.2 Read and Write Stability

The voltage division between the pull-down as well as access transistors determines the lowest voltage that can be achieved across a read operation, which is referred to as the read voltage. Low access transistor driving strength, which lowers read voltage, is an indicator of read stability. Write voltage, which is the highest voltage that may be obtained during a write operation, is calculated by divide the voltage between the access transistor and the pull-up transistor. Strong access transistor driving strength, which lowers write voltage and can be used to verify write stability [22].

1.2.3 Speed and Leakage Current

SRAM cells are always required to have low leakage power, which improves cell performance and operating speed. Low threshold voltages can be used to boost speed, but they also increase the device's leakage power. Less threshold voltage results from increasing voltage scaling; this raises speed and increases leakage power. To overcome leakage power and high threshold voltages may be utilized, but the performance cost is too high [23].

1.3 Benefits and Drawbacks of FinFETs for In-Memory Computing Applications

1.3.1 Benefits

- FinFETs significantly reduce leakage current due to their improved gate control. With the presence of several gates encircling the channel, they attain improved electrostatic control, leading to a reduction in subthreshold leakage. This feature makes FinFETs ideal for low-power applications such as mobile devices and battery-powered electronics.
- FinFETs provide increased drive current and faster switching speeds based on their better control of the channel. This results in lower switching delay and enables increased operating frequencies, making them suitable for high-performance computing, artificial intelligence, and data centers [24].
- With shrinking transistors, conventional MOSFETs are plagued by SCEs such as reduction in threshold voltage and leakage enhancement. FinFETs counter these issues by

encircling the gate over the channel, improving electrostatic control and reducing leakage current.

- FinFETs allow more transistors to be integrated into the same space, increasing transistor density. This increases chip efficiency and aids in the continued Moore's Law trend, allowing for more powerful processors in smaller form factors.
- In MOSFETs with a planar structure, doping concentration variations can lead to threshold voltage instability. FinFETs demand less doping, creating a more stable threshold voltage, thus improving integrated circuit reliability.
- FinFETs have greater transconductance and less noise susceptibility owing to their enhanced gate control. This makes them especially ideal for analog and RF applications where signal integrity has to be preserved.

1.3.2 Drawbacks of FinFETs

- The production of FinFETs uses multi-patterning processes, accurate etching and state-of-the-art lithography, which means the manufacturing process is more complex than that of planar MOSFETs. Increased complexity takes longer to produce and requires sophisticated fabrication facilities.
- The complex nature of the FinFET process drives production at a higher cost. Firms have to invest in new equipment and redesigning circuits in order to exploit FinFET technology to the hilt, an expensive undertaking [25].
- Pre-designed circuits must be modified to accommodate the 3D nature of FinFETs, making the design process more complex.
- The 3D nature of FinFETs introduces additional parasitic resistances and capacitances that can impact the performance of the circuit. Managing these elements is important, particularly in high-speed circuits.
- FinFETs also exhibit greater power density due to their smaller size, which can lead to thermal issues. This creates the need for efficient heat dissipation techniques so that the reliability of the device is maintained.

The pictorial view for benefits and drawbacks of FinFET for SRAM cell design is as shown Figure 2 (a) and 2 (b) respectively.

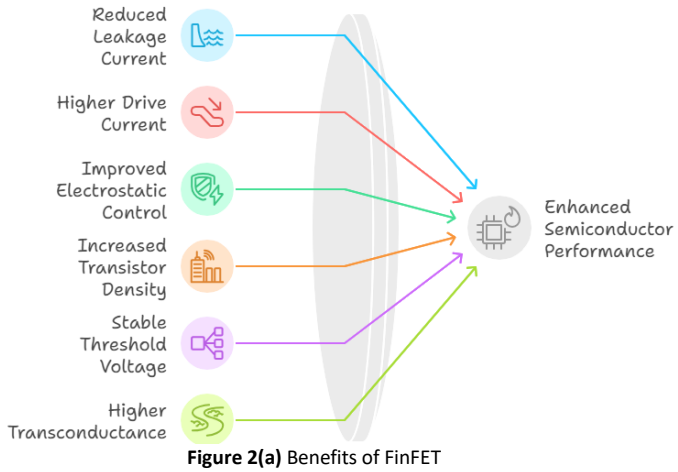

Figure 2(a) Benefits of FinFET

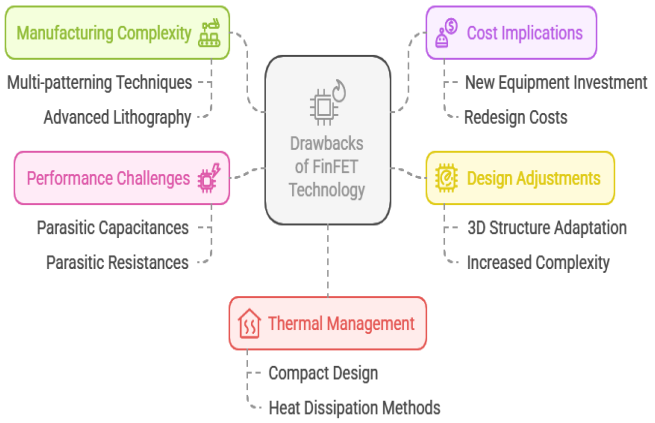

Figure 2(b) Drawbacks of FinFET

2.0 METHODOLOGY

Because of their decreased leakage, SRAM cells are appropriate for embedded and portable devices. At lower technical nodes, FinFETs have proven to be a promising low-power, high-performance solution. Low power consumption is a top goal for designers working on semiconductor memory, and this can be accomplished via lowering transistor leakage current. The suggested methodology focuses on creating FinFET-oriented SRAM cells that are less power-hungry and perform better than traditional 6T and 7T SRAM cells [26].

2.1 Methodological Flow

The design flow of proposed SRAM cell design is as shown Figure 3 and used steps in designing are given as:
Step-1: First, launch the Cadence Virtuoso application.
Step-2: Use instances to create the schematic diagram for the 6T and 7T SRAM cells.
Step-3: Instruction for identifying errors in schematic diagram.
Step-4: Create the symbol and save the diagram.
Step-5: Instruction for identifying errors in symbol.
Step-6: Create the remaining design after saving the symbol.
Step-7: Use specter to launch the simulation and confirm the analysis results.
Step-8: If satisfied with reports, generate the report using parametric analysis and note down the reading.

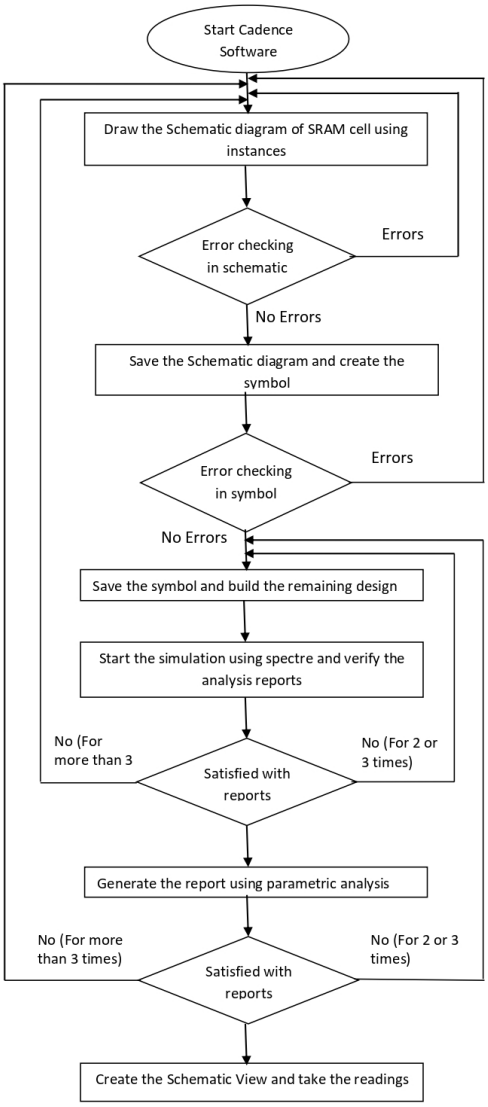

Figure 3 Design flow for designing of SRAM cell

2.2 FinFET Structure

Below 45 nm, FinFET technology has been overtaking CMOS technology and successfully replacing it. For at least three or four technology generations, this trend is anticipated to persist. FinFETs' multi-gate construction allows for more electrostatic control over the channel. This significantly improves the behavior of the short channels in nanoscale technologies. Light body doping is used in FinFET transistors to reduce random dopant fluctuations (RDF). This reduces the Ion/Ioff current and process fluctuation even more. FinFETs are becoming into a superior replacement for traditional bulk FETs in nano-scaled technologies as a result of their advantageous features and device properties [27–30]. Figure 4 illustrates the structure of planner FET and FinFET [31]. FinFET technology enhances controllability for low voltage operations by adding a second gate across from the conventional gate. The functions of both gates are used in a FinFET. FinFET is also known as multigate device.

A FinFET is an advanced type of multi-gate transistor that overcomes the limitations of traditional planar MOSFETs by providing better electrostatic control over the channel. The key distinguishing feature of a FinFET is the fin-like structure of the channel, which rises above the substrate and is surrounded by the gate on multiple sides. This design helps to suppress short-channel effects (SCEs), allowing FinFETs to operate efficiently at nanoscale dimensions. The two-dimensional structure of a FinFET is shown in Figure 5. The FinFET device is generally constructed on a semiconductor substrate, usually silicon. The most defining characteristic of a FinFET is the narrow, vertical, fin-shaped channel that acts as the conduction channel for current flow. This fin extends from the substrate and is typically constructed of silicon. The fin's height and width may differ based on the particular manufacturing process and design specifications. The gate is surrounding the fin and is constructed from a dielectric material like silicon dioxide (SiO_2). The gate electrode regulates the current through the fin using an electric field. On either side of the fin is the source and drain regions, which are highly doped with impurities in order to make it easy for charge carriers (electrons or holes) to flow into and out of the channel. Underneath the gate electrode is a thin gate dielectric material layer that electrically insulates the gate from the channel. Silicon dioxide and high-k dielectrics are typical gate dielectric materials, which are used to provide higher dielectric constants to decrease gate leakage current. Spacer material is usually applied to create isolation between the gate electrode and source/drain areas. These spacers assist in regulating the gate width and the channel length, which affects the performance of the transistor.

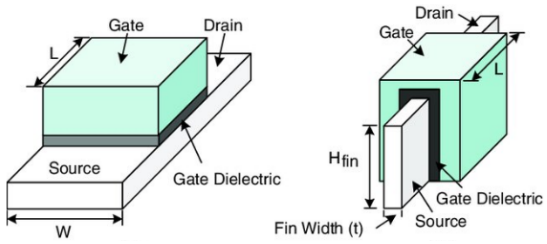

Figure 4 Structural View [31] (a) planar MOSFET and (b) FinFET

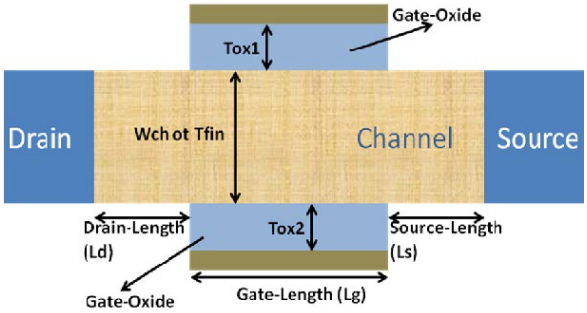

Figure 5 Two-dimensional structure of FinFET

FinFET is a type of transistor design that has become increasingly prevalent in modern semiconductor manufacturing processes. Here are some key features of FinFETs:

1. **Three-Dimensional Structure:** FinFETs have a three-dimensional structure, featuring a thin vertical "fin" of silicon protruding from the substrate. This vertical fin forms the conducting channel of the transistor.
2. **Improved Control over Gate:** The gate electrode of a FinFET wraps around the fin, providing superior control over the flow of current compared to traditional planar transistors. This upgraded control helps reduce leakage current and improves energy efficiency.
3. **Reduced Short Channel Effects:** Short channel effects refer to issues that arise when transistors are scaled down in size, leading to decreased control over the flow of current. FinFETs mitigate these effects due to their three-dimensional structure, allowing for better electrostatic control and reduced leakage current even at smaller transistor dimensions.
4. **Better Performance:** FinFETs typically offer better performance metrics such as lower delay, lower power consumption, and improved scalability compared to planar transistors. This improvement is particularly significant in sub-20nm semiconductor manufacturing processes and beyond.
5. **Multiple Gate Configurations:** FinFETs can be implemented in various gate configurations, such as tri-gate, quadruple-gate, and even more complex designs. These configurations further enhance control over the transistor's behavior and improve its performance.
6. **Compatibility with Advanced Nodes:** FinFET technology has been widely adopted in advanced semiconductor manufacturing processes. Its scalability and performance make it a crucial component in modern integrated circuits, especially for high-performance computing applications.
7. **Manufacturing Challenges:** While FinFETs offer significant advantages, their manufacturing process is more complex compared to traditional planar transistors. Fabricating FinFETs requires precise control over the etching and doping processes to create the vertical fins and the gate structure around them.

2.3 Cell Operation of 6T-SRAM

In Figure 6 shows the 6T SRAM cell configurations. Cutting the feedback connection between these dual inverters is necessary to allow writing in the cell. Between the inverters, an NMOS transistor facilitates the process. In comparison to a 6T cell, this aids in obtaining a high NM. Write operations in 7T cells are solely dependent on BL (single ended operations). In this SRAM, two P-type and 4- N-type FinFETs are used. Transistor M5 and M6 works as an access transistor whereas FinFETs M1, M2, M3, M4 works as single bit memory storage connected as a cross coupled structure. The different working operations of 6T SRAM using FinFET are discussed below:

Throughout the write operation, WL =1 is maintained. BLB is elevated to V_{DD} and BL will be depressed to 0V and if the cell contains 1 and 0 is to be written. A few considerations must be made in order for the SRAM cell to operate properly during read and write operations. The stability of read and write operations is determined by these design flaws [32-34].

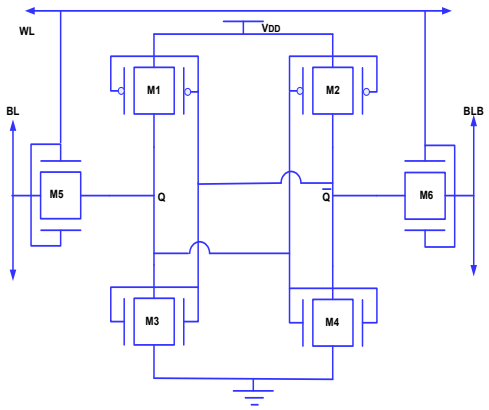

Figure 6 6T SRAM cell using FinFET

Throughout the read operation, the bit lines BLB and BL enable the access transistor and connect cell when WL=1. Values kept in nodes Q and $\overline{Q}$ are moved to corresponding bit-lines BL and BLB during the read operation. Transistor M1 and M2 will be ON and M3 and M4 will be OFF if 1 is stored at node Q. Through the driver transistor M2, BLB will be discharged, and BL will be dragged up and toward V_{DD} through the load transistor M1 [27–28].

Throughout the hold operation, as illustrated in Figure 3, no word line assertion occurs in this mode (WL=0), so access transistors M6 and M5 will be OFF and no data will be accessible via BL's. As long as the cross-coupled inverters are connected to the supply, they will continue to feedback with one another and stand-by the data in the latch [32–35].

2.3.1 Challenges of 6T SRAM for In-Memory Computing

The strong points of the 6T SRAM cell manifest during data storage; however, its unique architecture is proving extremely difficult for in-memory computing applications to deal with. The weakest point, though, lies with the parameter in whose designs its optimization stands: storage of data and retrieval thereof, but for performing complex computations on input signals not. The standard 6T SRAM cell carries no additional circuitry that performs arithmetic or logic operations within the memory array.

One of the major hurdles related to the use of the 6T SRAM cell for enabling in-memory computing functionalities is keeping the stability and reliability of the cell intact. Integrating additional transistors or sizing some of the existing transistors to enable computational functions will disrupt the fragile balance of the cross-coupled inverters, which may lead to compromising the cell's ability to retain data. Additionally, with the complexity of the design in terms of cell size and power consumption, all these might eliminate the advantages of performing in-memory computing. A larger area means less memory density, and higher power consumption would mean the energy efficiency of the system is limited. Therefore, careful consideration of the mentioned trade-offs is imperative for the cell to be functional and efficient as an in-memory computing SRAM cell.

2.4 Cell Operation of 7T-SRAM

Figure 7 displays the circuit diagram for a 7T SRAM cell that uses a FinFET. In this SRAM, two P-type and 5- N-type

FinFETs are used. Transistor M5 and M6 works as an access transistor whereas FinFETs M1, M2, M3, M4 works as single bit memory storage connected as a cross coupled structure and M7 is an extra FinFET transistor is used in the center of SRAM cell for controlling the leakage. The different working operations of 7T SRAM using FinFET is discuss below.

Throughout the write operation, the WL is enabled once the required data has been imported into BL. Turning on the access transistors (M5) enables the bit-lines to drive the cross-coupled inverters to the desired state. The write-enable transistor controls whether the data stored in the cell can be overridden. The ability to override the data stored in the cell is determined by the write-enable transistor. For writing "1" in the SC, BL needs to be held accountable to V_{DD}. Should '0' need to be written down, then WL represents the power supply level and BL is low. In write mode, RL is not in use.

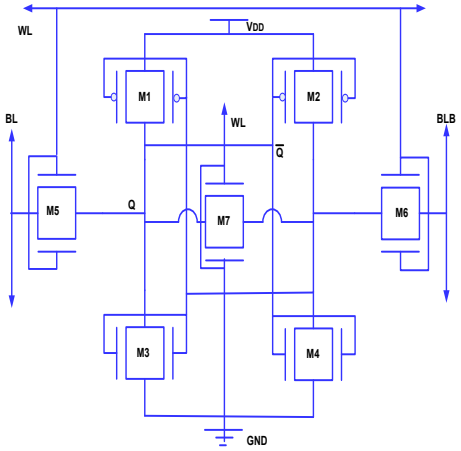

Figure 7 7T FinFET SRAM cell

Throughout the read operation (WL =1), the access transistors (M5, M6) are on. The cell's condition is determined by sensing the difference in voltage between the bit-lines. After that, the data is retrieved without changing its stored state. The BL, which is already charged to V_{DD}, may read the data in the cell. When RL is first charged, it turns on. The read operation is carried out based on the state of BL; if BL is charging to VDD, then the read data is '1'; if BL is discharging, then the read data is '0'.WL is never ON throughout this operation.

Throughout the hold operation (WL = 0), the transistor M1 and M2 are turned off. A sub-threshold leakage current passes through the transistors in the OFF state as a result of logic 0 in the SRAM cell. Additionally, the additional transistor M7 connects and disconnects feedback, and the SRAM cell just needs the BLB to carry out write operations.

2.4.1 Advantages of 7T SRAM for In-Memory Computing

- The improved features of the 7T SRAM cell make it especially suitable for in-memory computing applications. In-memory computing seeks to execute computational operations directly within the memory array, without transferring data between the memory and the processing unit, thus minimizing latency and energy expenditure. The 7T SRAM cell supports this paradigm by allowing more efficient and robust implementation of computational primitives within the memory array.
- One of the 7T SRAM cell's main benefits is its enhanced read stability. For in-memory computing, several read accesses could be necessary to execute a single computation, e.g., a multiply-accumulate (MAC) operation. The read disturb phenomenon in 6T SRAM cells will cause errors in such computations, particularly with large arrays and operations of high complexity. The 7T SRAM cell decoupled read path eliminates this problem, making it possible for more reliable and accurate in-memory computations.
- In the 7T SRAM cell, the seventh transistor can be used to facilitate a specific in-memory computing functionality and perform a bitwise XOR operation within the memory cell. The output of the XOR operation can be retrieved without disturbing the stored data by accurately controlling the voltage on the read word line and bit lines. This functionality can be utilized for more sophisticated arithmetic and logical computations within the memory array to enhance the overall efficiency of in-memory computing.
- Take, for instance, the MAC operation, which serves as a standard building block among numerous machine learning algorithms. Based on 7T SRAM cells, an individual MAC operation would involve reading input data from more than one cell, a bitwise multiplication by exploiting the seventh transistor, and then accumulation using the charge-sharing process. This method can greatly minimize energy usage and latency over conventional von Neumann architectures, in which the data has to be transferred to a different processing unit for computation. The 7T SRAM cell thus offers a promising platform for achieving energy-efficient and high-performance in-memory computing systems.

3.0 RESULTS AND DISCUSSION

The average power dissipation affects the threshold voltage and mobility of SRAM cell. This average power occurs on account of biasing, wiring as well as loose connections. The voltage control and or technological variations techniques are used to manage the power dissipation. A Fin-FET based SRAM cell is used in the design configuration of a low-power solution. Every computation is based on the local temperature of 27°C.

Table 2 gives a comparison of the average power of 6T and 7T Fin-FET based SRAM. The P-V comparison for various supply voltages of 6T & 7T SRAM is shown in Figure 7.

Table 2 Comparison of average power between 6T and 7T Fin-FET based SRAM

Supply Voltage (V)	Average power dissipation (nW)	
	6T SRAM	7T SRAM
0.6	21.76	17.76
0.5	8.96	8.26
0.4	3.968	3.498
0.3	2.161	1.946

Here, we compare the 6T and 7T SRAM cell using FinFET on the basis of two different parameters such as power dissipation and noise. It can be seen that when compare power dissipation of proposed 7T SRAM with previously designed 6T SRAM for

multiple power supply, 7T SRAM dissipate less power, means provide high handing capacity during the read or write operation. Figure 8 gives the comparative chart of power dissipation for 6T and 7T SRAM for better understanding.

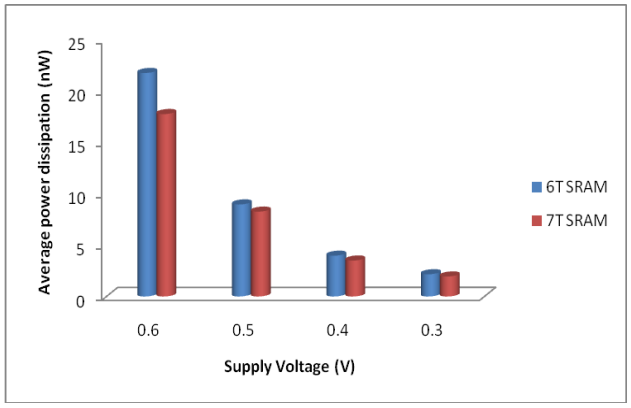

Figure 8 Comparative chart of power dissipation for 6T and 7T SRAM

Noise, an undesired signal, has the potential to distort data within an SRAM cell particularly during write operations. When the output data in the cross-coupled inverters are in a hold mode, noise can introduce variations at the output terminals specifically at Q and $\overline{Q}$. A comparative analysis of average noise voltage between 6T and 7T Fin-FET based SRAM is offered in Table 3.

Table 3 Comparison of average noise voltage between 6T and 7T Fin-FET based SRAM

Supply Voltage (V)	Average Noise Voltage (nV)	
	6T SRAM	7T SRAM
0.6	6.232	6.524
0.5	6.124	6.436
0.4	4.892	5.424
0.3	2.446	2.862

Figure 9 gives the comparative chart of Noise Voltage for 6T and 7T SRAM for better understanding.

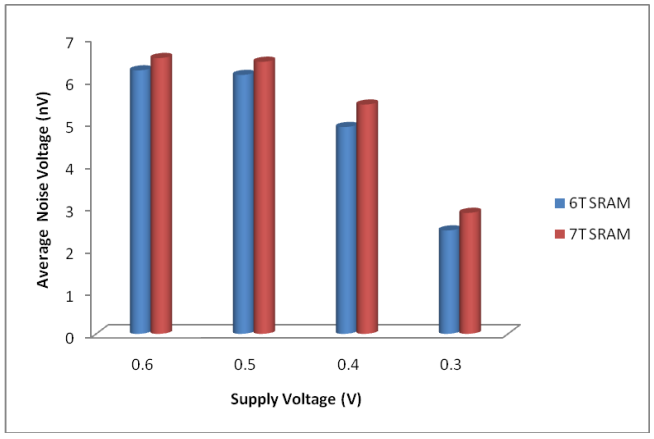

Figure 9 Comparative chart of Average Noise voltage for 6T and 7T SRAM

The comparative chart of Average power dissipation and average Noise Voltage for 6T and 7T SRAM is shown in Figures 10 & 11 respectively.

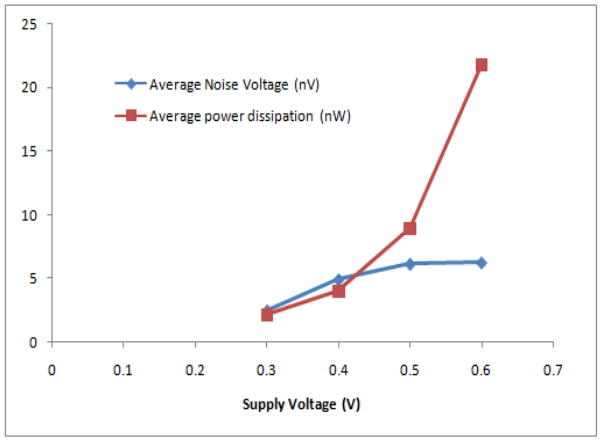

Figure 10 Comparative chart of Average Power and Average Noise voltage for 6T SRAM.

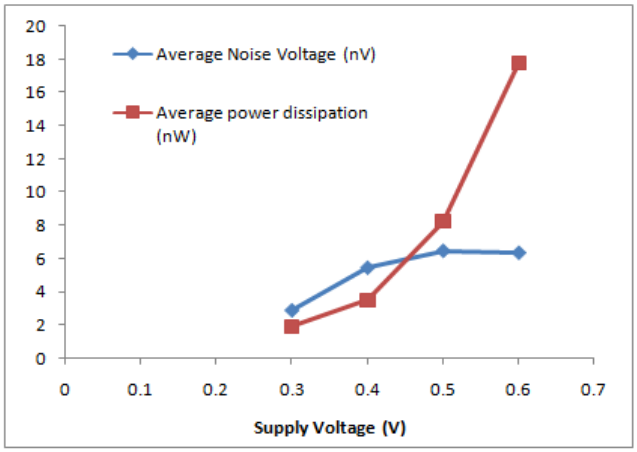

Figure 11 Comparative chart of Average Power and Noise voltage Comparative chart for 7T SRAM

3.1 Challenges

Although there are lots of benefits of FinFET-based SRAMs but it also has few challenges, such as:

- The FinFET device fabrication process is more intricate than the fabrication of planar devices, causing higher manufacturing costs.
- FinFET SRAM scaling down heat dissipation becomes a problem at some heating system speed due to its high-speed data processing in the case of in-memory computing applications.

4.0 CONCLUSION

This research paper presented a comprehensive performance comparison and study of 6T and 7T SRAM cells implemented using FinFET technology, with a focus on exploring variations and deriving insights into their average power dissipation. Firstly, the 6T SRAM cell, being the conventional choice,

exhibited commendable performance in terms of static noise margin (SNM) and read stability. The power consumption analysis indicated that while the 6T cell maintains lower active power usage, its leakage power can be a concern, especially in low-power applications.

On the other hand, the extra transistor in the 7T SRAM cells makes read and write performance better, which fixes some of the problems with the 6T design. The 7T configuration exhibits better tolerance to process variations and enhances robustness. On the other hand, this may increase area and marginally increase power consumption, creating a trade-off depending on application requirements.

The comparative analysis indicated that while the 6T SRAM cell remains a good option for some mainstream applications, given its smaller area and higher power consumption, the 7T SRAM cell brings a great advantage to the table with respect to requirements of higher stability and reliability. The latter-FinFET technology-provides much better control over short-channel effects and therefore reduces leakage currents, which significantly enhances the performance of both SRAM cell designs, making them much more attractive for future high-performance and low-power electronic systems.

FinFET-based SRAM technology enables the next generation of memory-intensive computing. Owing to better read/write speed, good power efficiency, and scalability, it suits applications for which high-performance memory solutions or real-time data processing is necessary. The proper performance benefits with power control required by highly memory-intensive computing will lend itself to FinFET SRAM, including AI, big data, and neuromorphic computing.

In conclusion, it is found that the stability and power handling capability of a FinFET SRAM cell are improved in a 45-nm process. With the introduction of 7T FinFET SRAM, solution average power dissipation decreases by around 12%, while average noise voltage improves by approximately 7% compared with the standard 6T SRAM cells.

Nomenclature			
AI	Artificial Intelligence	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
BG	Back Gate	ML	Machine Learning
BL	Bit Line	NM	Noise Margin
BLB	Bit Line with Bar	NTV	Near Threshold Voltage
CMOS	Complementary Metal Oxide Semiconductor	PDP	Power Delay Product
CNT	Carbon Nano Tube	RL	Read Line
CR	Cell Ratio	RBL	Read Bit Line
DG	Double-Gate	RNM	Read Noise Margin
DRAM	Dynamic Random Access Memory	SCE	Short Channel Effects
FET	Field Effect Transistor	SNM	Static Noise Margin
FinFET	Fin Field Effect Transistor	SRAM	Static Random Access Memory
FP	Fin Pitch	TFET	Tunnel FET
GP	Gate Pitch	T_{Fin}	Thickness of Fin
H_{FIN}	Height of silicon Fin (distance between top gate and buried oxides)	T_{OX1}	Front- gate thickness of oxide layer of FinFET
IC	Integrated Circuit	T_{OX2}	Back-gate thickness of oxide layer of FinFET
IG	Independent gate	V_{DD}	Positive Power Supply
IMC	In-Memory Computing	VLSI	Very Large-Scale Integration
IoT	Internet of Things	V_{SS}	Ground
L_d	Drain Length	V_{TH}	Threshold Voltage
L_S	Source Length	W_{fin}	Geometrical channel width ($W_{fin}=2H_{fin}+T_{Si}$)
L_G	Gate Length	WL	Word Line

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Conflicts of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper.

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