

INTER-PORT POWER SHARING OF A SPV-BATTERY INTEGRATED THREE PORT SOFT-SWITCHED DC-DC CONVERTER

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Article history

Received

22 July 2025

Received in revised form

04 November 2025

Accepted

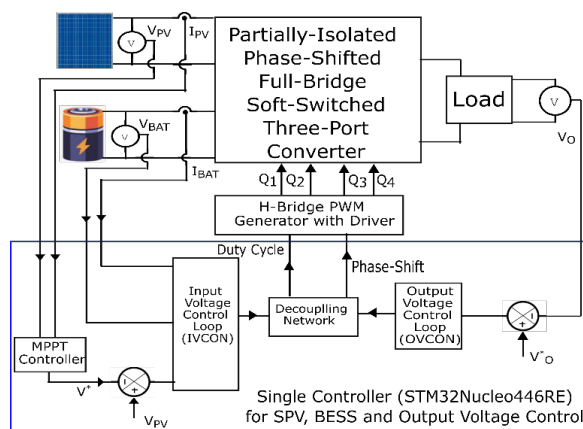
20 November 2025

Published online

31 May 2026

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Graphical abstract



Abstract

A soft-switched isolated three-port converter (TPC), integrating solar photovoltaic (SPV) source, battery storage and load is proposed in this work. The load port is isolated from the SPV source and battery port by a high frequency transformer. The proposed TPC is built on the modified structure of phase-shift full bridge (PSFB) converter. All switches of the converter operate under soft-switched conditions and the diodes recover softly. Brief operating principle, small signal modelling and controller design for the inter-port power sharing, load voltage regulation, maximum power point tracking (MPPT) of SPV source, and charge/discharge control of the battery storage are elaborated in this work. Finally, a hardware prototype of rated 144W, 48V, 100kHz has been developed in the laboratory for real-time performance verification. In various operating scenarios, the soft-switching behavior of the active switches, dynamic stability of the controller and the regulated load port power transfer have been established with 95.2% efficiency.

Keywords: Inter-port power sharing, MPPT, PSFB converter, soft-switching, three-port converter

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1.0 INTRODUCTION

Extensive studies are conducted on renewable energy systems to mitigate environmental pollution and global warming. Solar photovoltaic (SPV) is the most useful renewable energy source available across the world [1]–[3]. However, the erratic pattern of SPV generation necessitates integration of battery energy storage systems (BESS) or super-capacitors to enhance the system reliability by bridging the gap between inconsistent generation and uncontrolled load demand [4]. Power electronic converters play the crucial role of linking the SPV sources, BESS and the load. In conventional systems, the SPV source is linked to the load through a DC–DC converter for voltage level matching and maximum power extraction and a bidirectional DC–DC

converter is utilized for integrating the BESS to the SPV source or the load terminals. Such multi-stage architectures suffer from the disadvantages of low efficiency, increased dimension, reduced power density, and elevated cost. Three-port converters (TPC) integrating SPV source, BESS and the load has emerged as a potential option for such applications. The various TPC topologies, suggested in recent literatures, can be broadly classified into isolated, non-isolated, and partially isolated categories. Non-isolated TPCs [5]–[12] with the main advantage of reduced component count are the best choice for applications, where galvanic isolation is not a mandatory requirement. However, the mandatory safety requirement of load-port isolation in grid-tied SPV systems have prompted the development of many isolated TPCs [13]–[20] with all ports

isolated from each other by high-frequency transformers. These topologies are mostly developed on dual active bridge (DAB) configurations [21], series resonant converters (SRC) [4], [17] or triple active bridge (TAB) structures [22]. These converters can provide extended voltage gain by the adjustment of the transformer turns-ratio. However, proper handling of the transformer leakage energy is a major challenge, as it causes increased device stress, considerable power loss and interferences to communication networks [23]. Moreover, usage of two transformers and many components makes the isolated TPC structures bulky, heavy and costly [4]. Partially isolated TPCs, using only one high frequency transformer for load port isolation, is therefore a preferred choice than the isolated topologies for SPV applications [24]–[30]. Many new configurations of partially isolated TPCs have been proposed in recent years with their own advantages and limitations. The half bridge based partly isolated TPCs, suggested in [31]–[34], achieved effective power management and smooth mode transitions using a decoupling control network. However, large circulating current conduction loss and hard switching converter operation are the main drawbacks of such topologies. Full-bridge isolated TPCs presented in [35] have the advantages of reduced input current ripple and smooth switching operation. Phase shift full bridge (PSFB) converter based partially isolated TPCs allow smooth regulation of inter-port power transfer through control of duty cycle and phase-shift angle [31], [36], [37]. However, circulation of the passive mode freewheeling current is a major issue for such topologies [38].

This paper proposes a new partially isolated TPC [PI-TPC] integrating SPV source, battery storage and an isolated port for DC load or electric vehicle (EV) charging. Although the proposed TPC is based on the PSFB structure, it effectively eliminates passive mode circulating current and unnecessary conduction loss by integrating a compact current resetting network on the secondary side of the high-frequency transformer. All switches of the converter operate under soft-switched conditions and the diodes recover softly. The proposed converter with isolated load port enjoys the features of compact structure, reduced device stress and switching loss, and high efficiency. A centralized controller has been implemented in this work for inter-port power transfer with load voltage regulation, maximum power point tracking (MPPT) of SPV source, and charge/discharge control of the BESS. Finally, a hardware prototype of rated 144W, 48V, 100 kHz has been developed in the laboratory for the real-time performance verification.

This paper is organized in ten different sections. Section 1 provides a brief introduction, while section 2 describes the converter's operation. The overall control scheme and multiple operating modes of the suggested TPC are covered in sections 3 and 4 respectively. Section 5 presents the converter design considerations. The controller design with stability analysis is presented in section 6. Sections 7 provide an explanation of the experimental results, while Section 8 compares the suggested converter to other recent topologies. Finally, section 9 represents the conclusion.

2.0 MATERIALS AND METHODS

The proposed TPC, as depicted in Figure 1, is a structurally modified PSFB converter with integration of SPV source (V_{PV}) and battery (V_{BAT}) at primary side of a high frequency transformer and the load port (V_O) on the secondary side.

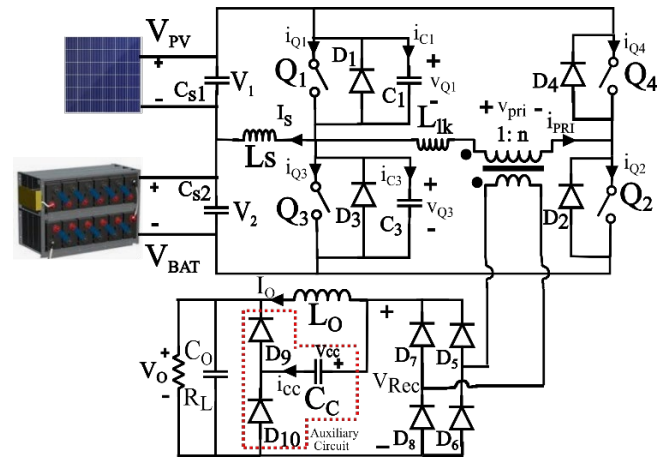


Figure 1 Power Circuit of proposed three-port converter

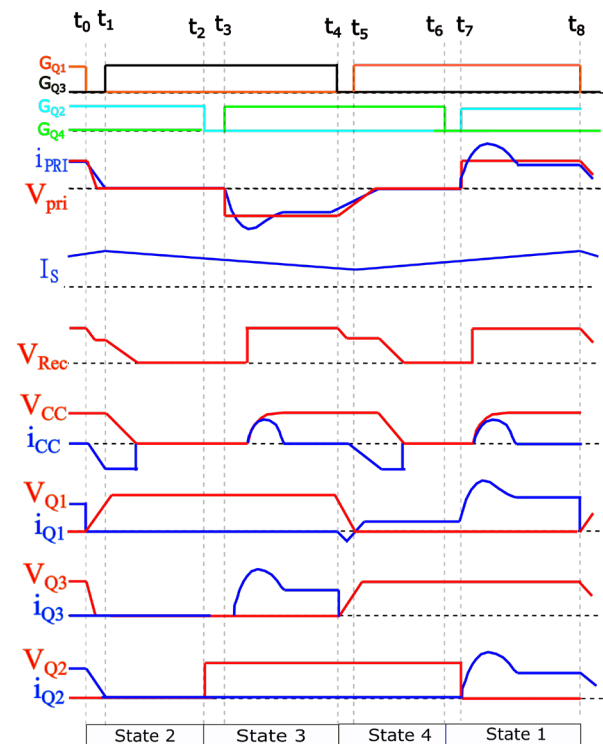


Figure 2 Operational waveforms of proposed converter

The converter uses a full-bridge of four semiconductor switches ($Q_1 \sim Q_4$) with integral body diodes ($D_1 \sim D_4$) and snubber capacitors ($C_1 \sim C_4$), which includes the drain-source parasitic capacitances of the corresponding switches. The link inductor (L_S), connected between the junction of two input ports and the junction of left leg switches (Q_1, Q_3), facilitates bidirectional energy transfer between the SPV source and the battery port. The secondary

diode bridge rectifier ($D_5 \sim D_8$) is followed by an auxiliary circuit (D_9, D_{10}, C_c) and a L_o - C_o filter.

Soft-switching is a technology adopted in high-frequency power electronic converters to reduce energy losses and electromagnetic interference (EMI) linked to conventional hard-switching techniques. It accomplishes this by modulating the switching transients to ensure that semiconductor devices, such as MOSFETs or IGBTs, operate at either zero voltage (ZVS) or zero current (ZCS). By removing the concurrent overlap of high voltage and high current during transitions, soft-switching markedly improves the converter's overall efficiency and enables dependable operation at substantially elevated switching frequencies.

The converter operation is explained from the initial condition that, the diagonal switches Q_1 and Q_2 are in conduction impressing the DC bus voltage ($V_{PV} + V_{BAT}$) across the transformer primary and the rectified secondary voltage (V_{Rec}) feeds the load. The link inductor now gets energized from V_{PV} through Q_1 . The clamping capacitor is charged to the initial voltage V_{CC} and with the converter operation is initiated with the turn-off of switch Q_1 . The operational waveforms of the converter are depicted in Figure 2.

As Q_1 turns off, C_1 charges and C_3 discharges by the transformer primary current (i_{PRI}) and the link inductor current (I_s). This causes a linear decrease in transformer primary and secondary rectified voltage, until D_{10} starts conduction. Thus, C_1 turns off under ZVS. As C_3 is completely discharged, i_{PRI} and I_s find conduction path through D_3 . The switch (Q_3) is now turned on under ZV-ZCS condition. With the conduction of D_{10} , the primary and secondary currents rapidly drop as a result of the reflected clamped capacitor voltage being impressed across the Transformer primary winding. As both of the transformer winding currents decrease to zero, Q_2 turns off under ZCS condition and the rectifier diodes (D_5 and D_8) recover softly. However, C_c continues to deliver the load power through D_{10} and the battery gets energized by the stored energy of the link inductor (L_s). As Q_4 is turned on after a dead time, the DC bus voltage ($V_{PV} + V_{BAT}$) is applied across the leakage inductor (L_{lk}) and the primary winding current (i_{PRI}) increases linearly from zero in the opposite direction. Thus, Q_4 starts conduction with zero current. As the primary winding current reaches to the link inductor current (I_s), D_3 commutates softly and the excess current ($i_{PRI} - I_s$), conducted through Q_3 starts increasing from zero. The rectified voltage (V_{Rec}) is now $n(V_{PV} + V_{BAT})$ and accordingly the clamping capacitor (C_c) in resonance with the reflected leakage inductance ($n^2 L_{lk}$) gets charged to $V_{CCO} = 2 \{n(V_{PV} + V_{BAT}) - V_o\}$. As Q_3 is turned off, C_3 charges and C_1 discharges by the primary current. Consequently, C_3 turns off under ZVS, and the subsequent half cycle is operated in the same manner.

3.0 PROPOSED SPV SYSTEM AND INTERPORT POWER SHARING

The proposed partially isolated TPC along with the centralized controller is shown in Figure 3. It is built on a PSFB structure with the SPV source and the battery bank connected at the input ports and the load port is magnetically isolated from the input ports by a high-frequency transformer. A centralized controller on sensing the voltage and current signals of the input ports and

the voltage signal of the load port generates requisite gate pulses for the switches to enable MPPT operation of SPV source, load voltage regulation, and charge/discharge control of the BESS.

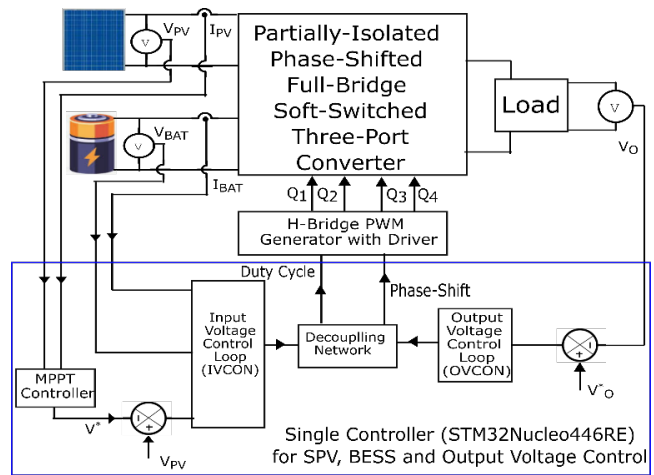


Figure 3 Partially isolated TPC and control scheme of proposed SPV system

The control operations are accomplished through two separate control loops: Input Voltage Control (IVCON) for deciding the gate pulse duty ratio (D) and the Output Voltage Control (OVCON) for adjusting the phase-shift (ϕ) between the leading and lagging leg switches. A detailed discussion on the controller working principle is presented in section 4.

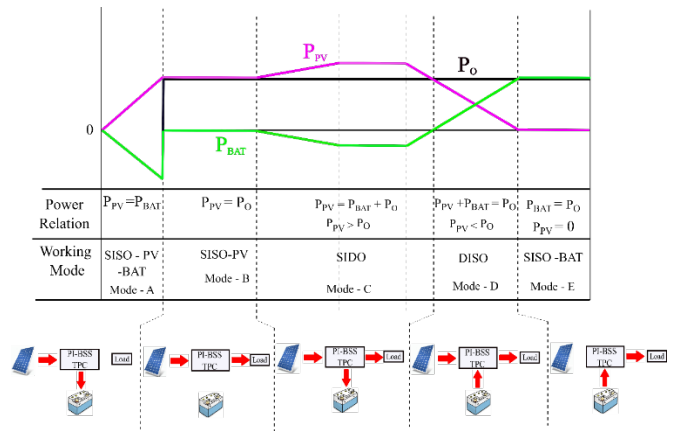


Figure 4 Inter-port power sharing strategies of proposed SPV system

The inter-port power sharing strategies for various combinations of SPV power, load power and BESS, as graphically represented in Figure 4, can be accomplished in five different modes: Mode A (SPV to BESS), Mode B (SPV to Load), Mode C (SPV to Load and BESS), Mode D (SPV and BESS to Load) and Mode E (BESS to Load). Only in mode A, the converter works with a fixed phase-shift (ϕ) between the switching gate pulses and for all other modes, the OVCON controller suitably adjusts the phase-shift (ϕ) for power sharing control.

Mode A (PV-to-Bat power transfer): Without any load power demand, if the SPV power generation goes on increasing, the entire power is utilized by the converter to charge the

batteries, i.e. $P_{PV} = P_{BAT}$. In this mode, the converter operates with MPPT control, with variable duty cycle (D) and fixed phase shift (ϕ), until the state of charge (SOC) of the battery is not reached to its maximum limit.

Mode B (PV-to-Load power transfer): If the load is switched on and the battery is fully charged or in disconnected condition, then with a fixed SPV power generation the converter operates in this mode feeding entire SPV power to the load, i.e. $P_{PV} = P_O$. In this mode, the converter operates with MPPT control, if the load can draw the entire SPV power. If the load power demand goes below the peak SPV power, then the converter control switches over to load voltage regulation mode.

Mode C (PV-to-Load & Bat power transfer): If the battery is not fully charged and the SPV power is more than the load power demand, then the converter operates in this mode feeding the excess SPV power to the battery, i.e. $P_{PV} = P_{BAT} + P_O$. In this mode, the converter operates with MPPT control and load voltage control, as well. Here, with constant SPV power generation the battery charges up at a fixed rate and when the SPV generation starts reducing, the battery charging rate also reduces accordingly.

Mode D (PV & Bat-to-Load power transfer): This mode is activated, when the SPV generation reduces below the load power demand and the deficit is met by discharging the battery storage i.e. $P_{PV} + P_{BAT} = P_O$. Here also, both the MPPT control of SPV source and load voltage control are activated simultaneously.

Mode E (Bat-to-Load power transfer): This mode is activated, when the SPV generation is completely absent and the entire load power is supplied by the battery storage, i.e. $P_O = P_{BAT}$. Here, the converter operates with load voltage regulation mode.

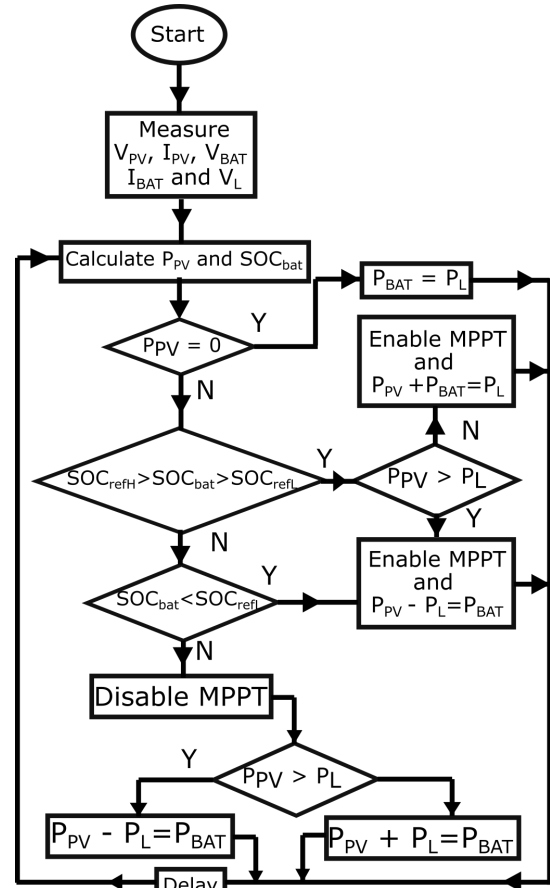


Figure 5 Flow diagram of the proposed control algorithm

4.0 CONTROL SCHEME OF PROPOSED TPC

The proposed TPC uses a centralized controller for inter-port power sharing among the SPV source, battery port and load towards achieving MPPT control of SPV source, load voltage regulation, and charge/discharge control of the BESS. The schematic control blocks are shown in Figure 3 and the power control flowchart is shown in Figure 5. The automatic power balance among the three ports is controlled by the gate pulse duty ratio (D) and the load voltage is controlled by the gate pulse duty ratio (D) and the phase shift (ϕ) between leading and lagging leg gate pulses both. Using the incremental conductance (IC) technique, the MPPT controller determines the reference voltage signal (V^*) that correlates to the maximum power point (MPP) of the SPV source by detecting the SPV voltage (V_{PV}) and SPV current (I_{PV}). The error signal of V^* and V_{PV} along with the battery voltage and current signals (V_{BAT} and I_{BAT}) are fed to the Input Voltage Control (IVCON) loop to calculate the requisite switching duty ratio (D) for the proposed TPC. Based on the error signal of the desired output voltage (V_o^*) to the actual output voltage (V_o), the PI control based output voltage control loop (OVCON) determines the requisite phase-shift value (ϕ) between the gate pulses of the leading leg and lagging leg switches of the PSFB converter.

5.0 DESIGN CONSIDERATION AND ANALYSIS

This section elaborates important design guidelines of the PSFB converter.

5.1 Isolation Transformer

The transformer turns-ratio (n) is determined following the conventional approach as below [39].

$$n = \frac{N_2}{N_1} = \frac{V_o + 2V_F}{2 \cdot k \cdot D \cdot (V_{PV} + V_{BAT} - 2V_F)} \quad (1)$$

Considering the maximum and minimum duty ratio (D) corresponding to the minimum and maximum SPV voltage (100V and 140V) as 0.45 and 0.35 respectively, the transformer turns-ratio (n) is fixed to 0.85.

5.2 Link Inductor

The link inductor (L_s), in association with the leading leg switches (Q_1 and Q_3) and the body diodes, functions as a bidirectional buck-boost converter between the SPV source (V_{PV}) and the battery storage (V_{BAT}). Thus, L_s is selected using the following relationship.

$$L_s = \frac{V_{PV} \cdot D_{max}}{\Delta I_{LS} \cdot f_s} \quad (2)$$

Here, a 650 μH inductor is selected for L_s , such that the buck-boost converter works just above the boundary conduction mode.

5.3 Switching Devices

The leading leg switches (Q_1 and Q_3) of the proposed TPC are operated under ZVS conditions, like conventional PSFB converters and hence realized with MOSFETs for the reasons described in [40]. However, the auxiliary network of the proposed TPC forces the lagging leg switches (Q_2 and Q_4) to change their switching states under ZCS conditions. IGBT switches, having comparatively smaller body capacitances than MOSFETs, are therefore more suitable for such applications [40].

5.4 Analysis of Duty Cycle and Circulating Current Loss Estimation

The leading leg and trailing leg switches of conventional PSFB converter are both operated under ZVS conditions. However, ZVS transition of the trailing leg switches over wide load range requires a large leakage inductor, which is managed by connecting an external inductor in series with the transformer primary. This causes a slow rise of transformer secondary voltage and accordingly a considerable duty cycle loss, as depicted in Figure 6(a). The passive mode circulating current also causes large ohmic loss in the transformer windings and the semiconductor devices.

The auxiliary network used in the proposed converter impresses the clamping capacitor voltage in opposition to the transformer primary current, thereby quickly diminishing the passive mode circulating current, as shown in Figure 6(b). This enables ZCS transition of the lagging leg switches over the entire load range. In the absence of any additional series inductor, the proposed PSFB converter has wider duty cycle range and simultaneously the passive mode circulating current conduction loss is avoided.

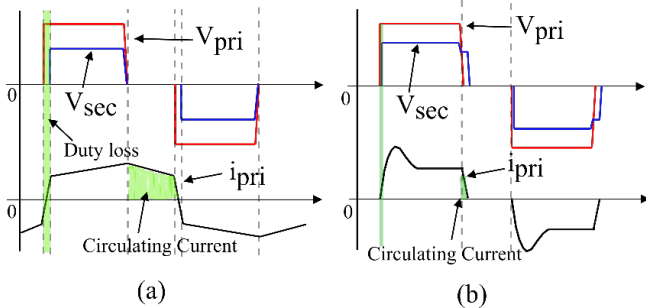


Figure 6 Duty cycle loss and circulating current comparative waveform (a) Conventional PSFB Converter (b) Proposed PSFB Converter

6.0 STABILITY ANALYSIS AND DESIGN OF CONTROLLER

The small-signal model of the proposed TPC is derived from the equivalent circuit shown in Figure 7. Here, V_1' and V_2' represents the internal voltages of the SPV source and BESS respectively, while their internal resistances are represented by R_1 and R_2 respectively. C_{S1} and C_{S2} are the bus capacitors.

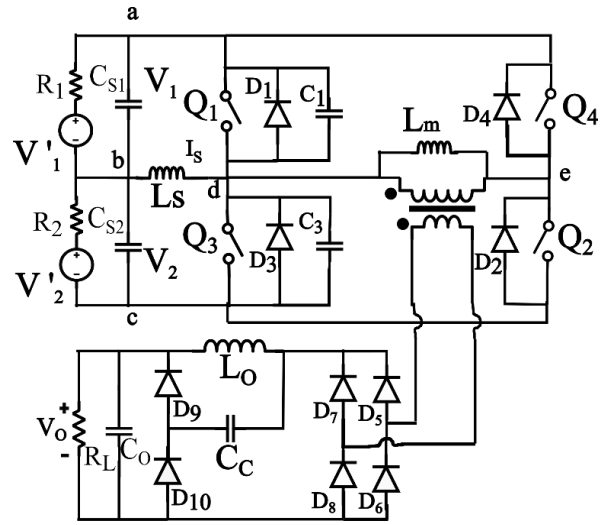


Figure 7 Equivalent circuit of TPC

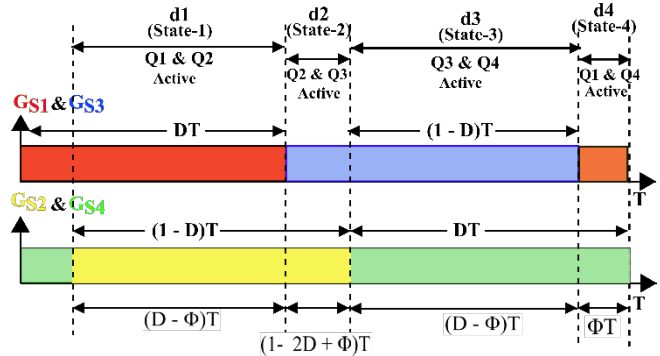


Figure 8 Duration of the control pulse

In this analysis, the dead time between the complementary gate signals are neglected for being very small in comparison to the switching time period. With this assumption, the switching cycle is divided in four states of duration ($d_1 \sim d_4$) as shown in Figure 8. Here, D is the switching duty ratio of Q_1 and ϕ is the phase shift between the gate pulses of Q_1 and Q_2 . From Figure 8, the duration matrix of the four states are obtained as below.

$$D = [(D-\phi) (1-2D+\phi) (D-\phi) (\phi)] \quad (3)$$

The six state variables considered for average modeling are given as below.

$$x = [v_1, v_2, i_{Ls}, i_{Lm}, i_{Lo}, v_0] \quad (4)$$

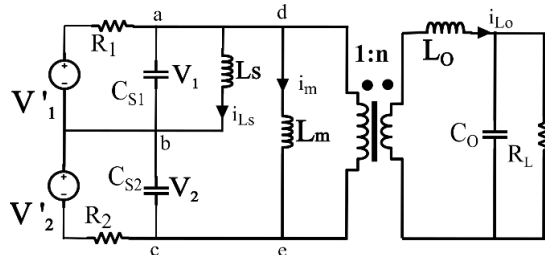


Figure 9 Equivalent circuit in state 1

State 1 (Q1 and Q2 activated): The state-space equation corresponding to Figure 9 is represented by equation (5).

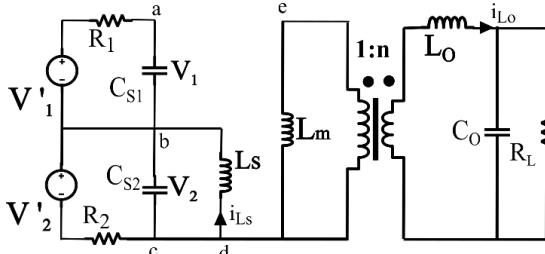


Figure 10 Equivalent circuit in state 2

State 2 (Q2 and Q3 activated): The state-space equation corresponding to Figure 10 is represented by equation (6).

$$\begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{LS} \\ \dot{i}_{LM} \\ \dot{i}_{LO} \\ \dot{v}_o \end{pmatrix} = \begin{bmatrix} -1/C_{S1}R_1 & 0 & -1/C_{S1} & -1/C_{S1} & -1/nC_{S1} & 0 \\ 0 & -1/C_{S2}R_2 & 0 & -1/C_{S2} & -1/nC_{S2} & 0 \\ 1/L_S & 0 & 0 & 0 & 0 & 0 \\ 1/L_m & 1/L_m & 0 & 0 & 0 & 0 \\ 1/nL_o & 1/nL_o & 0 & 0 & 0 & -1/L_o \\ 0 & 0 & 0 & 0 & 1/C_o & -1/C_oR_o \end{bmatrix} \begin{pmatrix} v_1 \\ v_2 \\ i_{LS} \\ i_{LM} \\ i_{LO} \\ v_o \end{pmatrix} + \begin{pmatrix} 1/C_{S1}R_1 & 0 \\ 0 & 1/C_{S2}R_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} v_1' \\ v_2' \end{pmatrix} \quad (5)$$

$$\begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{LS} \\ \dot{i}_{LM} \\ \dot{i}_{LO} \\ \dot{v}_o \end{pmatrix} = \begin{bmatrix} -1/C_{S1}R_1 & 0 & -1/C_{S1} & 0 & 0 & 0 \\ 0 & -1/C_{S2}R_2 & 1/C_{S2} & 0 & 0 & 0 \\ 1/L_S & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/L_o & 0 \\ 0 & 0 & 0 & 0 & 1/C_o & -1/C_oR_o \end{bmatrix} \begin{pmatrix} v_1 \\ v_2 \\ i_{LS} \\ i_{LM} \\ i_{LO} \\ v_o \end{pmatrix} + \begin{pmatrix} 1/C_{S1}R_1 & 0 \\ 0 & 1/C_{S2}R_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} v_1' \\ v_2' \end{pmatrix} \quad (6)$$

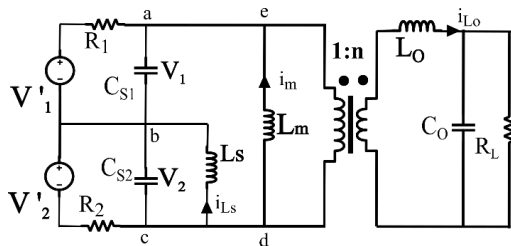


Figure 11 Equivalent circuit at state 3

State 3 (Q3 and Q4 activated): The state-space equation corresponding to Figure 11 is represented by equation (7).

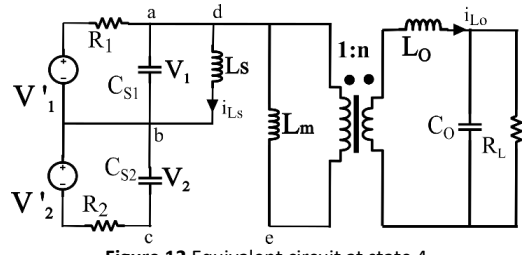


Figure 12 Equivalent circuit at state 4

State 4 (Q4 and Q1 activated): The state-space equation corresponding to Figure 12 is represented by equation (8).

$$\begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{LS} \\ \dot{i}_{LM} \\ \dot{i}_{LO} \\ \dot{v}_o \end{pmatrix} = \begin{bmatrix} -1/C_{S1}R_1 & 0 & 0 & 1/C_{S1} & 1/nC_{S1} & 0 \\ 0 & -1/C_{S2}R_2 & 1/C_{S2} & 1/C_{S2} & 1/nC_{S2} & 0 \\ 0 & 1/L_S & 0 & 0 & 0 & 0 \\ -1/L_m & -1/L_m & 0 & 0 & 0 & 0 \\ 1/nL_o & 1/nL_o & 0 & 0 & 0 & -1/L_o \\ 0 & 0 & 0 & 0 & 1/C_o & -1/C_oR_o \end{bmatrix} \begin{pmatrix} v_1 \\ v_2 \\ i_{LS} \\ i_{LM} \\ i_{LO} \\ v_o \end{pmatrix} + \begin{pmatrix} 1/C_{S1}R_1 & 0 \\ 0 & 1/C_{S2}R_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} v_1' \\ v_2' \end{pmatrix} \quad (7)$$

$$\begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{LS} \\ \dot{i}_{LM} \\ \dot{i}_{LO} \\ \dot{v}_o \end{pmatrix} = \begin{bmatrix} -1/C_{S1}R_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1/C_{S2}R_2 & 1/C_{S2} & 0 & 0 & 0 \\ 0 & -1/L_S & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/L_o & 0 \\ 0 & 0 & 0 & 0 & 1/C_o & -1/C_oR_o \end{bmatrix} \begin{pmatrix} v_1 \\ v_2 \\ i_{LS} \\ i_{LM} \\ i_{LO} \\ v_o \end{pmatrix} + \begin{pmatrix} 1/C_{S1}R_1 & 0 \\ 0 & 1/C_{S2}R_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} v_1' \\ v_2' \end{pmatrix} \quad (8)$$

Finally, the average model of A matrix is calculated by using $A = (A_1 \cdot d_1) + (A_2 \cdot d_2) + (A_3 \cdot d_3) + (A_4 \cdot d_4)$ [9]

So the nonlinear equation becomes

$$\dot{x} = [A_1d_1 + A_2d_2 + A_3d_3 + A_4d_4] x(t) + [B_1d_1 + B_2d_2 + B_3d_3 + B_4d_4] u(t) \quad (10)$$

After replacing the value of the state matrix the final expression can be represented as equation (11).

$$\begin{pmatrix} \dot{v}_1 \\ \dot{v}_2 \\ \dot{i}_{LS} \\ \dot{i}_{LM} \\ \dot{i}_{LO} \\ \dot{v}_o \end{pmatrix} = \begin{bmatrix} -1/C_{S1}R_1 & 0 & (d-1)/C_{S1} & 0 & 0 & 0 \\ 0 & -1/C_{S2}R_2 & d/C_{S2} & 0 & 0 & 0 \\ -(d-1)/L_S & -d/L_S & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 2(d-\phi)/nL_o & 2(d-\phi)/nL_o & 0 & 0 & -1/L_o & 0 \\ 0 & 0 & 0 & 0 & 1/C_o & -1/C_oR_o \end{bmatrix} \begin{pmatrix} v_1 \\ v_2 \\ i_{LS} \\ i_{LM} \\ i_{LO} \\ v_o \end{pmatrix} + \begin{pmatrix} 1/C_{S1}R_1 & 0 \\ 0 & 1/C_{S2}R_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} v_1' \\ v_2' \end{pmatrix} \quad (11)$$

Finally, the numerical expressions of the transfer functions, TF1(s) and TF2(s) are obtained from the converter specifications and major components detailed in Table 1.

Table 1 Specification of proposed PI-TPC prototype

Component	Detail specifications
Source 1 (SPV Source)	$V_{OC} = 145 \text{ V}$, $V_{MP} = 100 \text{ V} - 110 \text{ V}$ $I_{MP} = 1.5 \text{ A}$, $I_{SC} = 1.6 \text{ A}$, $P_{MP} = 165 \text{ W}$
Source 2 (Battery bank)	$V_{BAT} = 48 \text{ V}$
Rated output	$V_o = 48 \text{ V}$, $I_o = 3 \text{ A}$

Switching frequency	$f_s = 100 \text{ kHz}$
Active Switch	Q ₁ and Q ₃ : STF26N60N (600 V, 20 A) Q ₂ and Q ₄ : IRG4PC50UD (600 V, 27 A)
Power Diode	D ₅ –D ₁₀ : MUR1560 (600 V, 15 A)
Transformer	Turn ratio (n) = 0.85, Leakage Inductance = 2.2 μH, Magnetizing Inductance = 13.6
Capacitors	C _{CC} = 2.2 nF, C ₁ = C ₃ = 1 nF, C ₀ = 3.3 μF
Inductors	L _s = 650 μH, L _o = 223.4 μH.

$$TF1(s) = \frac{V_1(s)}{D(s)} = \frac{9.176e^4 s^2 + 1.151e^{10} s + 6.063e^{13}}{s^3 + 1.207e^5 s^2 + 8.372e^7 s + 5.719e^{11}} \quad (12)$$

$$TF2(s) = \frac{V_o(s)}{\phi(s)} = \frac{-7.288e^8}{s^2 + 434 s + 1e^7} \quad (13)$$

Here, TF1(s) and TF2(s) represent the input voltage loop and output voltage loop transfer functions respectively.

A complex conjugate pole pair at $-3.39 \pm 1.49e^{03}i$ on the pole-zero mapping along with the undesirable response of 4234 rad/s gain crossover frequency (GCF) and 146° phase margin (PM) is observed on the bode plot of TF1(s) (Figure 14). Similarly, a pair of complex poles at $-2.17 \pm 3.15e^{03}i$ on the pole-zero mapping along with the gain crossover frequency of 9234 rad/s and 176° phase margin is depicted on the bode plot of TF2(s) (Figure 15). The above observations demand for appropriate controllers. As the output parameters are dependent on multiple control variables, a decoupling network is used to make each state independent of each other [41]. The transfer function G(s) and the decoupling network (D_c) are described in equations 14 and 15 respectively and the block diagram of the multivariable system is described in Figure 13.

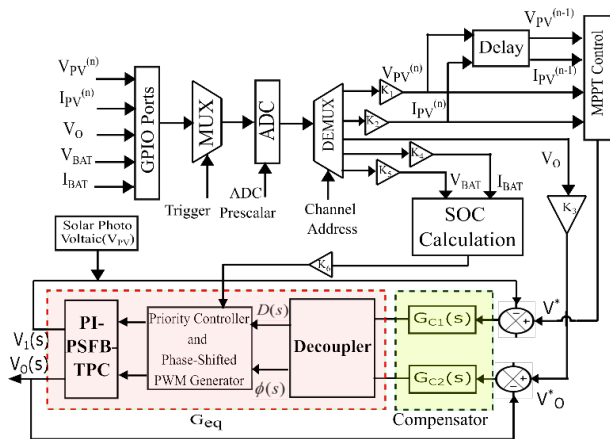


Figure 13 Multivariable system signal flow

$$G(s) = \begin{bmatrix} g_{11}(s) & g_{12}(s) \\ g_{21}(s) & g_{22}(s) \end{bmatrix} = \begin{bmatrix} \frac{V_1(s)}{D(s)} & \frac{V_1(s)}{\phi(s)} \\ \frac{V_o(s)}{D(s)} & \frac{V_o(s)}{\phi(s)} \end{bmatrix} \quad (14)$$

$$D_c = \begin{bmatrix} \frac{-g_{22}(s)}{g_{21}(s)} & 0 \\ \frac{-g_{11}(s)}{g_{21}(s)} & \frac{-g_{11}(s)}{g_{12}(s)} \end{bmatrix} \quad (15)$$

$$G_{eq} = G * D = \begin{bmatrix} g_{11}(s) & g_{12}(s) \\ g_{21}(s) & g_{22}(s) \end{bmatrix} * \begin{bmatrix} \frac{-g_{22}(s)}{g_{21}(s)} & 0 \\ \frac{-g_{11}(s)}{g_{21}(s)} & \frac{-g_{11}(s)}{g_{12}(s)} \end{bmatrix} \quad (16)$$

$$G_{eq} = \begin{bmatrix} \frac{-g_{11}(s)}{g_{21}(s)} [g_{22}(s) + g_{12}(s)] & -g_{11}(s) \\ g_{22}(s) & \frac{-g_{11}(s)}{g_{12}(s)} [g_{21}(s) + g_{22}(s)] \end{bmatrix} \quad (17)$$

Further, the decoupled system transfer function has been calculated in equations 16 and 17 respectively. The decoupling terms, $g_{12}(s)$ and $g_{21}(s)$ show the plant's multi-variability. As shown in Figure 13, two different compensators, $G_{c1}(s)$ and $G_{c2}(s)$ have been introduced for compensating the steady-state error and the phase margin. Additionally, the pole-zero cancellation technique is used to choose the corresponding compensator parameters to maintain the necessary phase margin. The value of the $G_{c1}(s)$ and $G_{c2}(s)$ are calculated as shown in equations 18 and 19.

$$G_{c1}(s) = \frac{0.001 s^2 + 0.0012 s + 0.704}{s} \quad (18)$$

$$G_{c2}(s) = \frac{0.000348 s^2 + 0.022 s + 1.863}{s} \quad (19)$$

Stability is correlated with both the phase margin and the gain margin; the larger the value of either of these, the more stable the system is and the less likely it is to oscillate. The response is correlated with crossover frequency: the higher the crossover frequency, the more responsive it is and the more efficiently load transient-induced output variations may be dampened. After adding the type-1 compensation, the system stability is increased as depicted in the bode plot, shown in Figure 14 and Figure 15. Higher Gain Crossover Frequency (GCF) is achieved after adding a compensator, which implies stability enhancement. From the pole zero plot analysis it's also found that the shifting of pole from imaginary axis towards the left hand of the complex plane after implementing the compensation.

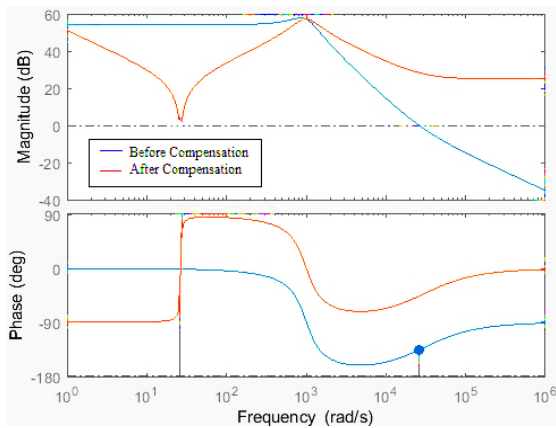


Figure 14 Bode plot of $V_1(s)/D(s)$ before and after $G_{C1}(s)$ compensation

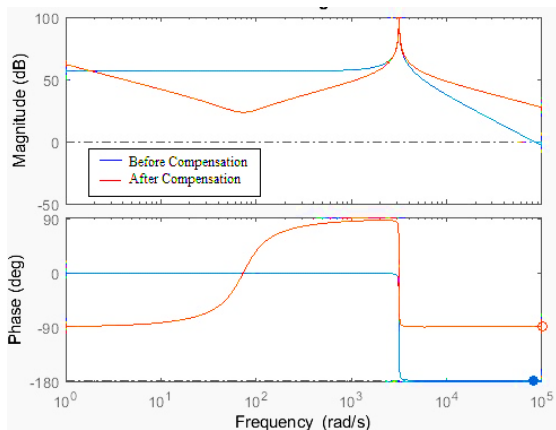


Figure 15 Bode plot of $V_o(s)/\phi(s)$ before and after $G_{C2}(s)$ compensation

7.0 LABORATORY TESTING AND EXPERIMENTAL RESULTS

A 144W, 100-kHz hardware prototype of the proposed PI-TPC has been designed and developed to corroborate the theoretical analysis with converter's real-time performance. The specifications and major components of the TPC are detailed in Table 1. The PSFB structure of the TPC uses MOSFETs (STF26N60N) for the leading leg switches and IGBTs (IRG4PC50UD) for the lagging leg switches. Ultrafast diodes (RHRP1560) are selected for the secondary side rectifiers and auxiliary clamping circuit. The isolation transformer is built on Cosmo ferrite core (EE4215) with 13 and 10 number of primary and secondary turns. The leakage inductance of the transformer is measured with an approximate value of $2.2\mu\text{H}$. Similarly, the $223\mu\text{H}$ output inductor is also developed on EE4014 Cosmo ferrite core. The hall-effect transducers' LEM LV25-P and LEM LA25-P are used to measure BESS port voltage, current, and the load port current whereas the SPV voltage and current are directly sensed from SPV solar simulator. The measuring resistances for the LEM LV25-P and LEM LA25-P are selected as 250Ω and 220Ω respectively. The control circuitry used ARM

based STM32NucleoF446RE microcontroller to generate the 100 kHz phase shifted PWM signals with 500ns dead time between the complementary gate pulses. The ADC ports of the controller are configured to 12-bit resolution for better interfacing. Dual channel half-bridge gate drivers (UCC21520) of Texas Instruments with less than 5 ns propagation delay are used to drive the active power switches of the TPC. The experimental setup is shown in Figure 16. In the experimental setup, solar emulator (ITECH IT6514C) and battery simulator (ITECH IT6433) have been used as SPV source and BESS respectively. Besides, a dc single channel electronic load (ITECH IT8512B) is used as D.C. load. Important voltage and current waveforms at different operating conditions are recorded by digital storage oscilloscope of Agilent Technologies (Infinii Vision DSO-X-4024A).

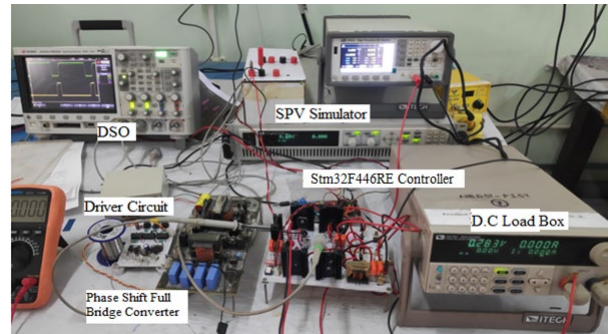


Figure 16 Experimental Setup

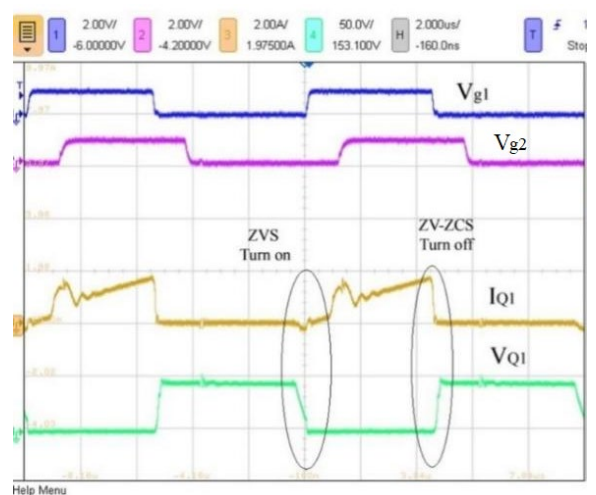


Figure 17 Leading leg switch (Q_1) Zero Voltage Switching Operation: Experimental waveforms of V_{g1} and V_{g2} : gate pulses for switch Q_1 and Q_2 (scale: 20V/div), current through switch Q_1 : I_{q1} (scale: 5 A/div) and voltage across switch Q_1 : V_{q1} (scale: 150V/div)

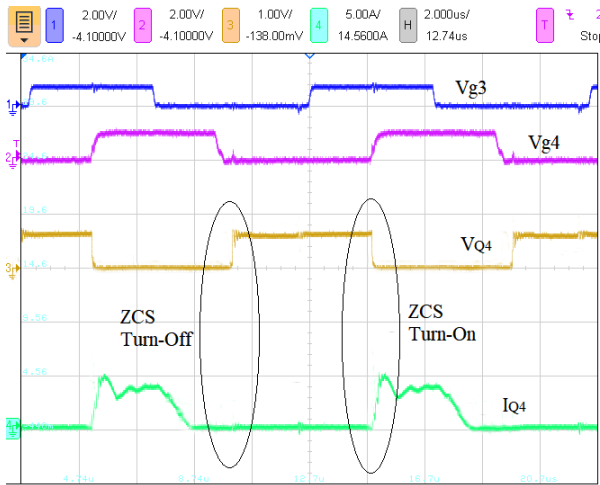


Figure 18 Lagging leg switch (Q_4) Zero Current Switching Operation: Experimental waveforms of V_{g3} and V_{g4} : gate pulses for switch Q_3 and Q_4 (scale: 20V/div), voltage across switch Q_4 : V_{Q4} (scale: 150V/div) and current through switch Q_4 : I_{Q4} (scale: 5 A/div)

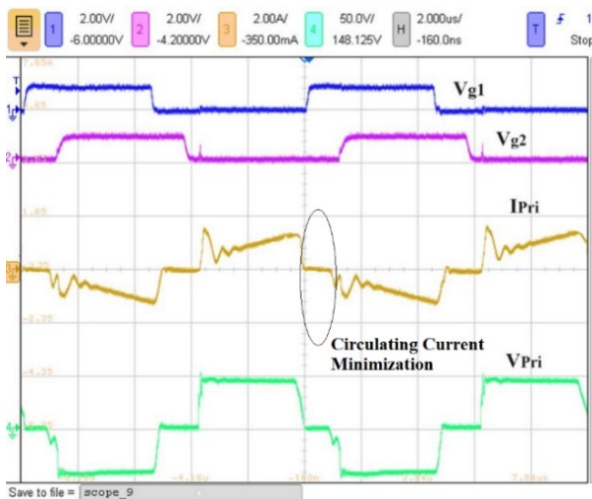


Figure 19 Minimization of transformer primary circulating current: Experimental waveforms of V_{g1} and V_{g2} : gate pulses for switch Q_1 and Q_2 (scale: 20V/div), current through transformer primary winding: I_{Pri} (scale: 5 A/div) and voltage across transformer primary winding: V_{Pri} (scale: 100V/div)

The dynamic and steady-state performance of the prototype TPC has been evaluated under varying solar irradiance and load conditions to validate the converter's behavior. Important findings are presented in this section. Figure 17 displays the voltage and current waveforms of the leading leg switch (Q_1) along with the gate pulses of Q_1 and Q_2 . It is observed that Q_1 turns on under ZVS and turns off under ZV-ZCS condition. Similarly, the voltage and current waveforms of the lagging leg switch (Q_4) along with the switching gate pulses of Q_3 and Q_4 are shown in Figure 18. It demonstrates that, the turn-on current of Q_4 rises gradually from zero and prior to withdrawal of switching gate pulse it is reset to zero, thereby establishing ZCS turn-on and turn-off of the switch. The transformer current resetting establishing circulating current minimization in the passive mode is captured in Figure 19.

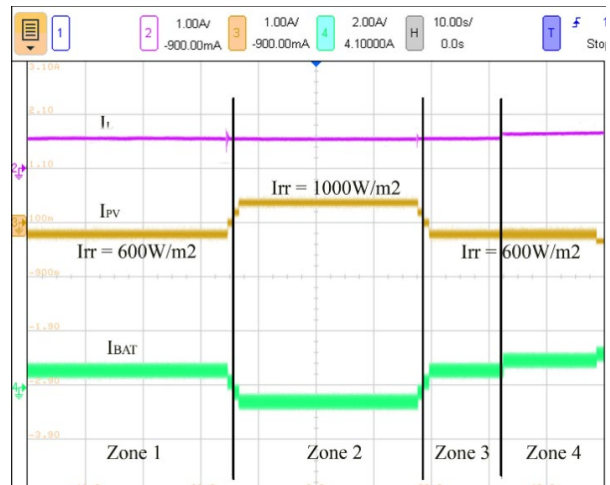


Figure 20 Experimental waveforms of PI-TPC for mode C (Zone 2) and mode D (Zone 1, 3, and 4), load current (scale: 5A/div), solar PV panel output current (scale: 5A/div), battery output current (scale: 2.5A/div)

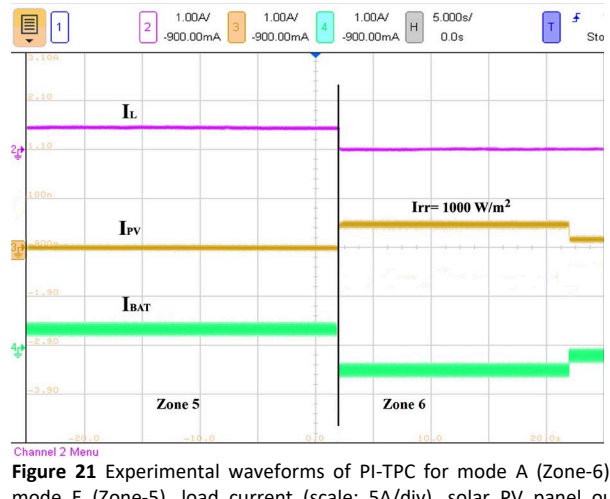


Figure 21 Experimental waveforms of PI-TPC for mode A (Zone-6) and mode E (Zone-5), load current (scale: 5A/div), solar PV panel output current (scale: 2.5A/div), battery output current (scale: 5A/div)

The effectiveness of the controller in inter-port power sharing has been thoroughly investigated at different combinations of solar power, load power and battery charging/ discharging control. The various combinations of SPV, load and battery power, as measured at the three ports of the TPC, are presented in 4 different zones, shown in Figure 20. In zone 1, the 81.6W (109V, 0.74A) SPV power generation at a solar irradiance of 600W/m² is not sufficient to meet the 132W (48V and 2.75A) load demand. Hence, the TPC draws the 45.8W deficit load power from the battery port (47.8V and 0.96A). As the solar irradiance is increased to 1000W/m², the SPV power increases to 165W (110V and 1.5A). Now, the SPV power being more than the load power, the excess SPV power (28W) is sent to the BESS and thus, the battery switches over from discharging to the charging mode. This event is depicted in zone 2. In mode 3, the solar irradiance again reduces to 600W/m² with the same load condition. Thus, mode 3 operation is identical to mode 1. In zone 4, solar irradiance is maintained same, but the load demand is increased to 144W. Now the TPC draws the 14W deficit load power from the BESS and hence the battery discharge current changes to 1.42A. Figure 21 represents the inter-port power

sharing in zone 5. Here, in absence of any SPV power, the entire load power 96W (48V, 2A) is exclusively supplied by the battery (47.53V and 2A). The converter operation can be continued in mode E, till the battery SOC reaches the minimum permissible limit, after which the converter switches over to idle mode. In zone 6, the entire SPV generated power 162W (110V, 1.47A) is utilized to charge the battery, as there is no load power demand.

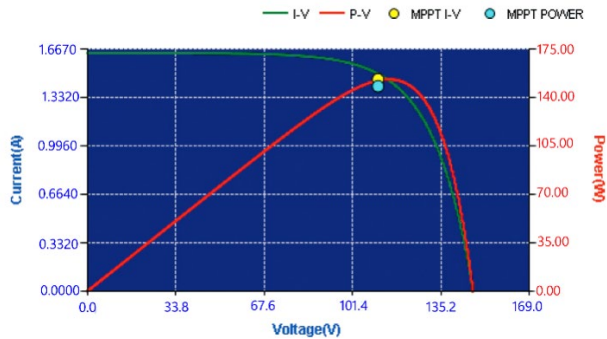


Figure 22 I-V and P-V plot of SPV source

The performance behavior of the controller in extraction of maximum power from the SPV source has also been validated by capturing the instantaneous I-V and P-V plot from the SPV emulator. The sample result shown in Figure 22 establishes 96.6% MPPT efficiency, while extracting 153.4W SPV power.

8.0 COMPARISON WITH OTHER CONVERTER

A brief comparison of the proposed topology with other TPCs is demonstrated in Table 3. Two different structures of non-isolated TPCs [42], [43], fully isolated TPCs [13], [18] and partially isolated TPCs [22], [36] along with the proposed TPC have been considered in this analysis. Amongst them, the non-isolated converter presented in [43] has the least component count, but it suffers from the problems associated with hard-switched converter operation and poor efficiency. The converter presented in [42] operates under fully soft-switched condition, but does not fulfill the mandatory requirement of load port isolation. Both the fully isolated converters [13], [18] are operated under fully soft-switched conditions. However, use of many magnetic elements and capacitors makes the power circuit heavy and bulky. In this respect, the partially isolated converters [22], [36] and the proposed TPC has comparatively less count of magnetic and filter components. However, the converters [22], [36] are operated under partial soft-switched conditions, whereas the proposed TPC enjoys the benefits of fully soft-switched converter operation over wide load range.

Table 3 Comparison with other similar converter topologies

Reference TPCs		[42]	[43]	[18]	[13]	[22]	[36]	Proposed TPC
Electric Isolation		Non-isolated	Non-isolated	Fully Isolated	Fully Isolated	Partially isolated	Partially isolated	Partially isolated
MPPT of SPV source		NA	Enabled	NA	NA	NA	Not Enabled	Enabled
Switching transition		Fully soft-switched	Hard-switched	Fully soft-switched	Fully soft-switched	Partial soft-switching	Partial soft-switching	Fully Soft-switched
Semiconductor device count	Active Switches	3	4	12	12	3	4	4
	Diodes	7	1	0	0	4	4	6
Passive Component count	Capacitor	8	4	5	5	5	1	3
	Transformer/Inductor	1	1	4	4	5	2	3
Efficiency		97.20%	85.2%	96.3%	-	93.20%	94%	95.20%

9.0 CONCLUSION

This study effectively introduced and substantiated a novel, partially isolated three-port DC-DC converter (TPC) topology, specifically designed for the efficient and integrated management of Solar Photovoltaic (SPV) energy and a Battery Energy Storage System (BESS). The suggested architecture offers substantial performance improvements compared to traditional multi-port converters. It offers galvanic isolation for the load port, enhancing overall system safety and operating flexibility. Efficiency is optimized by facilitating a smooth

transition of all semiconductor switches and a gentle recovery of power diodes, thus reducing related switching losses. A significant architectural accomplishment is the eradication of passive mode circulating current loss, a prevalent efficiency barrier in conventional phase-shift full bridge converters. Moreover, operational complexity is simplified by the adoption of a singular, integrated controller. This controller adeptly oversees three essential duties concurrently: executing Maximum Power Point Tracking (MPPT) for the solar photovoltaic source, accurately regulating the load voltage, and managing the intelligent charge and discharge processes of the

Battery Energy Storage System (BESS). The theoretical benefits and the thorough comparative analysis versus other TPCs were extensively tested by rigorous laboratory testing. The effective real-time operation of the developed 144W, 48V hardware prototype validates the converter's durability, high efficiency, and practical feasibility for renewable energy integration. Subsequent research will concentrate on enhancing the converter for elevated power grid-connected applications and using sophisticated model predictive control techniques to optimize battery longevity and system responsiveness in dynamic operating environments.

Acknowledgement

We would like to thank University of Calcutta for their helpful feedback and support.

Conflict of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper

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