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DIGITAL CONTROLLED OSCILLATOR (DCO) FOR ALL DIGITAL PHASE-LOCKED LOOP (ADPLL) – A REVIEW

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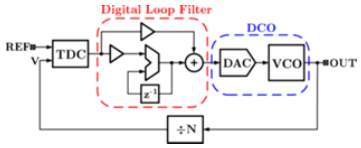
Graphical abstract



Abstract

Digital controlled oscillator (DCO) is becoming an attractive replacement over the voltage control oscillator (VCO) with the advances of digital intensive research on all-digital phase locked-loop (ADPLL) in complementary metal-oxide semiconductor (CMOS) process technology. This paper presents a review of various CMOS DCO schemes implemented in ADPLL and relationship between the DCO parameters with ADPLL performance. The DCO architecture evaluated through its power consumption, speed, chip area, frequency range, supply voltage, portability and resolution. It can be concluded that even though there are various schemes of DCO that have been implemented for ADPLL, the selection of the DCO is frequently based on the ADPLL applications and the complexity of the scheme. The demand for the low power dissipation and high resolution DCO in CMOS technology shall remain a challenging and active area of research for years to come. Thus, this review shall work as a guideline for the researchers who wish to work on all digital PLL.

Keywords: Digital controlled oscillator (DCO), all digital phase-locked loop (ADPLL), complementary metal-oxide semiconductor (CMOS), phase-locked loop, low power

Abstrak

Pengayun terkawal digital (DCO) semakin mendapat perhatian bagi menggantikan pengayun terkawal voltan dengan kemajuan penyelidikan intensif digital untuk gelung terkunci fasa semua digital (ADPLL) di dalam proses teknologi semikonduktor oksida-logam pelengkap (CMOS). Artikel ini membentangkan kajian pelbagai skema DCO CMOS yang digunakan di dalam ADPLL dan kaitan di antara parameter-parameter CMOS dengan prestasi ADPLL. Rekabentuk DCO dinilai melalui penyerapan kuasanya, kelajuan, keluasan cip, julat frekuensi, bekalan voltan, mudah alih dan resolusi. Permintaan terhadap DCO yang mempunyai lesapan kuasa yang rendah dan beresolusi tinggi di dalam teknologi CMOS akan terus memberi cabaran di dalam dunia penyelidikan untuk tempoh beberapa tahun akan datang. Oleh itu, kajian ini boleh digunakan sebagai panduan kepada penyelidik yang bakal bekerja di dalam PLL digital.

Kata kunci: Pengayun terkawal digital (DCO), gelung terkunci fasa digital (ADPLL), gelung terkunci fasa, semikonduktor oksida logam pelengkap, kuasa rendah

1.0 INTRODUCTION

The modern communication systems for clock and data recovery (CDR) or frequency synthesis are widely use phase-locked loops (PLLs) [1-5]. Electronic devices such as televisions, radio, cellular phones, computers and radio highly rely on PLL performances to operate efficiently. PLLs have been broadly studied due to massive range of applications. PLLs regularly developed on analog based design [6-8]. The main drawbacks of analog PLL are substrate-induced noise and the digital switch noise coupled with power through the power supply [9]. Moreover, the changes over CMOS process parameter required analog PLL to be redesign as it highly sensitive to parameter change [10-12]. Extensive studies have been done to improve the jitter performance however analog PLL outcome usually long lock-in time and increase design complexity. Therefore, ADPLL is used to replace the typical analog PLL for faster lock-in time, better stability, testability and portability over different process parameters.

Figure 1 shows ADPLL block diagram that consists of functional blocks including phase detector (TDC), low pass filter, digital to analog converter (DAC), voltage-controlled oscillator (VCO), and a multi-modulus divider [13-14]. A phase comparator or phase detector is a logic circuit, frequency mixer, or analog multiplier that generates voltage signal makes up the difference in phase between two signal inputs. A low pass filter is a filter that passes signal with a frequency lower than a certain cut-off frequency. It eliminates signals with frequencies higher than the cut-off frequency.

Digital controlled oscillator (DCO) plays an important role in ADPLL. DCO used in numerous applications including measuring temperature variations in oscillator frequency [15]. The DCO function similar with voltage-controlled oscillator (VCO) and DCO is used to overcome tuning stability limitations occur in the VCO [16]. DCO has identical delay stages, which each stage measures input delay or phase difference. The measurements usually form in a rough tuning block for larger frequency range. Better tuning block means the better is the time resolution [1], [16]. Variable delays are major pull back in typical DCO design that required large number of power and jitter optimization iterations to enhance the ADPLL performance.

Modern solutions employ a time to digital converter (TDC) [17] to measure the time difference between the edges of the oscillator and reference signal, thus obtaining the phase error. The phase error is then processed by a Control Algorithm. The typical control is a lowpass filter, called loop filter in the PLL terminology. A possible solution for the control is a digital accumulator (integration in the discrete domain), which integrates the frequency error signal, thus computing the control word for the DCO [18]. The design proposed in [19] is based on the ring topology and consists of four log-domain current-mode integrators. Using this implementation, the frequency can be tuned using the bias currents. The bias currents are obtained using a binary decoder and a current division network. The binary decoder role is to generate the control signals for the switches inside a current division cell. A 10-bit control word was used to generate 1024 control signals which in turn conducted to 1024 current values and 1024 distinct frequencies.

The paper will first discuss the basic concept of DCO in Section 2.0. Next, the various DCO schemes for ADPLL is presented in Section 3.0. Finally, Section 4.0 presents the performance comparison of the various DCO schemes followed by conclusion section.

2.0 BASIC CONCEPT OF DCO

A standard DCO design can be divided into two main techniques. The first uses fixed capacitance loading to change the driving strength dynamically while the second tune the capacitance loading by using shunt capacitance technique [20]. Both method results in reasonable frequency operating range and produce good linear frequency when power dissipation does not been taken into consideration. In a DCO design, there is trade-off between the maximum frequency and the operating range for a DCO can achieve. By adding more capacitance load will increase the operating range causes higher power consumption and a lower maximum frequency. Figure 2 shows basic DCO cell. A functional DCO produces an oscillation period of T_{DCO} [20]. With reference to the digital input word; d, T_{DCO} can be written as:

$$T_{DCO} = f(d_{n-1}2^{n-1} + d_{n-1}2^{n-2} + \cdots + d_1 2^1 + d_0 2^0) \quad (1)$$

DCO transfer equation can also derive T_{DCO} period of oscillation that linear proportional to d along with an offset. Thus, the oscillation period can be rewritten as:

$$T_{DCO} = T_{offset} - d.T_{step} \quad (2)$$

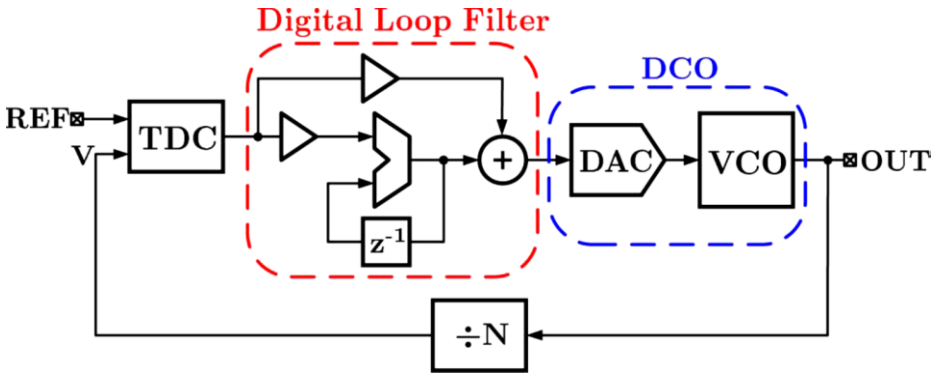


Figure 1 A conventional ADPLL block diagram [4]

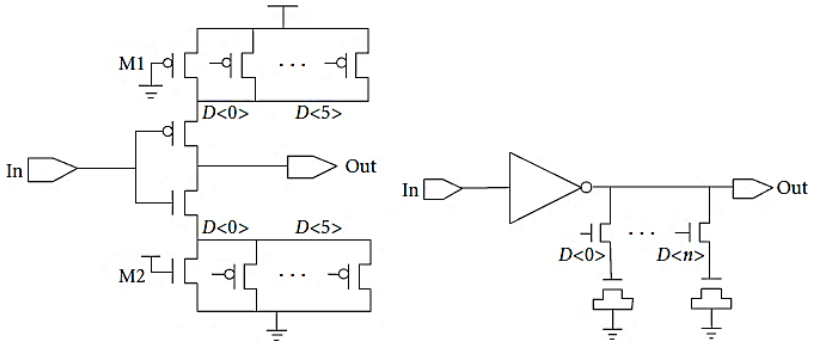


Figure 2 Drive strength control and shunt capacitance controlled standard cells used in DCO [20]

where d is digital control bits (DCB), T_{step} is the period of the quantization step, and T_{offset} is a constant offset period. Figure 2 show the conventional driving strength-controlled DCO. Calculating the constant delay of each cell is shown as follows:

$$T_{constant} = R_1(C_1 + C_2) + R_2C_2 \quad (3)$$

$$R_{1,2} \propto \frac{1}{W_{1,2}} \quad (4)$$

where W is width of transistor, C_1 and C_2 are the total capacitances at the drain M1 and M1' and R_1 and R_2 are the equivalent resistances of M1 and M1' respectively which mainly consist source to body and drain to body capacitances. Assume the driving strength is the same; this standard cell can obtain delay tuning range by using the equation as follow:

$$\frac{T_{tune}}{2} = R_1(C_1 + C_2)\frac{D.\Delta W}{W_1}, \left(\text{only if } \frac{D.\Delta W}{W_1} \ll 1\right) \quad (5)$$

Base on the Equation (5), the width of the transistor M1 needs to be increased in order to achieve a good linear tuning range. If the R_1 is decrease, the delay tuning range value will be smaller. By increasing the capacitance load, the tuning range will increase as well keeping the linear response. But this will decrease maximum frequency and will increase the power consumption of the DCO.

The DCO evaluated by its power consumption, speed, chip area, frequency range, supply voltage and resolution [15], [20-22]. Low power dissipation requires reducing DCO power consumption to meet the low power demands in system on chip (SoC) design [6], [21-22]. For ADPLL, 50% of the total power contributed by DCO which is a major disadvantage. Therefore, power saving a major concern in many electronic devices. DCO requires multiple-phase clock or high frequency [23-25]. The attributes of frequency generation cause difficulty to the DCOs to operate at wide frequency range [26]. Voltage supply is the voltage used by the circuit to operate [27-28]. Reducing it will save power. Finally, to get fine tuning, it is important for the oscillator to have high resolution.

3.0 DCO SCHEMES FOR ADPLL

3.1 Varactor Pair in DCO

Figure 3 shows a simplified schematic of DCO used varactor pairs technique [16], [29-31]. There are two independent varactor banks in the DCO. The first is fine tuning bank and the other is coarse tuning bank. The fine-tuning bank comprise and utilize unit weighted encoding of the proposed varactor pairs. On the other hand, the coarse tuning bank utilizes binary-weighted encoding. It also consists of the conventional pMOS varactors. 5-bit fine tuning bank and 8-bit course tuning

bank can be controlled by the DCO. Fine-tuning frequency control word (FFCW) controls each pair of varactors. In addition, the DCO can also be designed with lesser number of pairs. Figure 3 shows that there are five pMOS pairs are used for simple operation. FCWROW controls the row while the FCW controls the untied unit varactor pair.

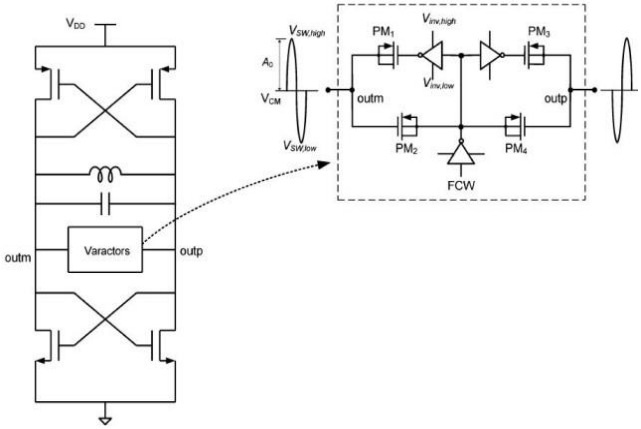


Figure 3 Schematic of DCO with varactor pairs [16]

The main idea of using varactor is for better frequency tuning application. Figure 4 shows the arrangement of varactor pairs. FCW_{ROW} has four control words. Each of them is connected with five varactor pairs unit. In the third row, four control words of the FCW control each unit varactor pair. There is also a pair control by the DCW in the centre of the layout for the dithering process to obtain a small fractional tuning resolution. The process variation is very sensitive to the small unit of capacitance in the tuning bank. Therefore, the DCO needs to increase reliability and to obtain uniform oscillation frequency by using the method of time averaging. Basically, the same amount of capacitance show has for each unit varactor pair cell. But during fabrication, it does not achieve the same. In Figure 4 show that for fine-tuning bank, in each clock cycle, one code can be expressed by different arrangement. By averaging different combination, the variation of capacitance can be decrease.

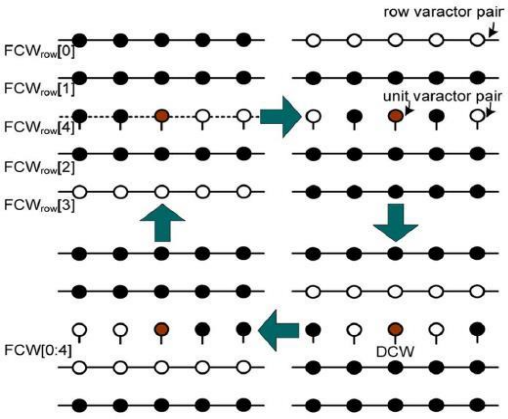


Figure 4 Arrangement of the unit varactor pairs in fine tuning [16]

3.2 Three Tuning Bank DCO

DCO schematic with load and three tuning banks is shown in Figure 5 [32]. The three segment tuning banks are coarse tuning bank (CB), fine tuning bank (FB) and mid-coarse tuning bank (MB). Each tuning bank has linear characteristics. Between the CB and FB bank, the gap in step size is bridge by tuning bank MB. The MB and CM are integrated with the transmission line (TL) as configurable metal shields that floats this is to form a compact, digital-controlled frequency tuning scheme. Both continuous-wave (CW) and frequency modulation (FM) in the ADPLL can be optimized by dividing FB into two part depicts in Figure 5(b). FM and FB_{LOOP} are dedicated to FB_{MOD} which is the centre of TL. It is used to correct DCO frequency wandering in the loop at low rate.

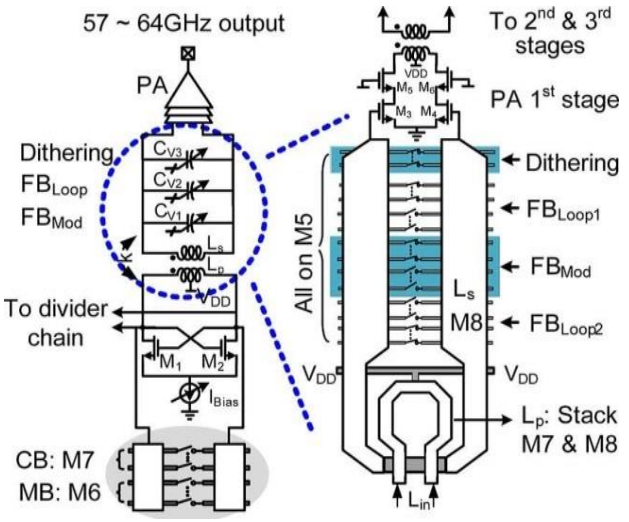


Figure 5 Schematic of DCO with three fine- tuning bank [32]

A decoding scheme for the FB is shown in Figure 6 proposed to overcome this problem. First turn ON half of the switches in each part (FB_{MOD} and FB_{LOOP}) by centering the fine-tuning bank. The switches in the upper half-part of FB_{LOOP2} are OFF (logic '0') and in the lower half-part of FB_{LOOP1} are ON (logic '1'). Both switches act as dummies when FB_{MOD} is at the centre position (logic '0'). The fine-tuning bank changes to state '+' when a small frequency drift upwards appears in the loop. This is the response to the positive phase error. Sufficient "virtual" dummy switches are attained for FB_{MOD} when switches are turned ON in the sequence shown in Figure 6. This type of gain should not happen in a normal operation. The DCO gain of FB_{MOD} achieves less than 5% nonlinearity and less than 0.1% of the DCO gain variation in FB_{MOD}. Even without extra dummy cell, FB_{MOD} measured relatively to the expected DCO gain non linearity with respected to the DCO centre frequency.

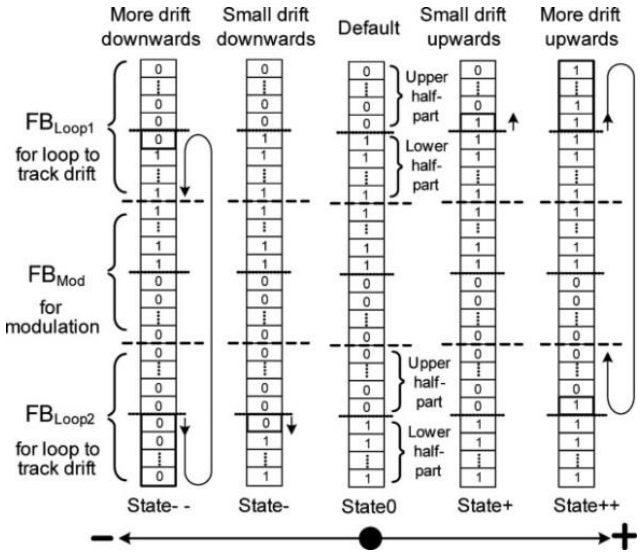


Figure 6 DCO fine-tuning bank decoding and configuration scheme [32]

3.3 Inductively Coupled Ditherless DCO

A DCO can limit the phase noise near the band edge from its quantization noise. To reduce to quantization noise, DCO dithering using a $\Delta\sum$ modulator has been used. Extra phase noise will be introduced when charge injected into the LC-tank through dithering if it were not properly retimed with a DCO clock [16], [29-30], [33-37]. A capacitor divider used to reduce the effective tuning step-size through shunt and reduce series combination of fixed capacitors with digital tuning varactors. However, this technique consumes metal-oxide-metal (MOM) and metal-insulator-metal (MIM) capacitors. This would limit the achievable tuning range. Digital tuning varactors also can be applied to the source nods of the cross-coupled transistor to improve the tuning resolution. An inductively coupled DCO reported can solve the DCO problems [36]. Circuit design and inductor layout of an inductive coupled DCO is shown in Figure 7.

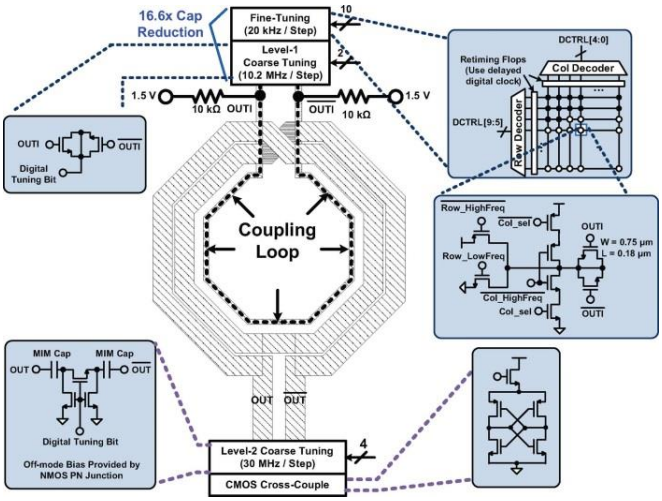


Figure 7 Inductively coupled DCO circuit and inductor layout [36]

In this design, it has a one-turn coupling loop and two-turn spiral inductor. The course tuning bank is placed on to the two-turn spiral inductor. Besides that, the coarse tuning bank and the fine-tune varactor bank are connected to the coupling loop. The one-turn coupling loop and the two-turn inductor form a transformer. When capacitance is applied to the coupling loop, it will reduce when translated to the main loop. For fine-tune and the varactor banks, the high-swing waveforms at the DCO output nodes are changed to low-swing waveform. This will result for the varactors in the coupling loop seem more linear and reduce the flicker noise.

3.4 Compensation Scheme

A wide frequency range can be achieved by using a compensation design on the DCO [38]. Figure 8 shows the architecture of DCO using the compensation scheme. This structural consist of the fine delay stage, the course delay stage and the switches. The switches can select tapping nodes where "UPPER" and "LOWER" are connected. There are 11 coarse unit stages and 6 taps used to achieve wide frequency range notably from 320 MHz to 1.25 GHz. The chain of the main inverter is made up of the coarse delay stage.

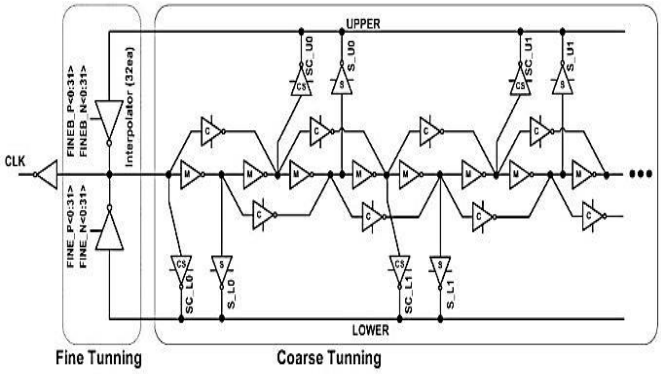


Figure 8 Compensation scheme on DCO architecture [38]

As shown in Figure 9, the compensator is made up of the current-starved inverter. Its driving strength can be controlled by a 4-bit binary code. Nominal voltage variations, chip calibration scheme and temperature are crucial in this process. The input is chosen by turning on one of the switches on "UPPER" and "LOWER" nodes. The interpolator and the transistor size of the compensator for the switch is bigger that the "C" compensator to deal with larger delay variation.

At fine stage, interpolation is employed to guarantee monotonicity with all digital control words. The fine stage consists of 32 current-starved inverters at each branch. It is also controlled with thermometer codes. The delay different between two selected taps and the number of the interpolation steps are used to determine the fine resolution. In 0.13 µm process, the delay differences between two taps with the optimized size produces 95 ps. Thus, the control bits number for interpolation steps can be reduced. The separate 32 fine interpolators-controlled pull-up and pull-down can improve the resolution.

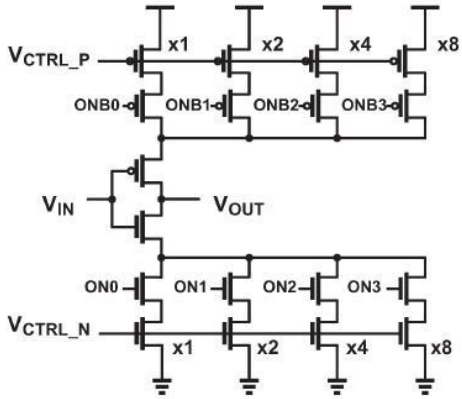
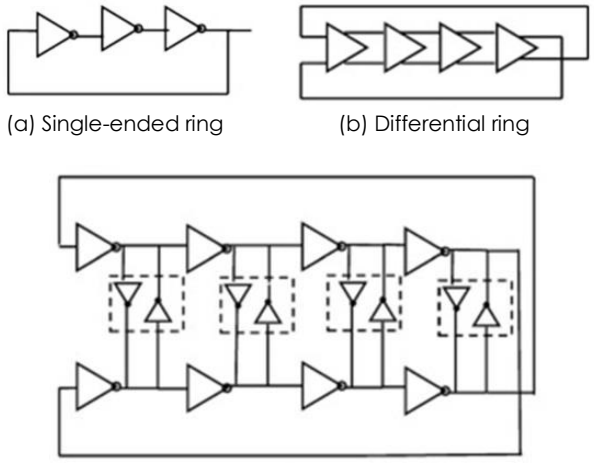


Figure 9 Structure of the DCO with compensator implemented [38]

3.5 Ring DCOs

DCO reported with mechanism to digitally change its frequency and an oscillator core. There are two broad categories of oscillator used in ADPLL. The first is LC oscillator and the other is ring oscillator [39-41]. LC oscillators are area-intensive but produce much better phase noise while ring oscillators are very are-efficient but have relatively have high phase noise. A vast majority radio frequency application generally requires LC oscillator. On the other hand, CDR use ring oscillator and PLLs used for clock generation [7]. Figure 10 shows commonly used ring oscillator topologies.



(a) Single-ended ring (b) Differential ring

(c) Pseudo-differential ring

Figure 10 Ring oscillator topologies [41]

Figure 10(a) is a single-ended ring oscillator. It used an odd number of inverter (usually 3 or 5). It is the most popular as it has the most power and area efficient topology. The frequency of this oscillator can be very wide range by using a digital to analog converter (DAC). Figure 10(b) shows a differential amplifier stages can be used to build a fully differential ring oscillator. A differential ring oscillator (DRO) can use an even number of stages which can be a distinct advantage. DRO is useful in some applications that need an even number of output clock phase. One problem for using differential amplifiers stage is that by simply use means of a current mode, DAC hardly achieve the frequency control. Therefore, either capacitors or resistors inside the stages need to be tuned. Although this is feasible, it is hard to produce a large tuning range while keeping a fine resolution without increasing the area consume. To overcome this problem, a pseudo differential architecture show in Figure 10(c) is proposed. A pseudo differential architecture is a single ended current controlled ring whose outputs are cross-coupled through latches. This it to force differential operation and ensure equally space output phases. The latch should be carefully sized because it adds power and phase noise. Dynamically decrease the latch size after the oscillation stabilizes will reduce latch power and improving the oscillator phase noise.

3.6 3G-DCO

A 3G-DCO can improve output frequency range, maximum output frequency and the resolution of the DCO simultaneously [8]. 3G-DCO is formed with a loop including three parts; alpha part, beta part, and gamma part. All these parts contributed directly to the DCO performances. For the alpha part shows in Figure 11 depicts the multistage tri-state buffer implement a series-connected delay chain with a path selector. It is used to extend the DCO output frequency range. Besides that, the maximum output frequency may be affected by the delay of series-connected delay chain. This drawback can be resolved by isolating the fastest path as an independent path; only happen if only one tri-state buffer exists in the fastest path.

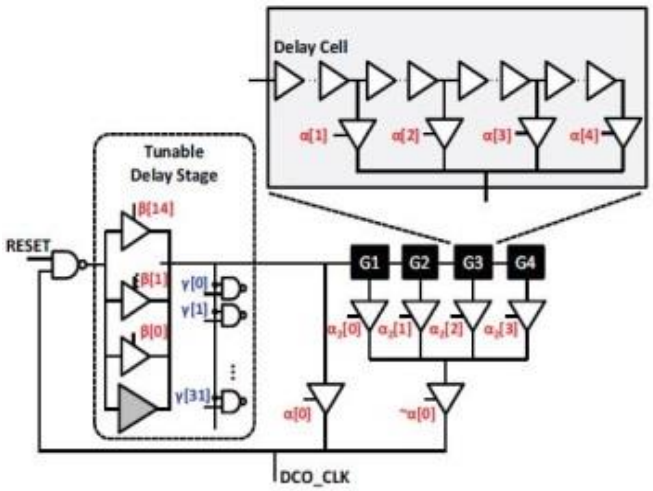


Figure 11 Architecture of 3G-DCO [8]

For beta part, varying driving strength method is used. In the tuneable delay stage, 15 tri-state buffer buffers are connected in parallel. Here is where a 4-b β-code controls the number of enabled and disabled tri-state buffers. Additional driving current is added when the number of enables tri-state buffers increases. Therefore, the overall delay of the delay chain will decrease. The gamma part determines the finest resolution of the DCO. Variable loading capacitance is provided by a number of two-input NAND gates to a tuneable-delay stage. By controlling the number of turned on NAND gates one can thus fine-tune the output frequency of the DCO. This is because the increase number of the turn-on NAND gates will increase the loading effect on the output node of the tuneable delay stage. In conclusion, the resolution of DCO is decided by the clock period difference of the DCO between turn k NAND gates and $(k+1)$ NAND gates.

3.7 DCO Combined with DAC and VCO

Many researchers developed ADPLL that uses a DCO composed of a DAC and VCO depicts in Figure 12 to produce a very high-resolution DAC but utilized big silicon area [34], [41], [45-49]. Therefore, another approach reported a high-speed dithering on the digital filter output fractional part.

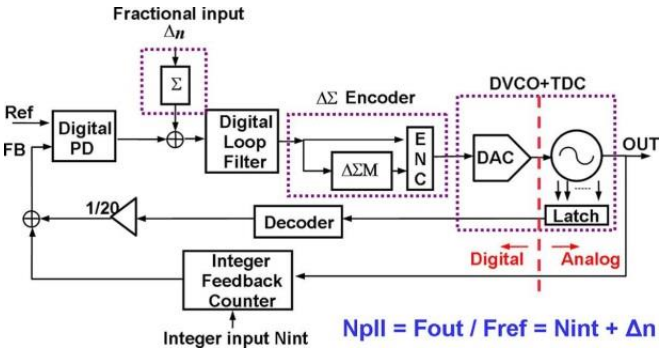


Figure 12 ADPLL architecture with DCO combined with DAC and VCO [48]

The interface between the DAC array and digital filter is shown in Figure 13. To enhance the DAC resolution, the fractional control word from the digital loop filter is fed into a configurable first/second order delta sigma modulator. The integer control word and modulation output are first summed together which then converted into a thermometer code. The 9-bit unitary DAC array is directly controlled by this code. One advantage of performing thermometer encoding is that even if the DAC unit is not exactly match, the frequency operation range is still fully covered.

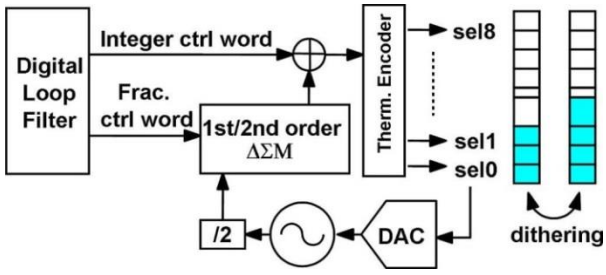


Figure 13 DAC interface [50]

4.0 DISCUSSION AND CONCLUDING REMARK

This review article presented various design topologies of digital controlled oscillator (DCO) designs in ADPLL. Table 1 provides a quick summary to aid the reader about different DCO techniques advantages and disadvantages. The understanding of basic principle and consideration are vital in designing DCO.

Table 2 summarize the design performance of different ADPLL applications used DCO reported from

2010 to 2018. The table also compare important DCO parameters including CMOS process design technology, input power supply (voltage) and power consumption (Watt) of the circuits. Furthermore, chip area, DCO resolution and frequency range are included for quick understanding. Varactor pairs in DCO scheme found consume more power compare the rest of the design technique. This is one of the drawbacks in obtaining a better DCO performance is terms of resolution and good jitter. Despite the fact of high power consumption, it does not affect much to the chip area. Wanghua *et al.* (2014) have achieved the first 60GHz ADPLL by using three tuning bank design in the DCO scheme.

Besides having a good frequency range, it produces good jitter, ultra-fast settling, and very low spur but this varactor pair scheme suffers high power consumption consuming more power to the circuit. Inductive coupled ditherless DCO design scheme produced good resolution and wide frequency range. Besides, the circuit function using low voltage supply and has wide frequency range DCO. This method reduced the silicon area of the DCO core by 50% and lowering power consumption by 67%. The ring DCO scheme also consumed smaller area, power efficient and wide frequency range combine with fine resolution. Pei-Ying *et al.* (2013) developed 3G-DCO design [8]. It achieved low jitter, consume low power and low design area. The work done in [19] produced the highest tuning range and is possible to obtain quadrature signals.

Finally, the DCO combine with DAC and VCO scheme show fascinating results by improving linearity while decreasing the area and power usage. We can conclude that even though there are various schemes of DCO that have been implemented for ADPLL, the selection of the DCO is frequently based on the ADPLL applications and the complexity of the scheme. The DCO is recognized as one of the modules that can give direct impact to the ADPLL performance. ADPLL needs low voltage and low power consumption, small chip area, highly portable, wide frequency range, and high resolution of DCO designs. The considerations to these DCO parameters are vital in improving APDLL performance.

Table 1 Advantages and disadvantages of DCO schemes

Item	[Reference]	DCO scheme	Advantages	Disadvantages
3.1	[16], [29-31]	Varactor Pair in DCO	• Good resolution • Good jitter performance • Small area	High power consumption
3.2	[32]	Three Tuning Bank DCO	• First 60Ghz ADPLL ever recorded • Good jitter • Ultra-fast settling	High power consumption
3.3	[33-34], [36-37]	Inductive Coupled Ditherless DCO	• Fine DCO resolution wide frequency range • Work with low voltage supply • DCO phase noise lower than oscillator phase noise	
3.4	[38]	Compensation Scheme DCO	• DCO area reduce by half and power consumption by two third	
3.5	[39], [40-44]	Ring DCOs	• Wide frequency range • Fine resolution • Area and power efficient	
3.6	[8]	3G-DCO	• Achieve small area • Low power and low jitter	
3.7	[46-49]	DCO combine with DAC and VCO	• Linearity improved • Area and power consumption decrease	

Table 2 Performance characteristic DCO in different ADPLL application

Year [Ref]	DCO Scheme	Application	Process Technology (nm)	Power Supply (V)	Power Consumption (mWatt)	Chip Area (mm^2)	Resolution (ps)	Frequency Range (GHz)
2010 [28]	Ring DCOs	ADPLL with time windowed TDC	90	1.2	8.1	0.37	-	2.1 – 2.8
2010 [43]	Ring DCOs	Wireless sensor nodes	65	1.3	0.2	0.03	30	1
2010 [48]	DCO combine with DAC and VCO	DPLL with TDC	65	1.2	3.2	0.027	22	0.6 – 0.8

Year [Ref]	DCO Scheme	Application	Process Technology (nm)	Power Supply (V)	Power Consumption (mWatt)	Chip Area (mm^2)	Resolution (ps)	Frequency Range (GHz)
2010 [50]	Varactor Pair in DCO	LC-Tank Oscillator for DCO	65	1.8	16	0.315	-	3
2011 [10]	Varactor Pair in DCO	Multirate signal processing	65	1.2	32	0.35	-	-
2011 [21]	Compensation Scheme DCO	Clock and data recovery in ADPLL	130	1.2	11.4	0.074	1.0	0.4 – 2.1
2011 [24]	Ring DCOs	Bang-bang phase detector and integrated jitter	65	-	4.5	0.22	0.56	2.92 – 4.05
2011 [26]	Compensation Scheme DCO	Built in self-calibration circuit in DCO	65	1	0.142	0.01	13.2	0.048 – 0.539
2011 [38]	Compensation Scheme DCO	Feedforward inverter	130	1.2	1.68	-	-	0.32 – 1.25
2011 [4]	Varactor Pair in DCO	DPLL with Bandwidth Tracking	90	1	1.6	0.36	-	0.7 – 3.5
2011 [8]	3G-DCO	A jitter and power analysis in ADPLL	130	1.2	3.8	0.083	2.8	0.179 – 0.656
2012 [22]	Compensation Scheme DCO	Interlaced hysteresis delay cell	90	1.0	0.466	0.0086	3.5	0.18 – 0.53
2012 [23]	Ring DCOs	Digital Dual Loop CDRs	130	1.2	14-37	-	-	6 – 11.5
2012 [31]	Varactor Pair in DCO	ADPLL with Digital Supply Regulator	90	0.6	0.656	0.02	-	0.096 – 0.72
2012 [45]	Varactor Pair in DCO	Thermal Diffusive based DCO	160	1.8	2.1	0.5	20	-
2013 [25]	Ring DCOs	Digitally controlled delay lines in ADPLL High-Resolution	90	1	0.0282	0.032	-	0.5 – 1.0
2013 [29]	Varactor Pair in DCO	Millimeter-Wave	90	1 .2	12	0.16	-	56 – 62
2013 [30]	Varactor Pair in DCO	Stacked-LC DCO	180	1.5	9.2	0.1	-	2.4
2013 [34]	Inductive Coupled Ditherless DCO	DCO using Variable Inductor	90	1.2	19	0.075	-	37.6 – 43.4
2013 [36]	Inductive Coupled Ditherless DCO	Inductively Coupled Fine-Tuning DCO	180	1.8	17	0.62	-	2.8 – 3.2
2013 [41]	Ring DCOs	Clock multiplication techniques	130	1.1	1.35	0.2	0.9	0.8 – 2.0
2013 [46]	DCO combine with DAC and VCO	ADPLL for GALS n MPSoCs	65		2.7	0.0078	5.4	0.083 – 4

Year [Ref]	DCO Scheme	Application	Process Technology (nm)	Power Supply (V)	Power Consumption (mWatt)	Chip Area (mm^2)	Resolution (ps)	Frequency Range (GHz)
2013 [8]	Inductive Coupled Ditherless DCO	Smooth Code jumping	100	1.8	7.2	0.084	4.3	0.096 – 1.014
2014 [22]	Three Tuning Bank DCO	Two-point modulator	65	1.0	6.9	0.49	-	1.66 – 2.08
2014 [32]	Three Tuning Bank DCO	FMCW Radar	65	1.2	89	0.5	-	56.4 – 63.4
2014 [39]	Ring DCOs	Dual-loop ADPLL	28	1.0	3.1	0.032	15	0.25
2017 [17]	Ring DCOs	Dual-loop ADPLL	130	0.7	3.5	-	-	3.82 – 4.12
2016 [18]	Ring DCOs	Dual-loop ADPLL	90	0.5	2.8	-	-	0.16 - 1.5
2018 [19]	DCO combine with DAC and VCO	Dual-loop ADPLL	180	1.8	3	-	-	0.009 - 3.7
2017 [51]	Ring DCOs	Dual-loop ADPLL	130	0.5	15	-	-	3.06 – 7.25
2017 [52]	Ring DCOs	Dual-loop ADPLL	180	0.5	11	-	-	3.6 – 3.9
2017 [53]	Ring DCOs	Dual-loop ADPLL	180	1.2	8	-	-	1.26

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