

A VERY LOW-DROPOUT VOLTAGE REGULATOR IN 0.18- μM CMOS TECHNOLOGY FOR POWER MANAGEMENT SYSTEM

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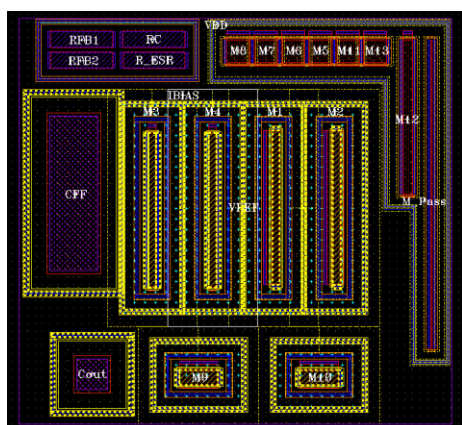
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Graphical abstract



Abstract

A low dropout (LDO) voltage regulator is a type of voltage regulator circuit that works well even when the output voltage is very close to the input voltage, improving its power efficiency. This paper proposes the LDO voltage regulator in 0.18- μm CMOS technology. The proposed LDO regulator consists of voltage reference, symmetrical operational transconductance amplifier (OTA), PMOS transistor, resistive feedback network and output capacitor. The NMOS symmetrical OTA is implemented as an error amplifier and a PMOS transistor is employed as a pass device to improve gain and minimize low dropout voltage, respectively. The proposed design is simulated using Spectre simulator in Cadence software to verify its regulator performance. The simulation results show that the proposed LDO is capable to operate from a supply voltage of 1.7-2.0 V with a low dropout voltage of 19.3 mV at a maximum 50 mA load current to regulate output voltage 1.5 V. The active chip is 2.96 mm² in size. The performance of the proposed LDO is suitable to enhance power management for system on chip (SoC) applications.

Keywords: Low-dropout, voltage regulator, output capacitor, resistive feedback, load current

Abstrak

Pengatur voltan kecikiran amat rendah (LDO) adalah satu jenis litar voltan pengatur yang berfungsi dengan baik walaupun voltan keluaran sangat dekat dengan voltan masukan seterusnya meningkatkan kecekapan kuasanya. Kertas ini mencadangkan reka bentuk LDO bagi teknologi CMOS 0.18- μm . Pengatur LDO yang dicadangkan terdiri daripada rujukan voltan, penguat aliran kendalian simetri (OTA), transistor PMOS, rangkaian suap balik rintangan dan kapasitor keluaran. OTA semetri NMOS dilaksanakan dengan penguat ralat dan satu transistor PMOS dijadikan sebagai peranti lulus untuk meningkatkan gandaan dan mengurangkan voltan kecikiran rendah, masing-masing. Reka bentuk yang dicadangkan telah disimulasi menggunakan simulator Spectre dalam perisian Cadence untuk mengesahkan pencapaian pengatur. Keputusan simulasi menunjukkan LDO yang dicadangkan berupaya untuk beroperasi dari 1.7-2.0 V voltan pembekal dengan voltan kecikiran rendah ialah 19.3 mV pada arus beban maksimum 50 mA untuk mengatur 1.5 V voltan

keluaran. Saiz cip aktif ialah 2.96 mm². Prestasi bagi LDO yang dicadangkan adalah sesuai untuk meningkatkan pengurusan kuasa bagi penggunaan sistem dalam cip (SoC).

Kata kunci: Keciciran rendah, pengatur voltan, kapasitor keluaran, suap balik rintangan, arus beban

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1.0 INTRODUCTION

The growth in electronics industry, coupled with the demand of efficient and compact power management systems has been the driving factor behind the efficient analog circuit design [1, 2]. As such, the circuits are desired to operate and consume minimum amount of power, lower values of standby current, lesser real estate, thus improving the battery life and making it more reliable for low voltage and low power management solutions [3, 4]. The demand for low voltage, low dropout regulators is expanding because of the developing interest in portable electronic devices, such as, mobile phones, pagers, laptops and others [5]. These mobile gadgets advertise requires low voltage and low quiescent current flow to increase the battery efficiency and longevity. The requirement for low voltage is intrinsic to portable low power gadgets and validated by lower breakdown voltages resulting from reduction in feature size [6]. Low quiescent current in a battery-operated system is an intrinsic performance parameter because it partially determines battery life.

LDO regulator being one of the fundamental building blocks of power management unit which is used in many portable battery powered systems [7]. Since the constant and stable output voltage of LDO regulator independent of the load impedance, input voltage variation, temperature and time is required as the battery discharges [8]. This characteristic leads to crucial stability improvement and noise reduction for subsequent circuits. Due to the rapid growth of technology trend, designers are forced to design circuits operating at lower supply voltages [9]. Thus, the LDO regulators are incorporated as they are ideal for giving multiple voltage levels and operate with a rather low dropout voltage [8]. In addition, LDO regulators also have capability of minimizing current consumption down to microamperes, which is important for current consumption of the sub-block in sleep mode. Another important characteristic of linear voltage regulator is their ability to suppress supply voltage noise, thus shielding the noise-sensitive blocks. As a result, power supply rejection ratio (PSRR) is an important parameter of linear regulators. Besides that, LDO linear voltage regulators are mostly

used in integrated circuit (IC) design due to their performance, low cost and simplicity [10].

Many types of LDO regulators have been proposed and developed by previous researchers to enhance the performance of the LDO regulators [5, 11, 12, 13, 14, 15, 16]. One of the most important parameters in designing the LDO regulator is the low dropout voltage [12]. Many techniques have been employed to obtain low dropout voltage such as double recycle folded cascode, bulk modulation and zero temperature coefficient compensated by MOS transistor and etc. were proposed [5, 12, 14, 15]. However, high dropout voltage was obtained. A folded cascode operational amplifier were proposed as an error amplifier which provide high gain and high output impedance [11, 12, 13, 14, 15, 16, 17]. The folded cascode structure has high efficiency of 120 mV drop out voltage was achieved by using active resistor feedback circuit which required additional circuit for transient enhancement [17]. Heavy load boosting and slew rate enhancement circuits were also adopted in LDO regulators to reduce drop out and enhance slew rate, respectively [14, 15]. In past, the proposed LDO required compensation circuit in order to meet the performance improvement [13, 14, 15, 16, 17]. Nevertheless, extra circuit on designing LDO increases the complexity of circuitry, high power consumption and large silicon area which are not suitable for SoC.

In this paper, a simple LDO voltage regulator is proposed using 0.18- μ m CMOS technology. The proposed LDO employed a NMOS symmetrical OTA with PMOS transistor as pass element to improve gain and reduce the dropout voltage less than 100 mV without needed extra compensation circuits. Based on our knowledge, this is the lowest drop out voltage LDO regulator that has been proposed up to date. This paper is organized as follows. Section 2 discusses the basic LDO voltage regulator in detail and Section 3 explains the proposed LDO regulator. In Section 4, the results and discussion along with the comparison with related work is presented. This paper concludes with a summary in Section 5.

2.0 BASIC LDO VOLTAGE REGULATOR

A basic LDO voltage regulator topology usually consists of an error amplifier, a voltage reference, a pass device, an external load capacitor with small amount of internal resistance and a resistive feedback network [6]. Figure 1 shows the overall topology of LDO voltage regulator. The basic schematic of generic LDO voltage regulators is based on a PMOS. The PMOS field effect transistor (FET) with common source configuration operates as the pass transistor between the input and the output voltages. A part of the output voltage is fed back through resistors R_{f1} and R_{f2} to the input and is compared to the voltage reference V_{ref} . An error amplifier in negative feedback condition detects an error signal when there is a difference between the feedback voltage and reference voltage. The error signal will control the gate of the pass transistor for maintaining constant output voltage to supply a variable current to the load circuit. The OTA is suitable for error amplifier since the output of error amplifier is utilized to drive the gate of the pass transistor [6]. Therefore, in the proposed design the OTA is implemented as an error amplifier.

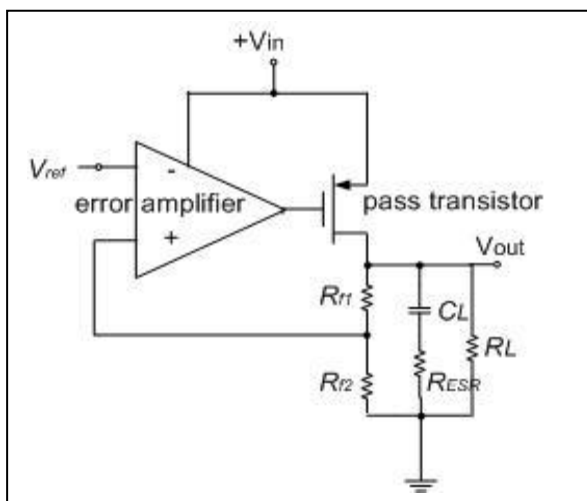


Figure 1 Basic topology of low dropout voltage regulator [6]

A NMOS transistor and PMOS transistor are normally used as a pass transistor in LDO regulator. However, a drawback of the NMOS is large dropout voltage when used as the pass transistor. Therefore, the PMOS pass transistor is a favorable candidate due to its good performance in dropout voltage, quiescent current flow, output current and speed [18]. The loop gain, bandwidth and stability also influenced by the pass device. The pass transistor should have large ratio of width and length in order to drive the maximum load current as well as to improve low dropout performance. However, by using large size of pass transistor, the gate capacitance will be increased and causes instability

in the system [19]. The voltage reference provides the nominal output voltage. As depicted in Figure 1, the resistors of R_{f1} and R_{f2} are used to obtain the output voltage V_{out} .

Voltage reference is used to set the operating point of the error amplifier which indicates the starting point of all regulators. The voltage reference V_{ref} is usually a band-gap type because it gives capability to operate at low supply voltages and better accuracy and stability under temperature variation which is sufficient for design of linear regulators. The overall power supply rejection ratio (PSRR) of the error amplifier is influenced by the output noise and contribution from the voltage reference. Addition of passive component filters to the design such as RC filters can be used to minimize the effect.

The design of error amplifier should be done in a simple manner so that it does not consume too much current. In general, an operational transconductance amplifier (OTA) is implemented to function as error amplifier due to its ability to drive the capacitive loads and the fact that the design is simple. Several requirements must be satisfied by the OTA such as low quiescent current, high power supply rejection ratio (PSRR), high open-loop gain, and high output voltage swing.

Generally, a transistor is utilized to operate as a pass element. The main function of the pass device is to drain current from the supply to the load. There are various topologies of pass devices such as PMOS with common source, NPN Darlington, PNP with common emitter, NPN follower and NMOS follower [16]. The designer is free to choose the correct topology based on the process technology that has been use and the LDO specifications. PMOS transistors are preferred as the pass device because they produce quiescent current flow, output current, good compromise of dropout voltage and speed.

The output capacitor consists of external load capacitor and small value of equivalent series resistance (ESR). Since the transient response depends on the output capacitor value (C_o) and the ESR of the output capacitor (R_{ESR}), large output capacitor and low ESR value is required to enhance the load transient response. In addition, the load transient response could be enhanced by adding a bypass capacitor (C_b) to the output capacitor. The output capacitor also plays an important role in the stability of the system, because it forms a low frequency pole and a zero at higher frequencies.

A control loop is formed between the operational amplifier and the pass transistor through the feedback network. Resistive feedback network scales the output voltage (V_{out}) to compare with the reference voltage (V_{ref}) by the error amplifier. It counteracts the effects of load current and also biases the pass transistor. Pair of resistors (R_{f1} and R_{f2}) are generally used to perform this task.

3.0 CIRCUIT IMPLEMENTATION

The schematic design of the proposed low-dropout (LDO) voltage regulator is presented in Figure 2. All the bulks of NMOS transistors are connected to ground and the bulks of PMOS are connected to supply voltage. The proposed LDO regulator consists of a symmetrical operational transconductance amplifier (OTA), a voltage reference, a PMOS pass transistor, a resistive feedback network and an external load capacitor with small value of equivalent series resistance (ESR). An error amplifier (EA) provides desirable transconductance and therefore voltage gain for the circuit. The proposed LDO is designed using 0.18- μm CMOS technology.

The EA consists of NMOS input pair M1 and M2 with PMOS active load M6 and M7. The drain current of M1 and M2 are mirrored to M5 and M8, respectively. The current I_1 and I_2 can be obtained from Equation (1) and (2):

$$I_1 = \frac{I_{bias}}{2} - g_{m(2)}V_{ref} \tag{1}$$

$$I_2 = \frac{I_{bias}}{2} - g_{m(1)}V_{fb} \tag{2}$$

The single ended output is taken with current flow as shown in Equation (3):

$$I_0 = 2g_{m(1,2)}\alpha v_i \tag{3}$$

Where $v_i = v_{fb} - v_{ref}$ the differential output whereby the voltage controlled current source is obtained. The transconductance of this OTA, G_m is represented by Equation (4):

$$G_m = \frac{I_0}{v_i} = 2\alpha g_{m(1,2)} \tag{4}$$

The transconductance of the OTA in Equation (4) is dependent on the g_m of the M1 and M2. The parameter alpha (α) is the gain factor that can be obtained by varying the transistor size W/L of M12 and M11. The load current flow through the pass device M_{pass} can be controlled to achieve a constant output voltage v_o by properly choosing values of reference voltage V_{ref} and resistors R_{FB1} and R_{FB2} . The output voltage is obtained by using Equation (5):

$$v_o = v_{ref} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \tag{5}$$

A current sink for input pair is M4. Transistors M3, M4 and M9, M10 are simple current mirror. The differential output from EA is connected to M11 and M12 to produce single ended signal to pass transistor.

The PMOS pass transistor M_{pass} is employed in the proposed LDO due to low power supply ripple rejection. In addition, PMOS helps to obtain low dropout voltage as compared to NMOS. Large PMOS transistor is required to increase current driving capability. The EA forms a negative feedback loop, which compares the error signal at the output with the reference voltage V_{ref} voltage to maintain constant output voltage by varying the gate voltage of pass transistor, and hence controlling the current flowing through it.

Meanwhile, the output capacitor C_{out} and an equivalent series resistance R_{ESR} are connected in the output node to provide stability for the circuit. The value of R_{ESR} of 0.5 Ω is selected to reduce the overshoot at the output. Resistive feedback network consists of resistors R_{FB1} and R_{FB2} operate as a voltage divider to set the output voltage. The transistors dimensions and other components of the proposed LDO regulator are represented in Table 1.

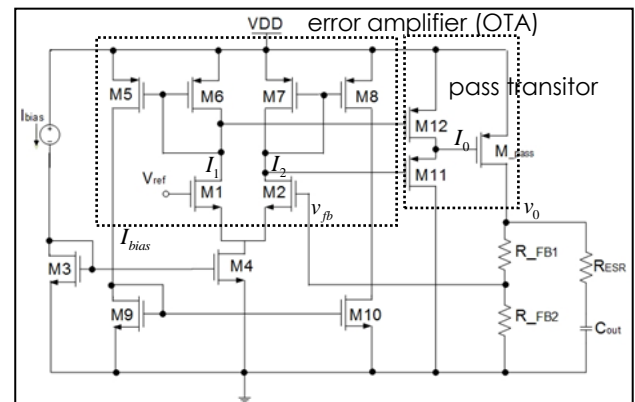


Figure 2 Schematic design of the proposed LDO voltage regulator

Table 1 The component value for the proposed LDO

Parameter	Value
M1, M2	20 μm /1 μm
M3, M4	1 μm /20 μm
M5, M6, M7, M8	3 μm /3 μm
M9, M10	2 μm /5 μm
M11, M12	3 μm /3 μm
M_{pass}	40 μm /0.18 μm
R_{FB1}	200 k Ω
R_{FB2}	800 k Ω
R_{ESR}	0.5 Ω
C_{out}	50 pF

4.0 SIMULATION RESULTS

In the proposed low LDO regulator has been designed in 0.18- μm CMOS technology. Three types of analysis are performed to verify the LDO regulator performance which are DC, transient and AC analysis. The DC analysis focuses on steady state parameters, transient analysis computes the LDO's

response as a function of time and AC analysis calculates the small-signal response of the LDO regulator. The proposed LDO regulator is simulated based on the input voltage range from 1.7 V to 2.0 V, input reference voltage of 1.2 V, output voltage of 1.5 V and the biasing current of 100 nA.

The input-output voltage characteristic of the proposed LDO regulator is obtained by sweeping the DC input voltage supply from 0 V to 2 V as shown in Figure 3. The characteristic is obtained under maximum load current conditions (I_{load}) of 50 mA in order to verify the dropout voltage value. As observed, the output voltage remains regulated for an input voltage range from 1.5 V – 2.0 V at output voltage of 1.5 V. The dropout voltage can also be extracted from Figure 3. It is a parameter that gives information about the LDO regulator efficiency. The dropout voltage value was obtained at the beginning of the regulation region of $V_{DO} = 19.3 \text{ mV}@V_{out} = 1.5 \text{ V}$. There is no dropout voltage in the dropout region since the input voltage increases linearly with the output voltage. According to the result, it could be seen that the LDO regulator is in the regulation region when the output voltage level is high enough. Therefore the LDO regulator can perform its two main functions such as keep the output voltage stable and deliver the required current to the load.

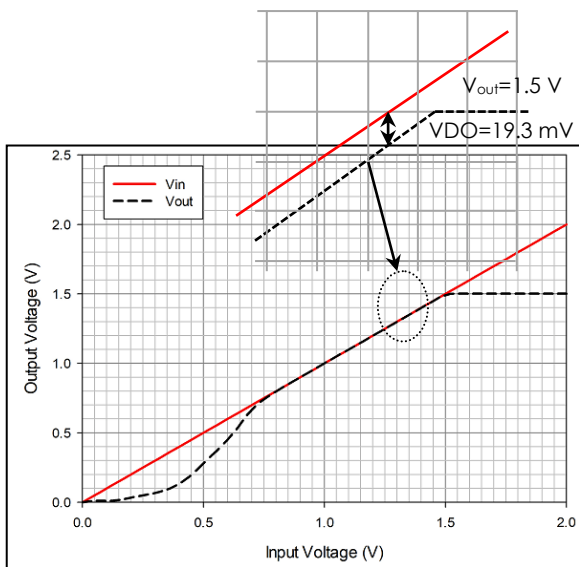


Figure 3 Input-output characteristics at output voltage 1.5 V

The line regulation is defined as the change at the output voltage in response to a change in the input voltage at a constant load current. This parameter is usually tested under the maximum load current conditions. The line regulation value can be extracted from the output variation ratio and results from a specific change in input voltage or in reference voltage, when the load circuit is open.

Figure 4 illustrates the changing of output voltage with respect to the input voltage when the LDO operates in the linear region (regulating region). As can be seen, the line regulation of 1.67 mV/V was achieved for 1.5 V output voltage with a constant load current of 50 mA.

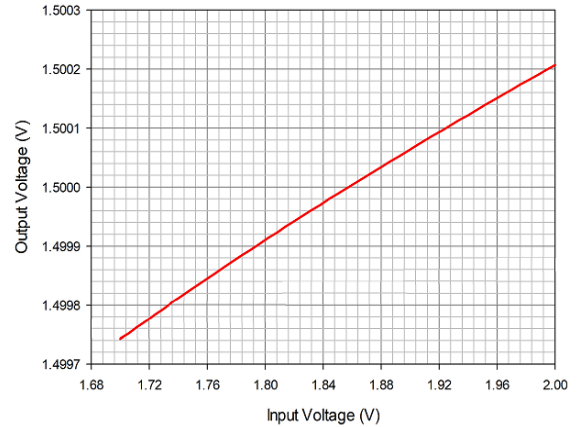


Figure 4 Simulated LDO regulator line regulation at 1.5 V output voltage

The load regulation is defined as the change at the output voltage due to a change at the load current keeping the input voltage constant. Figure 5 shows the simulated load regulation at input voltage of 1.7 V under maximum load current conditions of 50 mA. As observed, a load regulation of 0.92 mV/mA was obtained when the load current changes from 10 μA to 50 mA at 1.5 V output voltage.

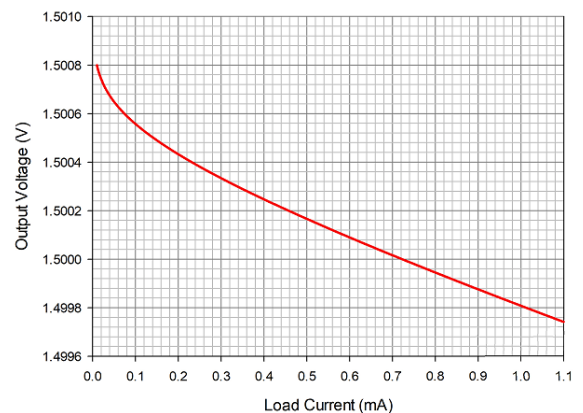


Figure 5 LDO regulator load regulation simulation

Transient analysis is performed to investigate how the circuit behaves in real time with varying large signal transients. The important parameters of LDO regulator in transient domain are line and load transient responses. Figure 6 shows the load transient response at 5 kHz frequency. A small overshoot in the LDO output voltage in the millivolts range can be

observed. The overshoot is mainly caused by the equivalent series resistance (ESR) of the output capacitor. The larger the current step and ESR, the bigger the overshoot because the capacitor is trying to sink the current to the load

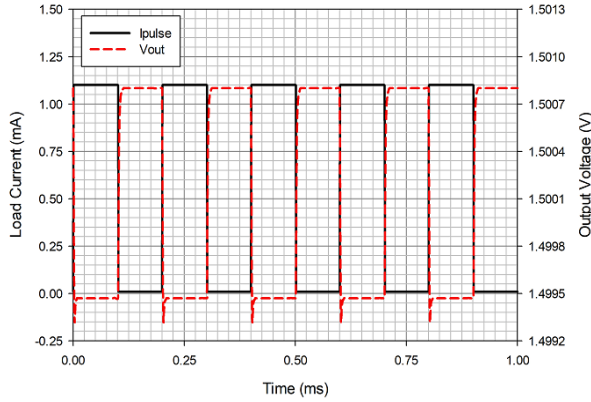


Figure 6 Load transient at low frequency of 5 kHz

The line transient behaves quite differently from the load transient. The difference between the steady state voltages of the line transient is much lower, because it corresponds with the power supply rejection and line regulation. The overshoots of the line transient are in opposite directions to the overshoots of the load transient. There is a large difference between line transient for small and large load current. Figure 7 illustrates the line transient response at maximum load current.

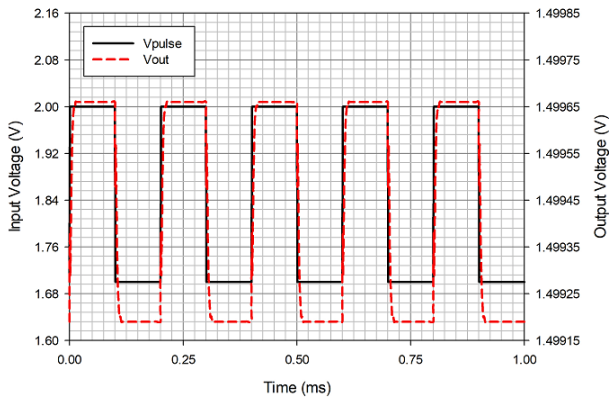
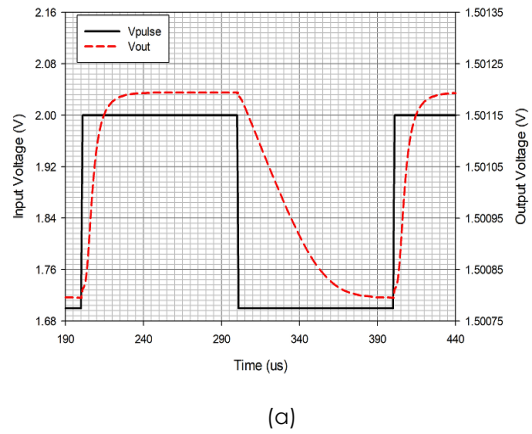


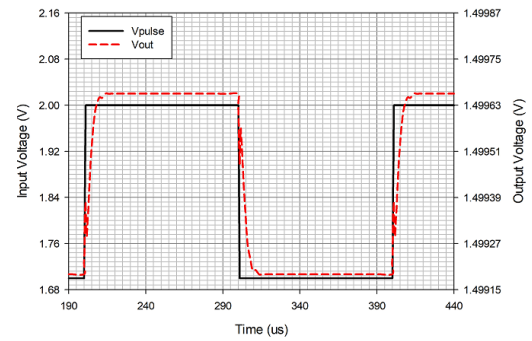
Figure 7 Line transient from 1.7 V to 2.0 V for load current of 50 mA at 5 kHz frequency

Figure 8 shows the line transient response at load current of 10 μ A and 50 mA. Both results are analyzed and comparison is deduced in line transient response for different load current. As observed, the response is fast when the voltage rises due to the capacitor being charged by the current from the supply. However, when the voltage drops, the output

capacitor holds its value for longer time because it is discharged only by a small amount of load current.



(a)



(b)

Figure 8 Line transient from 1.7 V to 2 V, (a) at load current of 10 μ A, (b) at load current of 50 mA

It is essential to measure the open-loop parameters such as the open-loop gain and phase angle to define the phase margin and gain margin. Open-loop parameter such as phase margin also defines how the circuit behaves under step response inputs. The most important parameter is stability, which is defined by phase angle and gain margin. The gain margin (GM) and the phase margin (PM) can be achieved by properly sizing the transistors size in error amplifier. The GM and the PM can be obtained from the bode plot. Figure 9 shows the bode plot of open-loop gain and phase margin at frequency range from 1 Hz to 100 MHz at output resistance, R_{ESR} of 0.5 Ω and output capacitor, C_{out} of 50 pF. The GM is obtained when the phase angle is equal to 0°. As observed, the GM of the proposed LDO regulator is -19.34 dB. Meanwhile, the PM is attained when the open-loop gain is equal to 0 dB. As observed, the proposed LDO regulator has the PM of 69.45°. As such, the proposed LDO is in stable condition.

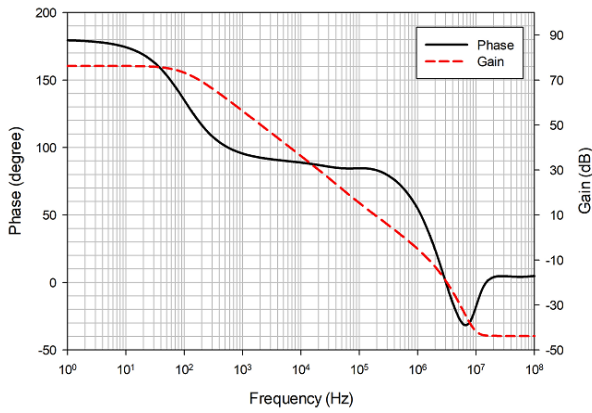


Figure 9 The bode plot of open-loop gain and phase margin

The next important parameter from AC analysis is power supply rejection ratio (PSRR). The PSRR is defined as how well the regulator suppresses the changing input voltage over the wide frequency range. Figure 10 shows the PSRR of the proposed LDO voltage regulator at input voltage of 1.7 V. As can be seen, the LDO regulator exhibits a PSRR value of -54.92 dB at 1 kHz at output voltage 1.5 V. PSRR can be improved by using low ESR value of the output capacitor and high output capacitor value. Finally, figure 11 shows the layout of the proposed LDO regulator. The total layout area is 52.60 μm x 56.20 μm .

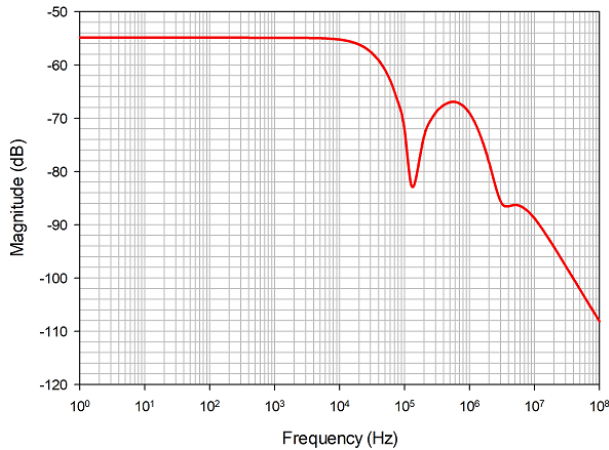


Figure 10 The simulated LDO regulator PSRR

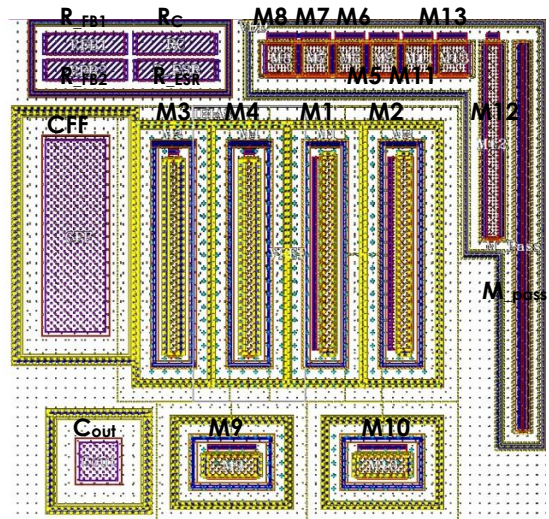


Figure 11 Layout of proposed LDO regulator in 0.18- μm CMOS technology

The proposed LDO regulator is compared with other related works as shown in Table 2. The references [11-13] and [17] are simulation results while references [14] and [15] are measurement results. Most of the previously published LDO regulators using a folded cascode (FC) for error amplifier [11, 12, 13, 14, 15, 16, 17]. In addition, buffer, pseudo load boosting, transient enhancement and heavy load boosting of compensation circuits are required, thus make the LDO circuitry design become complicated [11, 12, 13, 14]. The high dropout voltage more than 100 mV was obtained for all LDO regulators. However, the proposed LDO regulator in this work which implemented a NMOS symmetrical OTA gives the lowest dropout voltage of 19.3 mV as compared to the previously published works without any compensation circuit is required. Moreover, the proposed LDO regulator exhibits better line regulator of 1.67 mV/V which make it a useful choice in battery-powered portable application. Besides, the proposed design has higher power supply rejection (PSR) of -54.92 dB when compared to the proposed LDO regulator in [12] at frequency of 1 kHz. Based on these comparisons, the proposed LDO voltage regulator shows a very promising opportunity for power management system on chip (SoC) applications.

Table 2 Comparison with previously published LDO voltage regulators

References	[11]	[12]	[13]	[14]*	[15]*	[17]	This work
Year	2013	2015	2018	2017	2018	2017	2019
CMOS technology (μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	1.8	1.45 – 2	1.8	0.7-0.9	2.0-3.3	1.3-3.6	1.5 – 2.0
Output voltage (V)	1.64	1.4	-	0.5	1.8	1.2	1.5
Dropout voltage (mV)	160	200	200	200	200	120	19.3
Load current (mA)	150	0-100	50	50	-	50	50
Quiescent current, I_q (μA)	0.33	68	21.89	-	1.2	5.9	4.59
Line regulation (mV/V)	-	7.27	65	71.25	15.38	0.038	1.67
Load regulation (mV/mA)	-	0.016	2.4	0.438	0.4	0.002	0.92
PSR at 1 kHz (dB)	-	-49.26	-	-	-	-	-54.92
Chip size (mm^2)	-	-	-	0.10	0.42	-	2.96
C_{Load} (pF)	-	-	50	-	-	50	50
Error amplifier	FC	FC	FC	Constant gate-source	FC	FC	OTA
Compensation circuit	Buffer	Compensation	Transient enhancement	Load boosting	Buffer + SRE	Transient control circuit	No

FC : folded cascode

*experiment

5.0 CONCLUSION

A very low-dropout voltage regulator using 0.18- μm CMOS technology was successfully designed and simulated. A PMOS pass device was chosen because it gives a good trade-off between dropout voltage, quiescent current flow, output current and speed. An operational transconductance amplifier (OTA) was utilized as an error amplifier since the pass device has a high capacity load. Symmetrical OTA circuitry was chosen due to its large output voltage swing as its output voltage varies significantly with the changing load conditions. The proposed design provided a regulated output voltage of 1.5 V with the input voltage range from 1.5 V to 2 V. The LDO regulator has the dropout voltage of 19.3 mV and the quiescent current of 4.59 μA . The line and the load regulation for the proposed design were 1.67 mV/V and 0.92 mV/mA, respectively. Meanwhile, a gain margin of -19.34 dB and a phase margin of 69.45° were obtained. The LDO regulator exhibited the PSR value of -54.92 dB at 1 kHz. The total layout area for the proposed design was 52.60 x 56.20 μm^2 . Therefore, the proposed LDO regulator is suitable to be implemented in a low voltage power management system.

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