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ALL-DIGITAL PHASE LOCKED LOOP (ADPLL) TOPOLOGIES FOR RFID SYSTEM APPLICATION: A REVIEW

S. N. Ishak[a], J. Sampe[a*], Z. Yusoff[b], M. Faseehuddin[c]

[a]Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia (UKM), 43600 Bangi, Selangor, Malaysia
[b]Faculty of Engineering, Multimedia University, Jalan Multimedia, 63100 Cyberjaya, Selangor, Malaysia
[c]Department of Electronics & Telecommunication, Symbiosis Institute of Technology, Symbiosis International [Deemed University], Lavale, Pune, Maharashtra 412115, India

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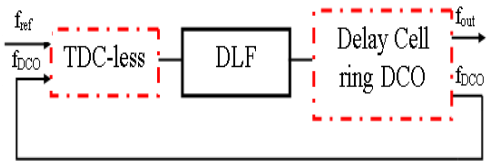
*Corresponding author
jahariah@ukm.edu.my

Graphical abstract



Abstract

An all-digital phase locked loop (ADPLL)-based local oscillator (LO) of RF transceiver application such as radio-frequency identification (RFID) system has gained popularity by accessing the benefits in complementary metal-oxide semiconductor (CMOS) process technology. This paper reviews some state-of-art of the ADPLL structures based on their applications and analyses its major implementation block, which is the digital-controlled oscillator (DCO). The DCO is evaluated based on its CMOS scaling and its performance in ADPLL, such as the power consumption, the chip area, the frequency range, the supply voltage, and the phase noise. Based on the review, the reduction in CMOS scaling decreases the transistor size in ADPLL design which leads to a smaller area and a low power dissipation. The combination of the time-to-digital (TDC) and the digital-to-time converter (DTC) that is used as the phase-frequency detector (PFD) in ADPLL is proposed to reduce the power and phase noise performance due to their high linearity design. The delay cell oscillator is found to consume more power at higher operating frequency, but it has an advantage of having less complexity and consuming less power and area in the circuit compared to the LC tank oscillator. For future work, it is recommended that an ADPLL-based LO of RFID transceiver with lowest voltage supply implementation is chosen and the use of the TDC-less as the PFD is selected due to its small area. While for the DCO, the delay cell will be designed due to its simpler implementation and occupy small area.

Keywords: All-digital, phase-locked loop, digital-controlled oscillator, radio-frequency identification, delay cell

Abstrak

Fasa gelung terkunci semua-digit (ADPLL) berasaskan pengayun tempatan (LO) bagi aplikasi pemancar-penerima RF seperti sistem pengenalpastian frekuensi radio (RFID) telah mendapat populariti dengan mendapat faedah dalam teknologi proses semikonduktor oksida-logam pelengkap (CMOS). Kerja ini mempersembah kaijan semula mengenai struktur ADPLL berdasarkan aplikasinya dan analisis mengenai perlaksanaan blok utama iaitu topologi reka bentuk pengayun terkawal digit (DCO) yang dinilai berdasarkan penskalaan CMOSnya dan prestasinya dalam ADPLL, seperti penggunaan kuasa, kawasan cip, julat frekuensi, voltan bekalan, dan hingar fasa. Berdasarkan tinjauan, pengurangan penskalaan CMOS mengurangkan saiz transistor dalam reka bentuk ADPLL yang menghasilkan kawasan yang lebih

kecil dan pelesapan kuasa rendah. Kombinasi antara penukar masa-ke-digit (TDC) dan penukar digit-ke-masa (DTC) yang digunakan sebagai pengesan frekuensi-fasa (PFD) dalam ADPLL dicadangkan untuk mengurangkan kuasa dan prestasi hingar fasa kerana reka bentuk kelelurusannya yang tinggi. Pengayun sel lengah didapati menggunakan lebih banyak kuasa pada frekuensi operasi yang lebih tinggi, tetapi kebaikannya adalah strukturnya yang ringkas, kurang menggunakan kuasa dan menempati kawasan yang kecil berbanding dengan penggunaan pengayun tangki LC. Untuk kajian di masa depan, LO berasaskan ADPLL pemancar-penerima RFID dengan pelaksanaan bekalan voltan terendah adalah dipilih dan penggunaan kurang-TDC sebagai PFD dipilih kerana kawasannya yang kecil. Sementara untuk DCO, sel lengah akan direkabentuk kerana pelaksanaannya lebih mudah dan menempati kawasan yang kecil.

Kata kunci: semua-digit, fasa gelung terkunci, pengayun digit terkawal, pengenalpastian radio-frekuensi, sel lengah

1.0 INTRODUCTION

Over the last few years, the interest in Radio Frequency Identification (RFID) system in research and industry fields have been developed and extensively used in healthcare and biomedical field [1]–[3], environment and building smart monitoring [4], tracking and localizing system [5]–[7], e-commerce management system [8], card management system [9], payment transaction [10] and other applications. This RFID technology system is a replacement of the conventional bar-code identification owing to its advantages such as real-time identification of a number of objects [11]. Figure 1 depicts a general RFID system that consists of three modules: a reader, a tag, and a host unit (computer). The system's intent is to transfer identification data/information between the reader and the tag through the RF transceiver in order to perform specific applications based on the data stored in the tag [12].

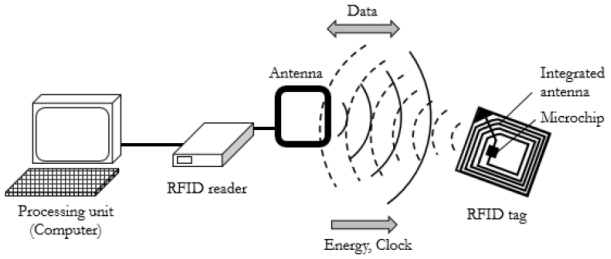


Figure 1 RFID System [12]

To date, the reported operating frequencies for RFID system are at 13.56 MHz of High Frequency (HF) communication band [13], the Ultra High Frequency (UHF) communication band that operates between 860 to 960 MHz [14], at 2.4 GHz [15], and 5.8 GHz for satellite application [16]. Each operating frequency is developed based on their suitable applications. Subsequently, current development of the RFID system is aiming for a low power device and a better data communication transfer. For examples, T. Norliza *et al.* designed an energy harvesting circuit in [12] by using hybrid input sources of energy to address the limitation of semi-active RFID tag lifespan issue due to the battery required to power the circuitries and J. Sampe *et al.* in [17] introduced a new technique of fast detection for the RFID system. Due to the advancement of the complementary metal-oxide semiconductor (CMOS) technology process, Christian *et al.* in [18] developed transceiver frontend chip for the passive RFID tag in industrial, scientific and medical (ISM) band while maintaining the power consumption performance. In the transceiver, the phase-locked loop (PLL) is an essential block for the local oscillator to generate frequency tuning range and normally the PLL comprises of a phase detector, a filter, and a voltage-controlled oscillator (VCO). However, with the advancement of CMOS technology process, the conventional PLL is no longer able to fulfill the requirement of the advanced transceiver [19]. Instead of a conventional mixed-signal PLL, all-digital format is proposed by research works in [20], [21] into the PLL in order to increase the performances of the local oscillator for the transceiver in terms of a low power consumption, an improved phase noise performance, a smaller chip area and have a low cost. Hence, this work reviews on a state-of-art of the all-digital phase locked loop (ADPLL) and its crucial block, which are phase frequency detector (PFD) and digital-controlled oscillator (DCO) scheme that will be compatible for future RFID system.

2.0 ALL-DIGITAL PHASE LOCKED LOOP STATE-OF-ART

Some RFID transceivers are built-in with the conventional PLL oscillator as reported in [18], [22], [23]. ADPLL has become popular among the researchers due to its advantages as compared to the analog counterpart such as the low power consumption and its smaller size. Other than the fast locking advantage, ADPLL is also easy to design and

implement, has increased stability, and has a better jitter performance [24] over the conventional PLL. ADPLL's main block configuration is similar to the conventional PLL, but its circuitry is purely in the digital format. The digital phase detector or the time-to-digital converter (TDC), the digital filter and the digital-controlled oscillator (DCO) are part of the ADPLL instead of the analog phase detector, the analog filter and the VCO that part of the conventional PLL's building block. In this part, the state-of-art of the current ADPLL will be reviewed based on the suggested application and its crucial blocks will be investigated.

An early modified ADPLL architecture was proposed by Motorola in 1995 [25]. They found that the half digital PLL (DPLL) needs longer time to lock the phase and the frequency. Besides, the manufacturing of the resistor and capacitor (RC) values in the LPF of the DPLL is very challenging. Hence, an ADPLL frequency synthesizer in [24] is designed to reduce the lock time. In 2005, R.B. Staszewski *et al.* designed the first ADPLL frequency synthesizer [26] for GSM/EDGE transceiver of the mobile phone and achieved a better phase noise performance as compared to their previous ADPLL work for Bluetooth as reported in [27]. Not only a good frequency-synthesizer was used, ADPLL had also provided a better performance in the microprocessors as its clock generation [24], [28].

C. Chung *et al.* in [29] proposed the ADPLL design for smart sensing applications by introducing two mode of operations of supply voltage to reduce voltage headroom issue and frequency estimation algorithm technique at cyclic TDC-embedded DCO block. This is to optimize the efficiency process of energy in various modes. The proposed ADPLL in this work is be able to compute the DCO control code with high accuracy and achieved fast settling time. With the energy-efficient performance, the proposed ADPLL consumes less power, and it is suitable for battery-powered system. C. W. Chang *et al.* in [30] used dynamic voltage for the power management unit (PMU) block in their ADPLL design. The PMU block is be able to reduce up to 39% of the power consumption of the circuit with minor PMU overhead. However, the proposed ADPLL only suitable for near-threshold operations. Meanwhile, F. Kuo *et al*. [31] proposed an ultra-low-voltage ADPLL that is powered from a single 0.5V supply voltage with a dc-dc converter that will double the supply. The DCO is connected directly to the single supply, while the double value of supply voltage will be connected to other digital circuitries.

Y. H. Tu *et al.* in [32] introduced a multi-phase scheme at the TDC and the DCO blocks in the ADPLL design. The multi-phase outputs are reused in a sampled clock of TDC, which can reduce occupied area. As the results, high operational frequencies are achieved by the proposed multi-phase DCO, while high timing resolution is obtained by the proposed multi-phase TDC. J. Bae *et al.* in [33] proposed an ADPLL design using a low supply voltage and includes the combination of a PFD and a controller loop topology to control the phase and frequency to achieve a stable output. Meanwhile the adopted delta-sigma modulator with a DCO is used to achieve high frequency resolution and a small number of capacitors. The phase selector block is designed after the DCO block which reduces the phase error and resulted faster settling time. Moreover, low phase noise performance in the proposed ADPLL is realized by a resistive biasing technique and weak-inversion operation. Y. Ho and C. Yao in [34] introduced a phase-frequency error compensation technique in their designed ADPLL. The compensation technique of the phase error and frequency error in the ADPLL are working simultaneously and fulfilled the fast-acquisition requirement.

2.1 Digital Phase Frequency Detector (DPFD)

The digital phase frequency detector (DPFD) is the first block in an ADPLL that measures the difference of the phase and the frequency of the input signal, which is the reference signal and the output signal of the DCO. One of the most popular methodology to build a DPFD is using time-to-digital converter (TDC). The advantage of the TDC is to measure the time difference between the two separate signals with good resolution [35]. Y. Balcioglu and G. Dundar [36] presented a new quantization noise suppression method to improve the noise performance in the TDC in order to achieve superior jitter performance. In this design, good jitter performance of the ADPLL is achieved and the occupied area is small. However, the proposed ADPLL is still consumed a large power. The Intel researchers consists of R. Levinger *et al.* [37] presented the ultra-low power ADPLL by interpolating the TDC block. The TDC integration is introduced to support the performance of the LC DCO bank.

However, some researchers found that the full range of TDC used may degrade the performance of the ADPLL due to its power hungry. T. Siriburanon *et al.* in [38] used the ADC with the voltage-domain digitization instead of a full range of TDC that produced a limited resolution of the phase digitization and dissipated a large power. While in [39], Y. Wu *et al.* maintained the used of the TDC, but the circuit is assisted by the addition of DTC in order to achieve a low in-band phase noise. This study is supported by H. Liu *et al.* in [40] which their DTC-assisted TDC achieved a high linearity phase detector. Besides that, the DTC-assisted TDC resulted in a high-resolution noise shaping. The other research that supported the DTC-TDC based is in [41] by N. Yan *et al.* that used phase prediction algorithm to minimize the detection range of the TDC. The $\Sigma\Delta$ dither block is designed to improve the nonlinearity of the DTC.

A few techniques are introduced to improve the power consumption of the ADPLL. As an example, a

reduction of a full-ranged TDC has been proposed in [42] by using the fractional TDC architecture. The proposed design consumed less power and occupied smaller area. J. K. Sahani *et al.* in [43] proposed the DPFD architecture which includes the high resolution TDC by calibrating the process-voltage-and-temperature (PVT) variation to enhance the jitter performance. The dynamic bang-bang PFD is used to improve the locking time performance. The use of the TDC with bang-bang PFD has also been used in [44] where the design achieved a higher resolution performance and a faster locking time. Table 1 shows the summary of the advantages and the disadvantages for the PFD design topologies in various ADPLL.

Table 1 The phase-frequency detector in various ADPLL

Ref	PFD	Advantages	Disadvantages
[37]	Full-TDC	• High resolution	• High power
[38]	ADC	•High resolution •Low power	
[39], [40], [41]	TDC with DTC	•Low in-band phase noise •High linearity •High resolution noise shaping	• More area needed
[42]	TDC-less	•Low power consumption •Save area consumption	• Resolution may degrade
[43]	TDC with bang-bang PFD	•High resolution •Low jitter and low power •Fast locking time •PVT robust	• More area needed

2.2 Digital Loop Filter (DLF)

Besides the phase-frequency detector block, the digital loop filter (DLF) is another challenging block to design in the ADPLL. Researchers W. Yang *et al*. in [45] proposed the phase self-alignment mechanism and the dynamic loop gain control in their digital loop filter (DLF) of the ADPLL. The phase self-alignment is proposed to resolve the overdamping caused by a large loop gain controller (K_I) in the DLF and to reduce the locking time of the ADPLL. The proposed design has reduced the locking time by 91% compared with conventional PLL. This design exhibited a superior performance in terms of locking time and the jitter performance, and suitable for the sub-GHz Internet-of-Things (IoT) band applications. M. Sayadi and E. Farshidi [46] introduced a new approach for the loop filter design by proposing a model predictive control (MPC) method. The proposed method achieved a faster transient response and the model can be designed to eliminate the noise sources that come from the oscillator without degrading the phase noise performance.

2.3 Digital-controlled Oscillator (DCO)

Furthermore, the design of DCO is one of the current interests among the researchers. As in the conventional PLL, the VCO is the heart and most critical design part. It is because the VCO's output frequency has a direct impact on the timing accuracy where phase alignment is required and the signal-to-noise ratio (SNR) frequency translation is performed [47]. This output frequency will affect the jitter and phase noise performance in the design as well as the power consumption in the transceiver. While in ADPLL, the DCO is used to perform the digital-to-frequency conversion [26]. The DCO, which was first reported in [48], designed for the RF wireless applications. The DCO lies at the heart of the ADPLL-based frequency synthesizer that acts as a local oscillator for the transmitter and the receiver. The DCO deliberately avoids any analog tuning controls. Similar to the VCO in the PLL, the DCO is the most power hungry circuit in the ADPLL [49].

2.3.1 LC-DCO

The basic of the LC-based DCO depicts as in Figure 2, which is comprised of the voltage supply, the LC tank, a pair of CMOS cross-coupled transistors, the varactors, the constant bias transistor, and a pair of inverters. The optimization of the phase noise performance can be done by putting an LC filter in parallel with the constant bias transistor [50] in order to transfer the noise signal to the ground. The use of this method needs an additional inductor to increase the impedance of the constant bias transistor at the oscillation frequency. The drawback of this method that it will increase the chip size and it will affect the inductor in working at the resonant frequencies. To solve the problem, the work in [51] added two MOS transistor at the top constant bias to optimise the phase noise performance. These two MOS transistors imposed the triode mode to the DCO, and the flicker noise has reduced as compared to the use of the normal transistor bias, which only operated in one mode. While in [52], the inductor-less technique is used in the LC tank, which resulted in less area consumption.

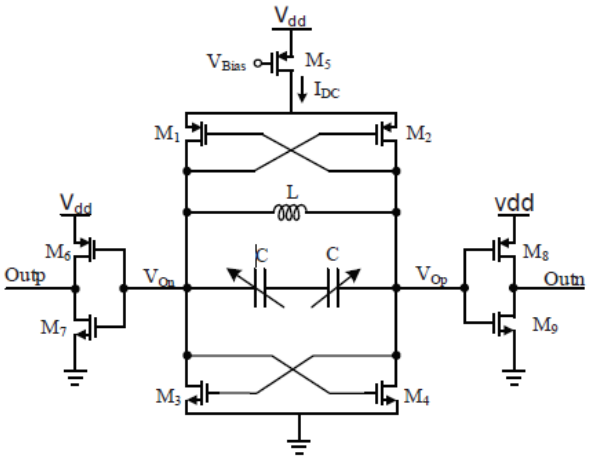


Figure 2 LC-DCO schematic [51]

Power consumption can be improved if the LC factor is increased. Y. Wang *et al.* in [53] presented an ultra-low power 1-bit DCO with a high quality factor capacitor and inductor to minimize the loss in the LC tank. In this case, the value of the capacitor and inductor must be well designed. However, the increase of the LC factor can increase the transistor size that leads to a large area. Other than that, the decrease of the voltage supply may also help the performance of the power consumption in the DCO. Work in M. Moreira *et al.* [54] proposed a low power cross-coupled LC-tank DCO by reducing the voltage supply down to 0.4 V in order to restrict the power consumption. The technique of downsizing the voltage supply is a critical challenge it may degrade the performance of the phase noise. To solve this problem, the transistor would be designed with an increased width size which to reduce the flicker noise. Unfortunately, the increase in the width of the transistor will occupy large area.

2.3.2 DCO (DAC+DCO)

Based on the literature, one approach in the DCO design is by the combination of the digital-to-analog converter (DAC) and the traditional VCO. Two separate designs of the DAC and the VCO are needed to ensure that the performance of the DCO can achieve flexibility and stability. The advantage of this DCO is straight-forward, which the usage of the DAC is to convert the phase error in digital format to the voltage form and drive the varactor in LC VCO to change the frequency. However, the big challenge of this approach is the head room issue due to the DAC works in the voltage domain. To overcome this problem, L. Lou *et al.* has proposed a continuous wide tuning range and a low phase noise of flexible DCO in [55].

E. Szopos *et al.* presented in [56] cascaded the DAC and the VCO to build a DCO block. The frequency lock time and jitter performance (two conflicting metrics) are mainly affected by the DCO resolution; thus a trade-off compromise should be sought when choosing the resolution. The jitter versus the resolution characteristics is an aid for the designer to choose the proper resolution for example, 0.1 ps jitter needs to use 18-bit DCO.

2.3.3 MOS Varactor

In the past work, the capacitor used in the LC tank oscillator of the VCO is a passive type. With the advancement of the CMOS process technology, the MOS varactor or the active capacitor are widely chosen due to its low power consumption and it occupied a small size area. The MOS varactor is varied by the control voltage. As the graph shown in the Figure 3, the increase of the control voltage will decrease the capacitance of the MOS varactor. Due to that, the MOS varactor is suitable for tuning in the LC-VCO circuit. The MOS varactor type, either NMOS or PMOS, is selected based on their design requirement. Based on P. Solanki *et al.* in [57] the NMOS varactor is chosen due to its weighting characteristic in terms of the small area, the wide tuning range and the low power consumption. However, according to L. Lou *et al.* [55] and M. S. Sadr *et al.* in [51], the NMOS varactor has high sensitivity to the noise due to the fabrication process. Hence, the PMOS varactor is highly recommended for a better noise performance and has less parasitic capacitance.

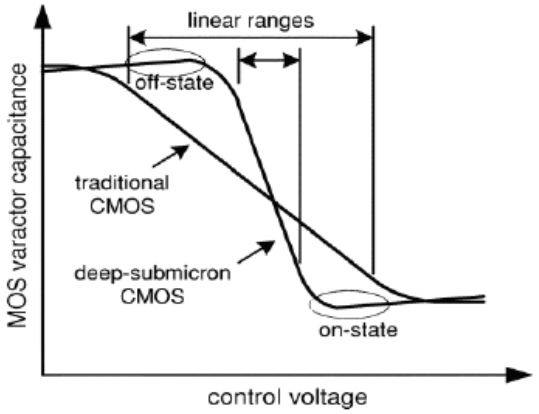


Figure 3 MOS varactor capacitance characteristics in CMOS [51]

2.3.4 Inverter or Delay Cell DCO

Besides the LC-tank approach, the delay cell with several stages can be used as the DCO. Typically, the inverter-based DCO is comprised of the PMOS and the NMOS transistors for each stage. Figure 4 below shows the conventional DCO with several stages or can be called as the ring DCO. The inverter introduces short time delay for each stage or delay cell and the needs of the inverter stage is depending on the design requirement [58].

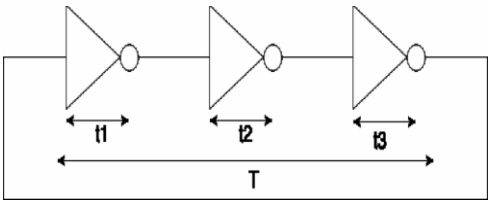


Figure 4 The conventional of DCO ring topology [58]

S. Dabas and M. Kumar in [59] added the NMOS transistors as the switching network which control the DCO bit and placed them in between the supply voltage and the CMOS inverter delay stage. The resistance posed by the switching network and the inverter offered by each stage is determined by the input vector applied which in turn determines the DCO output oscillation frequency. From this study, the use of the inverter stage will affect the performance of the power consumption and the output frequency range.

S. Pahlavan *et al*. in [60] introduced a differential ring oscillator with a delay element for the DCO that can work at two different frequency bands and is powered by the digital selection mode. The design achieved a lower and a higher power consumption at a lower and a higher frequency band respectively. Thus, this proposed design may only be suitable for low frequency multi-standard applications.

C. Yuan *et al.* in [61] presented a 2-stage differential ring oscillator with an inverter-based delay cells, a resistor-triode load and a weak cross-coupled latch cell to cancel the power supply noise. The proposed technique does not require the analog design and does not reduce voltage headroom. This technique minimally affects the phase noise only at large frequency offset, where its contribution to the integrated jitter is minimal. A proof-of-concept prototype DCO can withstand 50 mVpp excursions on the supply with less than 10% frequency pushing.

D. Sheng *et al*. in [62] presented a delay cell with the NAND gate approach as shown in Figure 5. The proposed multi-stage design is not only occupied a smaller silicon area, but also has a higher delay resolution. Furthermore, because the proposed design can migrate to a different process easily, it can decrease the design turn-around-time and the design effort significantly. As a result, it is very suitable for system-level integration and System-on-Chip (SoC) applications.

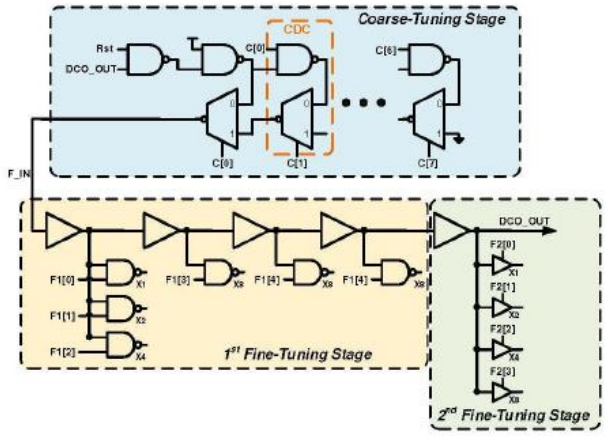


Figure 5 NAND gate approach of delay cell [62]

P. Bisiaux *et al.* in [63] presented the five stages differential amplifiers as the inverters or the delay cells and a bias circuit with a stable voltage output as shown as Figure 6. This design preferred delay cells based on differential current logic instead of voltage logic to minimize power supply variation noise. The hybrid of the binary to thermometer code block and the frequency control block (FCB) in this proposed design has achieved a high resolution and has minimized the mismatch effect.

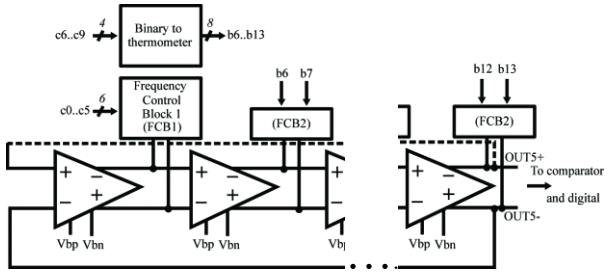


Figure 6 The five stages differential amplifiers delay cells [63]

S. Selvaraj *et al.* in [64] proposed a DCO by using four delay cells with a cross-coupled inverter architecture to improve the phase noise and jitter performance. The DCO composed of the combination of the DAC and the ring oscillator along with the output differential buffer as shown as Figure 7. The proposed design achieved high stability, high efficiency and, wide operating frequency range performance, and also the ability to generate multi-phase signals. The state-of-art of the DCO scheme is summarized as shown as Table 2 by differentiate the advantages and its design challenge.

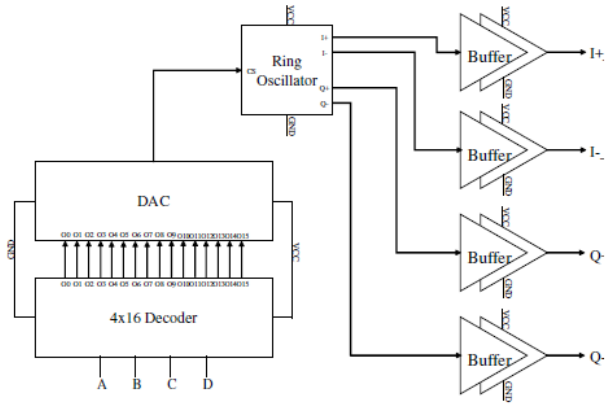


Figure 7 S. Selvaraj *et al*. proposed the DCO design in [64]

3.0 DISCUSSION

Generally, an ADPLL consists of a phase detector, a loop filter and a controlled oscillator with all-digital format. Recently, various designs are approached by numerous researchers in order to improve performance of the local oscillator in terms power consumption, phase noise, chip area, and cost. Based on the reviewed literature, the CMOS scaling is the most challenging design stage for the local oscillator because the circuit has to minimize to nanometres size. The component has to be designed meticulously in order to maintain the local oscillator performance.

The advantages and the applications of the state-of-art ADPLL are shown in Table 3. The reported ADPLLs are conducted from 2016 to 2020. From the Table 3, there are two major blocks that have been approached, which is the PFD and the DCO blocks. The use of the TDC as the phase detector is gaining popularity due to its simpler design and easier implementation. However, some researchers found that the full range TDC used can cause higher power consumption. The combination of the DTC with the TDC is proposed to reduce the power consumption and to increase the phase noise performance due to their high linearity in the design. The other approach of PFD design, the TDC-less such as in [42] and the combination of bang-bang PFD with TDC such as in [43] are quite impressive since both approaches offered less power consumption and smaller occupied area.

Table 2 The summary of the DCO advantages and challenges

Ref	DCO state-of-art	Advantages	Challenges
[50] [51] [52] [53] [54]	LC DCO	• Low power consumption. • Good phase noise performance.	• Large LC factor and transistor size increase chip size. • Proper value of LC is needed to design. • Difficult to design.
[55] [56]	DAC with LC VCO	• Straight forward flow design. • Low phase noise • Wide tuning range	• Head room issue • Need proper parameter on resolution design
[51] [55] [57] [65]	MOS Varactor	• Low power consumption • Occupy small area. • Suitable for LC-VCO circuit and inverter/delay cell.	• High sensitivity to the noise.
[59] [61] [62] [63], [64],	Inverter or delay cell	• Decrease design effort • High resolution • Minimize mismatch effect • High stability and high efficiency • Wide frequency tuning	• High power consumption at high operating frequency

Table 3 ADPLL review

Year, Ref	ADPLL state-of-art	Achievement	Application
2016, [29]	Dynamic supply voltage Frequency estimation TDC-embedded DCO	• Fast settling time • High energy efficiency • Low power consumption • Small chip area	Battery-powered smart sensing device
2016, [30]	Dynamic supply voltage	• Fast lock-in time • High efficiency • Low power consumption • Small chip area	Low-voltage system
2016, [32]	Multi-phase scheme technique at TDC and DCO	• Save area • Low power consumption at high frequency	Low-voltage system

Year, Ref	ADPLL state-of-art	Achievement	Application
2016, [33]	The combinational of PFD with controller. Delta-sigma modulator DCO Phase interpolator as filter	• Low power consumption • High stability • High frequency resolution • Fast settling time • Low phase noise	Medical implantable transceiver (MICS)
2016, [34]	Phase-frequency-error compensation technique	• Improved jitter performance • Fast acquisition time	Dynamic frequency scaling
2016, [38]	ADC used instead of TDC	• Low power consumption. • High resolution of phase digitization	Internet-of-Things (IoTs) device
2016, [46]	Model predictive control (MPC) loop filter	• Fast transient response	Wireless system
2017, [31]	Switched-capacitor doubler	• Low voltage supply is needed. • Low power device	Bluetooth low energy
2017, [39]	DTC-assisted TDC	• High resolution noise shaping • High linearity • Low band noise	RF system-on-chip (SoC)
2018, [40]	DTC-assisted TDC	• Occupied small area • Good jitter performance • Low power operation	BLE, Zigbee. And WPAN/WBAN
2019, [37]	Interpolating TDC and LC tank DCO	• Ultra-low power • Occupied small area • Good jitter performance	802.11ac standard
2019, [41]	DTC-assisted TDC	• Good in-band phase noise • Improved jitter performance • Reduced locking time	Narrow-band IoT
2019, [42]	Capacitively boosted differential ring oscillator DCO, TDC-less	• Ultra-low area • Low power consumption	Biomedical implant SoC
2020, [43]	Foreground LMS algorithm-based calibration method	• Low power • Low jitter • PVT robust	SoC and battery-powered high-speed applications

The DCO design is more crucial as compared to the phase detector because the DCO is the heart of the ADPLL system. Table 4 shows a list of the DCO cores of the ADPLL and their performance reported from year 2016 to 2020. Commonly, there are two types of the DCO approach: LC tank and delay cell based. The selection of DCO type is based on the desired performances. From Table 4, the performance of the DCO is evaluated by the CMOS scaling technology process, the frequency tuning range, the supply voltage, the power consumption, the figure-of-merit (FoM) and the occupied area. Based on the reviewed, LC tank oscillator is widely used by many researchers as compared to the delay cell element because of its better phase noise performance. Nevertheless, the frequency tuning range of LC tank is limited, and meticulous design is needed. Research works in [51] and other LC tank work need some specific value of LC in order to design the LC tank based on the desired frequency tuning range. This means that the LC tank oscillator is not flexible as changing the oscillation frequency will require redesigning the circuit again. Opposite to the delay cell based DCO, which can produce large frequency tuning and it is easy to design but it consumes more power at high frequency range. In 180 nm CMOS technology at low frequency range, LC tank DCO work in [57] offered almost 30% better power consumption when compared to delay cell work in [60]. However, the time to design the delay cell unit is saved, which decreases the design complexity compared to LC tank. D. Sheng *et al*. in [62] has been presented a multi-stage delay cell which is not only occupied 0.0018 mm^2 die area, but also has a higher delay resolution. In addition, the proposed design can be moved to a different process easily, as well as decreases the design time and the design complexity significantly.

In terms of area, the LC oscillator occupied more area compared to delay cell oscillator. We can see

from the Table 4, in 65nm CMOS technology, the delay cell-based DCO used in work [64] offered very small occupied area when compared to LC tank-based DCO used in [50]. Work research in [54] offered the lowest voltage supply for DCO circuit and followed by [53] and [61] which used supply less than 1 V. The voltage supply is another design challenge because the low supply can reduce the power consumption of the device. Energy harvester circuit is another option to power up the local oscillator. Hence, the limited power supply can be saved up more.

Table 4 DCO review

Year, Ref	DCO core	CMOS (nm)	Freq. Range. (GHz)	Supply (V)	Power (mW)	FoM (dBc/Hz)	Die Area (mm^2)
2016, [51]	LC tank	90	10 – 10.7	1.2	4.9	-189	n/a
2016, [55]	LC tank	65	13.69 – 15.93	1.2	16.5	-169.6	n/a
2016, [60]	Delay cell	180	1.39–1.452	1.8	10.1	n/a	n/a
2017, [66]	LC tank	28	39.3 – 42.9	1.0	10.5	-180	0.08
2018, [57]	LC tank	180	2.28 – 2.74	1.8	6.33	n/a	0.03
2019, [50]	LC tank	65	5.2 – 5.8	1.2	2.52	-183.77	0.28
2019, [52]	LC tank	130	1.8 – 2.6	1.1	5.3	-150	0.003
2019, [53]	LC tank	65	74.1 – 76.7	0.75	3.15	164.62	0.056
2019, [54]	LC tank	40	1.8 – 1.86	0.4	0.38	n/a	0.46
2019, [61]	Delay cell	65	0.9 – 1.4	0.85	2.45	n/a	0.0189
2019, [67]	LC tank	180	12.4 –12.6	n/a	n/a	n/a	n/a
2020, [62]	Delay cell	180	0.16 – 0.346	1.8	0.525	n/a	0.0018
2020, [63]	Delay Cell	28	1.13 – 1.54	1.0	0.84	-135.5	0.0056
2020, [64]	Delay cell	65	1.8 – 2.2	1.2	1.6	-219.2	0.00037

4.0 CONCLUSION

An ADPLL for the RF transceiver becoming popular among researchers due to the benefits of the CMOS technology process. In this work, the state-of-art of the ADPLL is reviewed based on its performance in terms of the design configuration and its suitable application. Based on the state-of-art ADPLL, the low voltage supply has improved the power consumption performance of the application. As for the PFD, the used of the TDC-less technique can reduce the power consumption and the die area. Furthermore, the DCO design is the more critical as compared to PFD. Hence, the review had focused on the current design topologies development of the DCO based on the type of the DCO core, either the LC tank or the delay cell element, the power performance, and the die area. It is found that, the selection of the DCO type is depending on the application design requirements. The LC DCO can give lower phase noise performance, but the design is more complex. As for a simpler and easier design, the delay cell element can be adopted in the DCO. However, the design challenge of the delay cell DCO is to maintain the low power consumption at high operating frequency. The delay cell DCO also can achieve wide tuning frequency ranges as compared to the LC DCO. Thus, for the future work of the local ADPLL RFID transceiver, the low voltage supply should be considered, and the TDC-less phase detector should be adopted to achieve smaller area and lower power consumption. The delay cell should be designed for the DCO for because of its simpler implementation and it consumed smaller area while maintaining the low power consumption at high operating frequency.

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