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EVOLUTION OF DISCRETE SEMICONDUCTOR COPPER WEDGE BOND IN BIASED TEMPERATURE HUMIDITY CHAMBER

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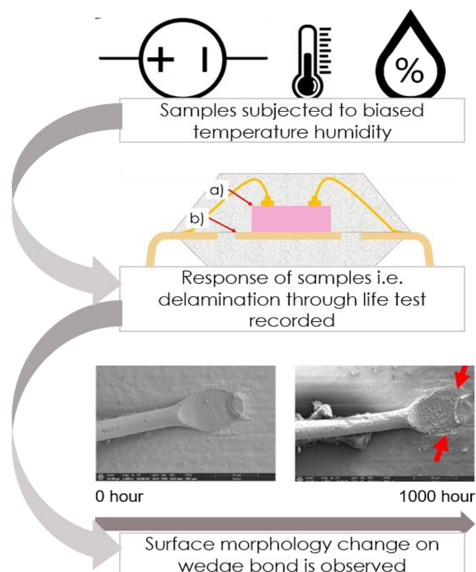
Graphical abstract



Abstract

The ability to provide electrolyte required in a corrosion process; and its role in facilitating the reaction is widely attributed to humidity. Although corrosion typically develop over time; its symptoms may start showing up much earlier- commonly in the form of degradation. This paper aims at documenting the symptoms- particularly surface morphology of Copper (Cu) wire in discrete semiconductor component as it evolves in a stress-accelerated environment of temperature-humidity chamber. Results gathered from the trial runs show tendencies of Cu wire to degrade in the said environment, with noticeable changes observed on Cu wire wedge bond morphology after completion of 1000 hours in temperature-humidity chamber. Apart from better understanding of how discrete semiconductor with Cu wire behaves in highly demanding end applications like automotive, data obtained also shed some light on the need to reduce probability of material degradation thru better process control and optimization; ultimately in addressing package integrity.

Keywords: Cu wire, morphology, temperature-humidity chamber, corrosion, discrete semiconductor

Abstrak

Kelembapan biasa dikaitkan dengan kakisan kerana keupayaannya untuk memudahkan tindak balas dengan menyediakan elektrolit yang diperlukan proses itu. Walaupun kakisan boleh mengambil masa untuk berkembang, ia biasanya didahului oleh gejala degradasi seperti perubahan pada morfologi permukaan. Objektif makalah ini ialah untuk mengkaji perubahan pada wayar kuprum komponen semikonduktor diskret dalam persekitaran dipercepat-tegasan oleh kebuk suhu-kelembapan. Terbukti daripada keputusan bahawa morfologi permukaan wayar kuprum mempunyai kecenderungan untuk mengalami degradasi apabila tertakluk kepada persekitaran dipercepat-tegasan, dengan perbezaan yang ketara dalam morfologi sambungan baji selepas 1000 jam dalam kebuk suhu-kelembapan. Ujian ini memberikan gambaran tentang kelakuan produk semikonduktor diskret berwayar kuprum dalam aplikasi melampau seperti automotif, dan menyerlahkan kepentingan pengoptimuman proses dalam memaksimumkan integriti pakej dan meminimumkan kebarangkalian

perubahan kritikal dalam bahan daripada berlaku.

Kata kunci: wayar Kuprum, morfologi, kebuk suhu-kelembapan, kakisan, semikonduktor diskret

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1.0 INTRODUCTION

Wire bonding, with 90% domination in integrated circuit (IC) packaging is the most commonly employed IC interconnect technology in the market. This is far ahead of other interconnect alternatives like wafer-level package, tape automated bonding and flip-chips [1, 2, 3]. While this is largely due to its flexibility, the are also other factors that drive this including very matured and well-established eco-system, not only from equipment readiness and materials availability standpoint, but also in terms of skilled manpower.

As far as wire bonding material, Gold (Au), with its highly reliable nature, has been the primary choice since the very beginning of semiconductor manufacturing days [4, 5, 6, 7, 8]. However, more wire bonding material alternatives like Copper (Cu) and Aluminum (Al) have been made available to provide competition to Au [9, 10]. This is in line with the progress in material science, driven primarily by cost reduction activities. Besides Cu and Al wires, the use of Cu clip as interconnect has also been developed for certain product types; while some manufacturers opted for a hybrid apprach by combining clip and wire in a package. Other than cost, good device performance; namely conductivity, surge current capability and stray inductance are some of the key advantages of Cu clip [11].

Cu wire, with lower overall cost is widely used as alternative for Au wire in discrete semiconductor component. Besides cost, this is also largely due to good compatibility with legacy Au wire devices design; from bond pad dimension, package footprint, pitch size, as well as wire looping clearance requirement, as opposed to options like Al wire or Cu clip; which are known to be more rigid [12]. In addition to that, there are also reports of better thermal and electrical properties in Cu as compared to Au wires, including higher conductivity by around 25%, and subsequently improved power rating and heat dissipation [13]. There are however some critical challenges to reliability of Cu wire products despite these advantages. This includes its higher tendency to degrade in conventional molding compounds; especially when halides are present [14].

Degradation of performance in discrete semiconductor is typically associated to products being used in highly demanding environment, as found in automotive with extreme thermal application in various climates. Some of the products would degrade and fail sometimes instantaneouly, and some others would be seen with electrical or physical signs of degradation before their eventual failure. Objective of this paper is to document surface morphology changes for Cu wire in discrete semiconductor in accelerated life test environment; subjected with electrical biasing and high temperature as well as relative humidity to replicate conditions in end applications. Besides observations of surface morphology, delamination is also a key indicator in this study to understand its relationship with evolution of surface morphology; both of which will be monitored at each life test interval.

2.0 MATERIALS AND METHODOLOGY

Manufacturing of a semiconductor component begins with fabrication of intended integrated circuit (IC) on a Silicon die. This takes place after Silicon wafers take their shape from an ingot. Fabrication process involves various materials, such as Boron (B) and Phosphorous (P) for P and N region, respectively; Oxide (O_2) for insulation, as well as Aluminum (Al) and Cu for contacts thru diffusion, implantation and etching processes, performed repeatedly.

Wafers will be subjected for probe testing upon completion of circuit fabrication; and this is performed either on the entire wafer or on sampling basis of certain area on a wafer. Failed dies are to be inked out from this process, in mapping software or physically so they are not picked up in subsequent assembly steps. To address the manufacturability aspects of the assembly process, a back-grinding process may sometimes be necessary; where wafers are thinned down by grinding and polishing to certain thickness. In some cases, this is also critical in optimizing electrical performance of a device.

Wafers will be sent for assembly next, with the very first step being wafer saw. In this process, wafers are sawn into individual piece of standalone functioning die. To enable this process and prevent any sawn die from flying off, wafers were first mounted on a sticky tape with metal ring. Wafer saw process is then followed by die attach process on a leadframe thru the formation of conductive eutectic alloy to enable contact to the substrate, which is an active terminal for the device. Die attach process may also be performed by other means, depending on the requirement of end products [15]. For example, solder attach is typically found in power packages to efficiently handle big current, while logic gate devices on the other hand used non-conductive epoxy since the substrate is not an active terminal.

Wire bonding process, where interconnections are made between attached die and the leadframe is performed next. In this process; active terminals of the device are connected with Cu wire with ball bond on the die and wedge or stitch bond on the leadframe. Completed unit with die and wire bond is then encapsulated with epoxy mold compound to protect both the fragile die and wire before they are sent for lead plating with Tin (Sn) to aid for solderability [16]. Final assembly step is trim and form; followed by electrical test.

Figure 1 below shows summary of assembly process steps; with the samples taken only once testing is completed. This is to ensure only good samples are taken for the study and essentially eliminates infant mortality failures to prevent misleading results and consequently maintain integrity of analysis performed.

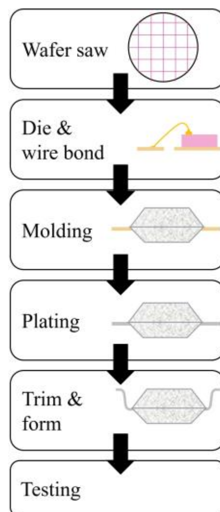

Figure 1 Process flow of semiconductor assembly

To establish good baseline for the samples, an engineering lot was built for this purpose with minimum variation in the raw materials used. Starting sample size for the study was 600 pieces, all to be eventually subjected to accelerated life test for 1000 hours, or an equivalent of 41 days.

High Humidity High Temperature Reverse Bias (H3TRB), listed as Test 9 in Automotive Electronics Council's AEC-Q101 document for qualification test definition [17] is the life test chosen for this study, and is performed to evaluate reliability of non-hermetically sealed packaged IC devices in humid environment. It is also known as Reverse Bias Tropical (RBT) or Steady State Temperature Humidity Bias Life Test, and is also governed by JEDEC's JESD22-A101C, Steady State Temperature Humidity Bias Life Test Standard. In this test, a combination of temperature, humidity and biasing are used to accelerate penetration of moisture through the package and the metallic conductors [18]. To enable this test, it is a pre-requisite to have the chamber capable of maintaining intended temperature and relative humidity continuously throughout ramping up and down process, while concurrently supplying electrical biasing required for the devices under test per the stipulated conditions.

Table 1 below lists conditions of life test as used in this study, with device-dependant biasing voltage applied at 80% of rated reverse voltage for the device.

Table 1 Life test conditions used

Test Condition	Unit
Temperature	85°C
Relative Humidity	60%
Bias voltage	V_{CE}: 48V V_{EB}: 1V

To enable analysis at area of interest; proper removal of mold compound is crucial to ensure analysis area and the surrounding components are adequately exposed and preserved. This is also to minimize noises and ensure accurate observations are made, considering the nature of physical degradation expected, and its extent. For this reason, the use of chemical decapsulation; typically, with HNO_3 and H_2SO_4 is strictly prohibited. Mechanical decapsulation on the other hand, although is free of chemicals- is not favorable due to the risk of inducing physical damages to the fragile components in the sample like wire bond and Si die. With chemical and mechanical decapsulation being ruled out for the aforementioned reasons, only laser ablation technique is therefore considered as viable to properly prepare the samples for this study. This is a process of removing epoxy mold compound by means of vaporization through the use of high-power laser. As it is capable of vaporizing epoxy mold compound with good efficiency; leaving very little or no residues and leftovers, no further finishing or cleaning is required for most cases in exposing target area for further analysis.

Package delamination check is performed with Sonoscan D6000 Scanning Acoustic Microscope (SAM), using C-scan. Unlike Thru-scan, C-scan is useful for open interfaces where signals are allowed thru without obstruction, and the feedback signals containing acoustic impedance information of the interface are reflected back to the receiver. 50MHz transducer is used for the package of interest in this study, based on its thickness and internal structure. While interfaces to scan are die and leadframe to epoxy mold compound. Scanning of good reference samples is required prior to analyzing actual samples to establish a baseline for subsequent scanning. As for the gain, amplitude value in the range of 60-70% is typically considered as adequate in obtaining good signal to noise ratio. Amplitude beyond this range might produce images with saturated white area, potentially leading to loss of important details at scanned area. It is also imperative that the

samples are baked for 2 hours at 100°C prior to the analysis; to reduce or eliminate moisture inside the package, while also ensuring comparable baseline condition for all samples. As samples are completely submersed in water bath throughout this analysis, absorption of water by the mold compound becomes inevitable. Therefore, scanning process is kept within 5 minutes as prolonged submersion in the water may lead to alteration of samples' condition through excessive absorption of water by the package. Results obtained from the analysis will then be analyzed with a pixel-based delamination quantification software based on the assigned color as defined by the reference color bar in SAM software. This reference color bar is used to indicate amount of delamination present; with the threshold defined during initial setup of the equipment using a standard sample. Threshold setting for SAM analysis is shown in Figure 2 below and is standardized across all package type for consistency purposes. White color on the bar indicates highest relative amplitude, where no significant negative changes in acoustic impedance are recorded between 2 materials at an interface, or in other words, no delamination. As acoustic impedance is heavily influenced by each material's density- no significant shifts in acoustic impedance is typically expected at any of the interfaces; unless with presence of air or moisture- both of which have very low density and are commonly associated with a delamination event. With this, any point with amplitude of -30% or less will be assigned with a color on the left region of the bar, with red being the lowest.

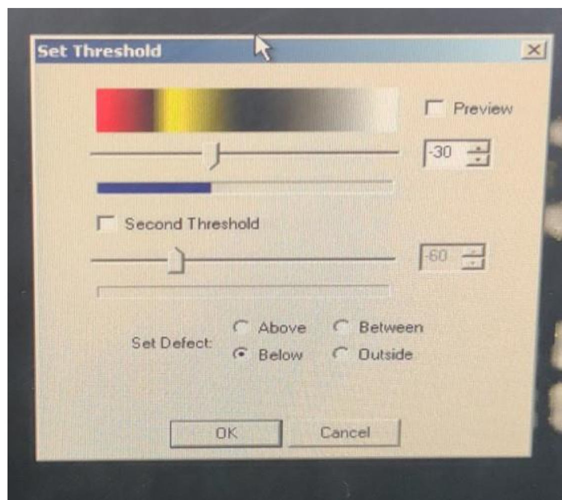

Figure 2 Snapshot of threshold setting in SAM

Next is surface morphology analysis, where samples are to be analyzed first with Leica S8AP0 metallurgical microscope at 10x magnification and bright field illumination. This first inspection serves to check for presence of defects or anomalies on the samples that may hinder accurate interpretation of surface morphology while also making sure that the target area has been sufficiently prepared for further analysis. Improperly prepared samples: for instance, with mold compound remnants still present at area of interest or mechanical damages induced at target area from sample preparation will require a rework; else outcomes will likely be inaccurate. Once samples are verified as good; analysis will continue with Scanning Electron Microscope (SEM) for detailed imaging. Equipment model used in this process is Apreo from FEI; with magnification of up to 1500x. As with other analysis processes, a baseline result is first established with a known good sample. This will be used as reference in subsequent scanning of the samples throughout all intervals of H^3TRB life test. In doing the imaging, acceleration voltage used falls in the range of 3kV to 10kV; to address variations in surface morphology severity, therefore ensuring no details are missed out in the process. Should a significant change in surface morphology is recorded in the process, corresponding area will also be examined to better understand roles of assembly components like mold compound and leadframe in the event. To further safeguard integrity of the outcomes, it is made mandatory for analysis to be carried out within 24 hours after samples are prepared. This is to avoid further degradation of the samples through oxidation or contamination. Figure 3 below shows image of an adequately prepared sample, ready for analysis.

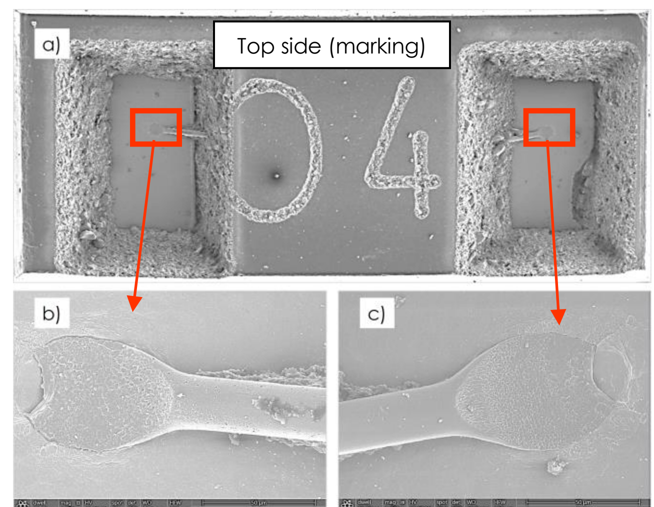

Figure 3 Electron microscope images of a properly prepared sample with, a) Overview and b), c) close up at the wedges

3.0 RESULTS AND DISCUSSION

Typical interfaces of interest for SAM analysis are shown in Figure 4 below, first is die top and followed by leadframe top, both interfacing with epoxy mold compound. Leadframe to epoxy mold compound, where the wedge bond is sitting, is the interface of interest in this study. While die top scanning is used to screen for any possible anomalies on the samples

possibly induced during the life test. While delamination is generally not favorable at any of the interfaces, interpretation of the impact needs to be done separately for each area; primarily due to the structure of the product.

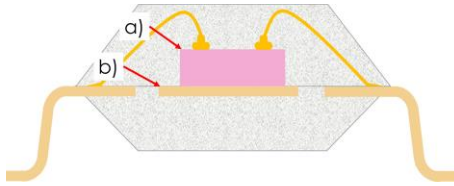

Figure 4 Simplified cross-sectional diagram of the sample and interfaces of interest for SAM, a) die to mold compound and b) leadframe to mold compound

Results obtained from SAM analysis performed is shown in Figure 5, with delamination area observed to be steadily increasing from approximately 24% to over 50% at 48 and 1000 hours, respectively. It is evident that the delamination is present predominantly at die attach pad, while no significant amount of delamination is recorded at lead area where the wedge bond is. For validation purposes, in some instances it may be necessary to perform mechanical cross-sectioning as well as electron imaging at the area; considering known limitation of SAM technique to detect delamination at sub-micron scale. In some other cases, decapsulation is also performed to understand an area of interest better; especially as mechanical cross-section is only able to provide 2-dimensional view of an area.

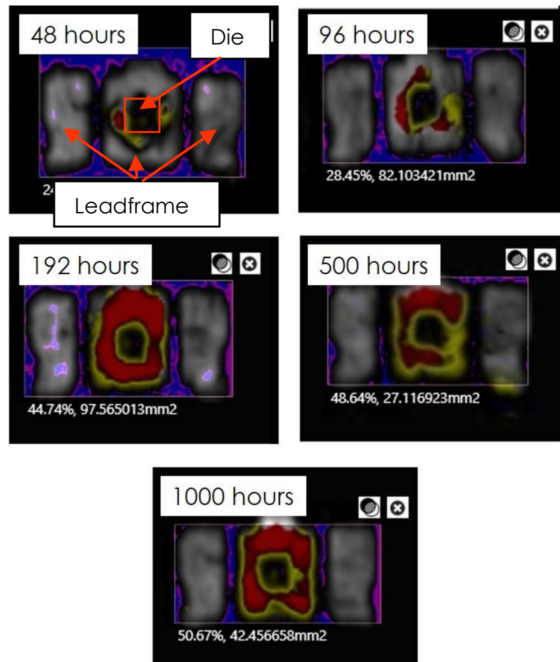

Figure 5 Sample SAM images with computed delamination area at all intervals.

Wedge bond or stitch bond is formed on Cu leadframe, after first ball is formed on die bond pad in the form of ball bond. Cu leadframe area where wedge bond is intended to land is plated with Silver (Ag) to aid in forming good attachment at the area. This is the area of interest, mainly due to its proximity with external lead; and therefore, its susceptibility to impact of delamination at leadframe to mold compound interface. Gap resulting from leadframe and mold compound delamination could lead to chemical ingression- subsequently accelerating degradation of assembly component in the vicinity, particularly the wedge bond. Figure 6 below shows diagram of wedge bond and physical aberration expected as samples are subjected to accelerated life test. Red region in the diagram shows area on the wedge expected with aberration, eventually expected to be consumed through the intervals of life test.

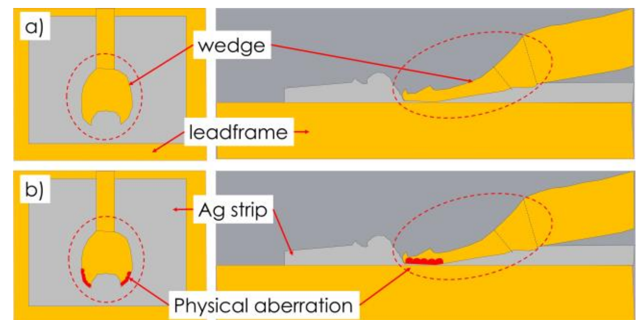

Figure 6 Schematic diagram for Cu wire wedge at, a) 0hr, and b) after life test, with dotted circle showing area of interest

Wedge bond, particularly its base as shown above is the target region for degradation to take place. This is due to its location being on Ag-strip of Cu leadframe; with both materials being good candidates to complete an electrochemical reaction along with the presence of an electrolyte. This electrolyte could either be introduced by chemical ingression through the surface of leadframe, or from the epoxy mold compound as widely reported [16, 19-20], which requires no degradation to the samples' physical condition for it to be present in the package.

Careful consideration needs to be made when choosing acceleration voltage for surface morphology analysis, taking into account various magnitude of morphology changes; some of which are very surface and therefore needs to be analyzed with lower acceleration voltage, typically in the range of 3 to 5kV. Use of higher acceleration voltage in such instances might lead to loss of surface details; ultimately jeopardizing interpretations of results obtained. Appropriate acceleration voltage also helps greatly in better documenting progress of degradation on the samples throughout the life test. Additionally, samples are not to be coated for SEM;

to minimize noises at analysis area as much as possible. This is despite charging effects expected from non-conductive materials on the samples, especially the mold compound. In addressing this, optimization of SEM parameters is often necessary to minimize charging effects; for instance, the use of lower spot size and beam current. Also, it is always a good practice to check for any sign of damages on the samples; whether they are induced during sample preparation or are pre-existing from assembly but not sufficiently severe to cause failure during testing. This is to make sure observations made are genuinely relevant to the life test conducted. Some instances of such failures include capillary mark on wire bond, which very often appears like a scratch throughout wire bonding loop and could be confused for surface degradation on the wire.

Electron imaging obtained on the samples in Figure 7 below showed changes in surface morphology beyond 500 hours. These changes can be identified with deformation at edge of wedge, as shown in Figure 6 b) earlier. This observation suggests that the presence of electrolyte at wedge base is likely in acting as a catalyst for the electrochemical reaction.

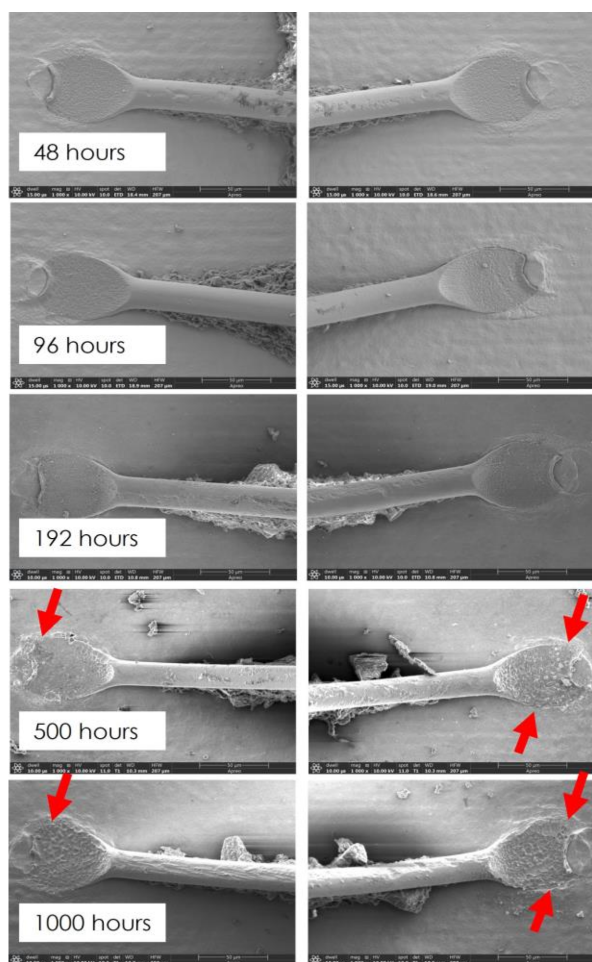

Figure 7 Electron images of wire bond at wedges through 1000 hours. Sign of degradation observed at 500 hours onwards in the form of consumed edges as pointed by red arrows

Significant changes in surface morphology beyond 500 hours is consistent with degradation in package delamination observed with SAM. Although no significant delamination was seen at lead area where the wedges are placed; steady overall increase in delamination is still a valid signal showing degradation in package condition- with further confirmation can be done through mechanical cross-section. Understanding this relationship could assist in shedding lighter on the effect of temperature-humidity chamber to changes in wire bond surface morphology.

4.0 CONCLUSION

Results obtained from this trial clearly show tendencies of Cu wire to degrade, as manifested thru surface morphology change at 1000 hours of accelerated life test with temperature and humidity; accompanied with SAM results showing worsening delamination. Steady increase of delamination over the life test interval also suggests possible relationship with degradation of Cu wire wedge bond from 500 hours onward, while also suggesting possible source of electrolyte from outside the package. These results provide important hints in gaining better understanding of Cu wire semiconductor products' behavior in highly demanding applications like automotive, aerospace and military. They also highlight the importance of assembly process optimization in improving package robustness and integrity to ultimately minimize probability of critical degradation on any internal component in the products, particularly Cu wire in this case.

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