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DEVELOPMENT OF DUAL-SWITCHES BRIDGELESS PFC TOTEM-POLE SEPIC CONVERTER FOR LED DRIVER APPLICATION

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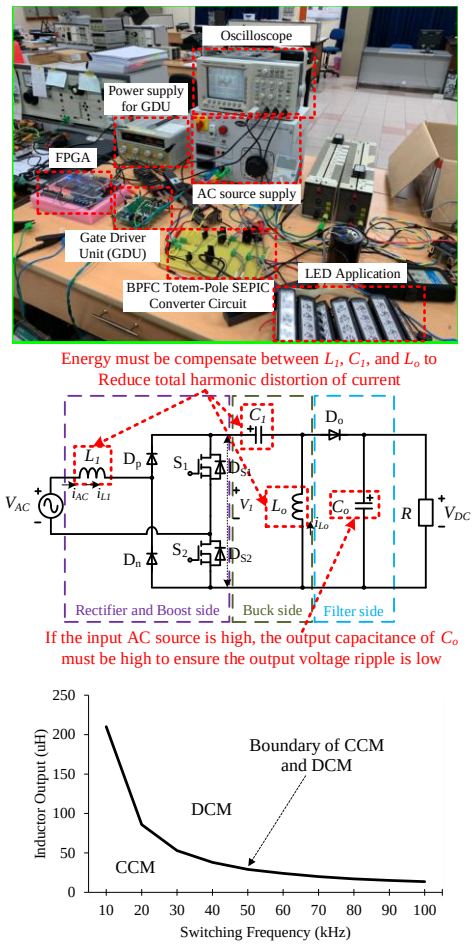
Graphical abstract



Abstract

This paper presents a Dual-Switch Bridgeless Power Factor Correction (DSBPFC) Single Ended Primary Inductor Converter (SEPIC) with Totem-Pole circuit structure for LED Driver Application. The conventional Full-Bridge Rectifier (FBR) SEPIC converter has five diodes, four in the rectifier bridge and one in the SEPIC. In addition, the FBR SEPIC converter has several drawbacks, including low power factor (PF), high current harmonics (THDi), and high output voltage ripple, due to the combination of two operation circuits in a single converter structure. The proposed DSBPFC SEPIC converter with Totem-Pole method improves PF and reduces THDi and output voltage ripple compared to the conventional FBR SEPIC. Additionally, it only requires three diodes instead of five. The optimization parameter design minimizes the THDi and output voltage ripple. In addition, to improve the quality of the AC source, the inductors are designed to operate in DCM and CCM based on the ripple-balancing concept between input and output inductors. As to reduce output voltage ripple, a high capacitance of output capacitor is used. The simulation result of the THDi is 3.8% whereas the experimental result shows that the THDi is 23.5%; which can be attributed to the parasitic elements at the passive components. Furthermore, the experimental results of the output voltage ripple are 2 V with output capacitance of 3300 µF, compared to the output voltage ripple of 4.40 V for 470 µF. Therefore, the proposed converter's design is confirmed with an output power of approximately 14.4 W.

Keywords: SEPIC converter, Bridgeless PFC, Totem-Pole design, PF, THD_i, output voltage ripple

Abstrak

Kertas kerja ini membentangkan *Dual-Switch Bridgeless Power Factor Correction (DSBPFC) Single Ended Primary Inductor Converter (SEPIC)* dengan struktur litar *Totem-Pole*. Penukar *Full-Bridge Rectifier (FBR) SEPIC* mempunyai empat diod di jambatan dan satu diod pada penukar *SEPIC*. Walau bagaimanapun, gabungan dua operasi litar dalam satu struktur penukar mempunyai akibat daripada isu kualiti kuasa. Beberapa kelemahan utama *FBR SEPIC* ialah faktor kuasa yang rendah (*PF*), jumlah ganguan harmonic arus yang tinggi (THD_i), dan riak voltan keluaran yang tinggi. Oleh itu, struktur *DSBPFC SEPIC* dengan kaedah *Totem-Pole* dicadangkan untuk mengurangkan THD_i, sambil meningkatkan faktor kuasa dan mengurangkan riak voltan keluaran. Di samping itu, penukar yang dicadangkan memerlukan hanya tiga diod berbanding dengan *full-bridge SEPIC* dengan lima diod. Reka

bentuk parameter pengoptimuman digunakan untuk memastikan THD_i dan riak voltan keluaran diminimumkan. Selain itu, untuk meningkatkan kualiti sumber AC, pengaruh direka bentuk untuk beroperasi dalam DCM dan CCM berdasarkan konsep pengimbangan riak antara pengaruh masukkan dan keluaran. Parameter reka bentuk penukar yang dicadangkan telah disahkan. Keputusan simulasi THD_i ialah 3.8% manakala keputusan eksperimen menunjukkan bahawa THD_i ialah 23.5%; yang boleh dikaitkan dengan komponen parasit pada komponen pasif. Tambahan pula, keputusan eksperimen riak voltan keluaran ialah 2 V dengan nilai pemuat keluaran 3300 µF, berbanding riak voltan keluaran 4.40 V untuk 470 µF. Oleh itu, reka bentuk penukar yang dicadangkan disahkan dengan kuasa keluaran kira-kira 14.4 W.

Kata kunci: Penukar *SEPIC*, PFC tanpa jambatan, Reka bentuk *Totem-Pole*, *PF*, THD_i, riak voltan keluaran

1.0 INTRODUCTION

Most people are now aware of LEDs' or light-emitting diodes' long shelf life and energy efficiency, as a result of increasing energy regulations. LEDs are semiconductor devices that emit light when an electric current flows across them. LED drivers are specialised devices necessary for the operation of these innovative light sources. LED drivers, also referred as LED power supplies, resemble fluorescent lamp ballasts or low voltage bulb transformers. Harmonic pollution is a significant problem that arises with conventional rectifiers [1]–[4]. Harmonics produced by these devices are limited by the International Electrotechnical Commission (IEC) 61000-3-2 [5]–[7]. Power-factor-correction (PFC) converters are used for AC-DC conversion in order to comply with standards.

Certain power application systems require an AC power source for input. To meet a variety of load requirements, rectifiers and DC-DC converters are used to convert AC to DC. While a bridge rectifier, transformer, inductor, and capacitor can generate a distortion-free DC output voltage, it frequently produces highly distorted input currents. Therefore, AC-DC conversion is critical in PFC converters to maintain purely sinusoidal waveforms for both input voltage and current sources. Several circuit topologies have been developed for PFC applications, including boost, buck-boost, SEPIC, and Cuk converters.

Four diodes are found in the rectifier while one is found in the SEPIC converter of a full-bridge SEPIC converter, which results in high THD_i, low power factor, and high output voltage ripple [8]–[17]. Hence, in order to mitigate this issue, a traditional bridgeless SEPIC converter is proposed. A conventional bridgeless SEPIC converter able to deliver high power over a large voltage range. Without inversion, the output voltage of the SEPIC converters can be decreased or increased [18]–[26]. Therefore, buck-boost converters such as single-ended primary-inductor converters (SEPIC) and Cuk converters have been applied.

In addition, BPFC Totem-Pole SEPIC converters is propsed to contribute into this study is to reduce the THD_i, while improving the power factor and reducing the output voltage ripple. Optimization parameter design is used to reduce THD_i and output voltage ripple. Furthermore, to improve the quality of the AC source, inductors are designed to operate in both DCM and CCM modes, with input and output inductors balancing the ripple. To reduce output voltage ripple, a high-capacitance output capacitor is used. Proposed Dual-Switch BPFC SEPIC converter using three diodes instead of five diodes in the full bridge rectifier SEPIC to convert AC to DC sources and stepped-up and stepped-down output voltages. This proposed converter produces the THD_i below the (IEC) 61000-3-2 standard (5%). The proposed converter also produces the output voltage ripple less than 10% of the output voltage.

2.0 METHODOLOGY

This methodology presents mode of operation of BPFC Totem-Pole SEPIC converter, principle and characteristics of proposed structure, and parameter design.

A conventional PFC SEPIC circuit structure that uses four diodes as a bridge is shown in Figure 1. D_p acts as a forwards biased during positive-half cycle while D_n acts as a reverse-biased. During negative-half cycle, D_n acts as a forwards biased during negative-half cycle while D_p acts as a reverse-biased. In this case, this converter can achieve a unity power factor due to the D_p and D_n are blocked current during current returning path when the cycle changes. Once the cycles are complete, the SEPIC receives inconstant DC and produces pure DC. This converter can produce pure output DC as the output capacitor, C_o filters output voltage ripple. The full-bridge rectifier SEPIC can step-up and step-down the voltage by controlling the duty cycle by using switch, S. Input inductor, L_1 is used to store energy while output inductor, L_o is used to filter the current which can reduce harmonic current. Besides, input

capacitor, C_1 is used to control resonant frequency and output diode, D_o is used to control output voltage DC always in positive polarity.

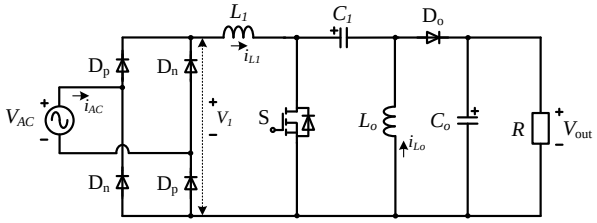


Figure 1 Conventional PFC SEPIC circuit structures

Furthermore, compared to the full-bridge, the BPFC Totem-Pole SEPIC converter uses two active switches and two diodes as shown in Figure 2.

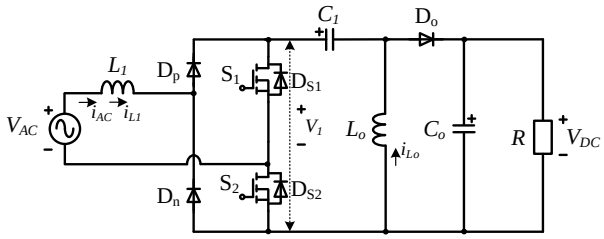


Figure 2 BPFC Totem-Pole SEPIC circuit structures

The switches are used to control and rectify the bridgeless AC to DC sources. Besides, the bridgeless is divided into two frequencies which are line frequency and switching frequency. As a result, this circuit is in an abnormal state in which the energy from the input is transferred to the output using two frequencies. This condition causes the charging and discharging of energy of components to be symmetrical during positive-half and negative-half cycles. The BPFC Totem-Pole SEPIC converter circuit, as shown in Figure 3, is investigated for the positive-half cycle structure, and duty cycle for switches S_1 and S_2 are same. As shown in Figure 3 (a)-(b), the circuit operating in a positive-half cycle of a switching period T_s can be divided into two operating modes, which can be defined as follows:

Mode 1: When the switches, S_1 and S_2 are T_{ON}, the input inductors, L_1 are charging and discharging and positive diode, D_p is always forward-biased during positive-half cycle. The output inductor, L_o is charging while the input and output capacitors, C_1 and C_o are discharging. During this interval, the output diode, D_o is in reverse-biased condition. The current is not flowing to the output as it is blocked by the output diode. Thus, the load receives the energy from the output capacitor as shown in Figure 3 (a).

Mode 2: When the S_1 and S_2 are T_{OFF}, the L_1 and L_o are discharging while the C_1 and C_o are charging. At the time, the output diode is in forward-biased condition, so the current is flowing from the input to the output. The diode of MOSFET, D_{S2} is forward biased for current returning path as shown in Figure 3 (b).

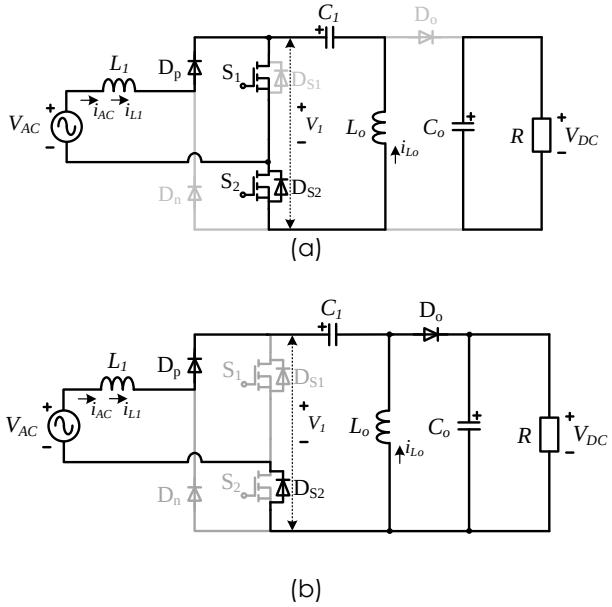


Figure 3 Mode of Operation of BPFC Totem-Pole SEPIC circuit structures (a) Mode-1 and (b) Mode-2

A full-bridge uncontrolled rectifier commonly uses four rectifying diodes connected in a closed loop "bridge" structure to produce the desired output voltage with inconstant DC. The major purpose of this bridge circuit is that it has the probability of not requiring the use of a special centre tapped transformer, as shown in Figure 1. Thus, the size and cost can be reduced. The inconstant DC output voltage is produced due to the diodes bridge that act as forward-biased and reverse-biased during positive-half and negative-half cycles as shown in Figure 4. This structure achieves approximately a unity *PF* as the voltage and current are in-phase and crossing at zero point.

Besides, the Bridgeless Totem-Pole PFC uses two standard diodes, one inductor, and two MOSFETs as shown in Figure 2. The circuit has the main advantage of using only a single-switch to control the circuit during positive-half and negative-half cycles. The chopped DC voltage output is produced due to the MOSFET is turned-on and turned-off depending on the duty cycle and switching frequency. The slow diodes act as a forward-biased and followed the path of the positive-half and negative-half cycles as shown in Figure 5. The inductor is used to boost the chopped DC output and to balance the energy between positive-half and negative-half cycles. Thereby, this structure achieves approximately a unity *PF* where the voltage and current are in-phase at the crossing at zero point.

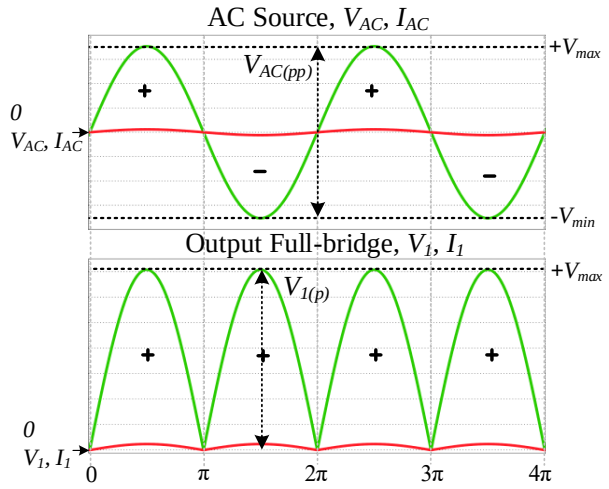


Figure 4 Output waveform of full-bridge

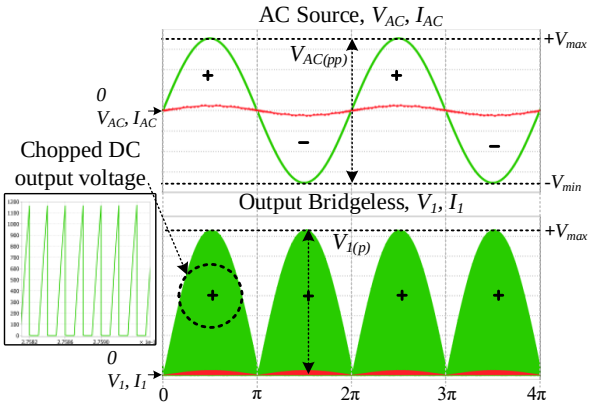


Figure 5 Output waveform of bridgeless Totem-Pole

Figure 6 shows the characteristics of the proposed converter based on circuit structure. The proposed structure consists of three sides which are rectifier and boost side, buck side, and filter side. For the rectifier and boost side, the input inductor L_1 acts as boost part where the energy stored at the L_1 during positive and negative cycles. Besides, the bridgeless Totem-pole is the rectifier side where the AC source is chopped with high frequency depending on the switching frequency. Thus, the buck side acts as control energy from the AC source and component C_1 and L_o are sensitive components. The sensitive components are crucial in controlling oscillation and THD_i. Figure 7 shows the boundary of Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) of L_o. The boundary of CCM and DCM are practically used for THD_i minimization. In this case, the L_o inductance must be chosen based on the switching frequency, with a high inductance for low switching frequencies. To ensure the THD_i is less than 5%, the L_o must be in CCM. Consequently, the filter side acts as direction current for D_o and filtering voltage for C_o. The function of D_o is to ensure that the voltage and current are always positive polarity, and to reduce output voltage ripple, the capacitance of C_o must be increased.

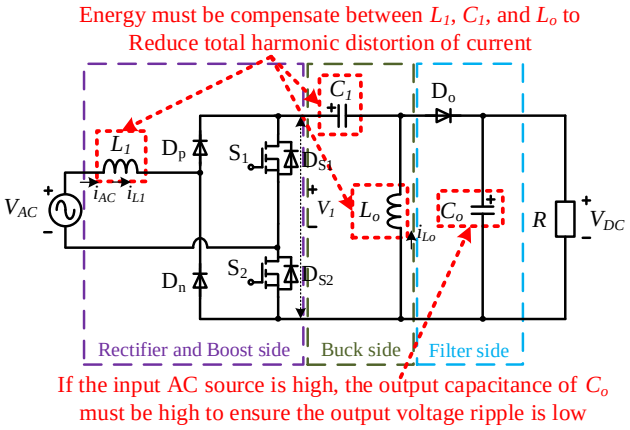


Figure 6 Characteristics of Proposed structure

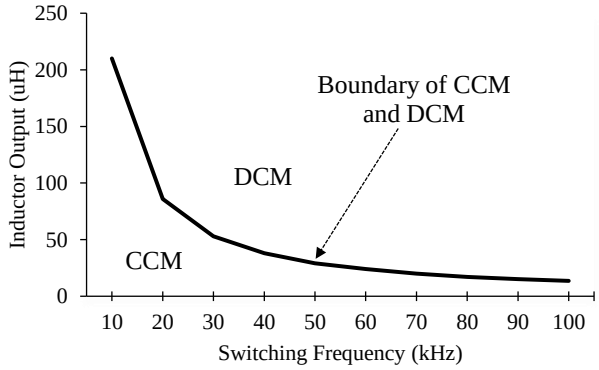


Figure 7 Boundary of CCM and DCM of output inductor

Besides, all parameter of components is estimated based on formulas in Equations (9), (11), (13) and (14). The initial parameter design of the proposed converter as shown in Table 1 is used for simulation and experimental design. The AC source of voltage in range 110 V – 240 V. The output voltage is fixed to 48 V and the resonant frequency is selected based on $F_L<F_R<F_{SW}$.

Table 1 Initial parameters of proposed converter

Parameters	Value
AC Voltage Source, V_{AC}	110 V – 240 V
DC Voltage Output, V_{DC}	48 V
Output Power, P_{out}	14.4 W
Line Frequency, F_L	50 Hz
Resonant Frequency, F_R	19.02 Hz
Switching Frequency, F_{SW}	10 kHz
Inductor current ripple, ΔI_L	<10% of input current

In terms of circuit structure parameters, the voltage conversion ratio, $M=V_o/V_M$, can be determined by using the power-balance principle where the P_{in} =

P_{AC} and assuming no losses in the converter. Equation (2) represents the average AC source current. R_e is defined as the effective input resistance and can be calculated using equation (3). The voltage conversion ratio then is calculated by evaluating the equation (2) using the equation (3) and utilizing the power balance between the AC source and DC output (4).

$$P_{AC} = \frac{2}{T}\int_0^{\frac{T}{2}} V_{AC}(t)\cdot I_{AC}(t)dt \quad (1)$$

$$I_{AC}(t) = \frac{V_{AC}(t)}{R_e} \quad (2)$$

$$R_e = \frac{2\cdot L_e}{D_{ton}{}^2\cdot T_s} \quad (3)$$

$$M = \frac{V_{DC}}{\sqrt{2}\cdot V_{AC}} \quad (4)$$

From the Equation (4), the duty cycle of the circuit structure can be decided by using the following equation (5)

$$D = \frac{M}{M+1} \quad (5)$$

The following equation can determine the Input current, I_{AC} by using the output power, P_{DC} that is given in Table 1.

$$I_{AC} = I_1 sin(\omega t) = \frac{2P_{DC}}{\eta V_1} sin(\omega t) \quad (6)$$

From the equation (5) and using the following equation the input current ripple, ΔI_L can be calculated:

$$\Delta I_L = \frac{V_{AC}(t_O)D}{L_1 f_{SW}} \quad (7)$$

The following Equation (8) can be used to calculate the output average current during a switching cycle:

$$I_{DC,avg} = \frac{V_{AC}^2(t_O)D^2}{2L_e V_{DC}} T \quad (8)$$

The input Inductor, L_1 can be calculated using the following equation,

$$L_1 = \frac{V_{AC}(t_o)D}{f_s \Delta I_L} \quad (9)$$

Using the resonance frequency range and the following equation that is given, the input capacitor can be calculated:

$$f_L < f_r < f_{sw} \quad (10)$$

$$C_1 = \frac{1}{(2\pi\cdot f_r)^2\cdot(L_1+L_O)} \quad (11)$$

From the equation of L_e and L_1, the following equation is used to find the output inductor:

$$L_e = \frac{V_1^2 D^2}{4V_{DC} f_{SW} I_{o,avg}} \quad (12)$$

$$\frac{1}{L_2} = \frac{1}{L_e} - \frac{1}{L_1} \quad (13)$$

The output ripple frequency is double the input frequency, and in worst-case scenario, the output capacitor must produce the output current during the half-period of ripple frequency. As a result, C_o can be obtained using the equation as follows, where f_L is the line frequency:

$$C_o = \frac{P_{DC}}{4 f_L . V_{DC} . \Delta V_{DC}} \quad (14)$$

3.0 RESULTS AND DISCUSSION

Figure 7 shows the experimental setup for the BPFC Totem-Pole SEPIC Converter that consists of FPGA, Power supply unit for Gate Driver Unit, Gate Driver Unit, the BPFC Totem-Pole SEPIC converter, AC source supply and oscilloscope. According to the mentioned parameters design consideration and from the following equation the initial specifications for the simulation and experimental of the proposed converter is as in the Table 2.

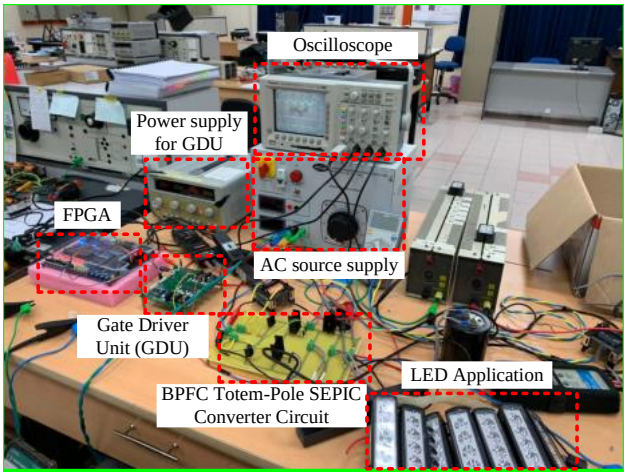
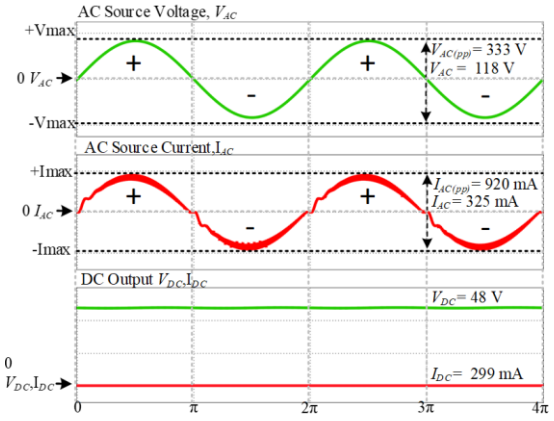


Figure 7 BPFC Totem-Pole SEPIC circuit structures experimental setup

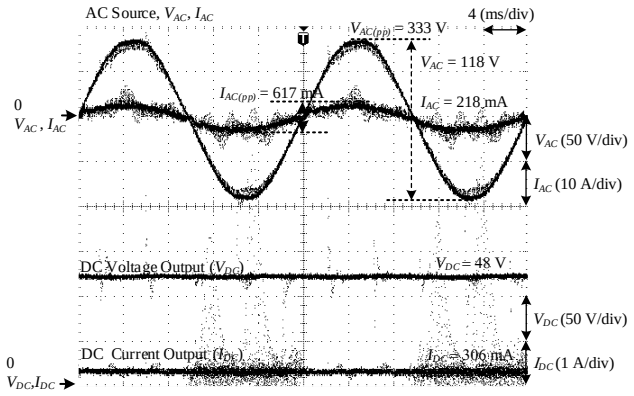
Table 2 Design parameters of proposed converter

Parameters	Value
AC Voltage Source, V_{AC}	110 V – 230 V
DC Voltage Output, V_{DC}	48 V
Output Power, P_{out}	14.4 W
Line Frequency, F_L	50 Hz
Resonant Frequency, F_R	19.02 Hz
Switching Frequency, F_{SW}	10 kHz
Resistor, R	160 Ω
Input Inductor, L_1	21 mH
Output Inductor, L_o	210 µH
Input Capacitor, C_1	0.5 µF
Output Capacitor, C_o	3300 µF

Figure 8 shows the AC sources and DC outputs for simulation and experimental results and the DC output voltage is fixed to 48 V. Figure 8 (a) and Figure 8 (b) show the AC source voltage, V_{AC} and AC source current, I_{AC} are in phase which is the *PF* is nearest to unity. From Figure 8 (a), it can be observed that the simulation results show the V_{AC} = 118 V, $V_{AC(pp)}$ = 333 V, I_{AC} = 325 mA, $I_{AC(pp)}$ = 920 mA, V_{DC} = 48 V and the I_{DC} = 299 mA. Besides, from Figure 8 (b), it can be observed that the experimental results show the V_{AC} = 118 V, $V_{AC(pp)}$ = 333 V, I_{AC} = 218 mA, $I_{AC(pp)}$ = 617 mA, V_{DC} = 48 V and the I_{DC} = 306 mA. The experimental results also have noise at the waveform, and this causes the parasitic element for components. From Figure 9 (a) the simulation results show the THD_i is 3.8%. Meanwhile, for the experimental result in Fig. 9(b) the THD_i is 23.5%. For the simulation results, Figure 9 (a) shows the input current harmonics are 3.8% below the IEC 61000-3-2 standard. Figure 9 (a) shows the input current in frequency domain. It can be observed from Figure 9 (b) that the input current harmonics are 23.5% above the IEC 61000-3-2 standard, and this can be attributed to the internal inductance in the output resistor. There is much similarity between the values of the output and the circuit model based on actual simulation and experimental result. However, there are slight differences in the $I_{AC(pp)}$ and the I_{AC}. This is because, if the circuit model based on actual parasitic component model simulation is used, it will consider the power losses that occur in the BPFC Totem-Pole SEPIC Converter circuit structure. In addition, the quality of the input current can achieve the pure sinusoidal waveform, and the THD_i can be reduced to be less than 5% when the output power is 100 W and above. This is because the energy transfer from the input of the load must compensate each other for the input and output inductors can charge and discharge efficiently.



(a)



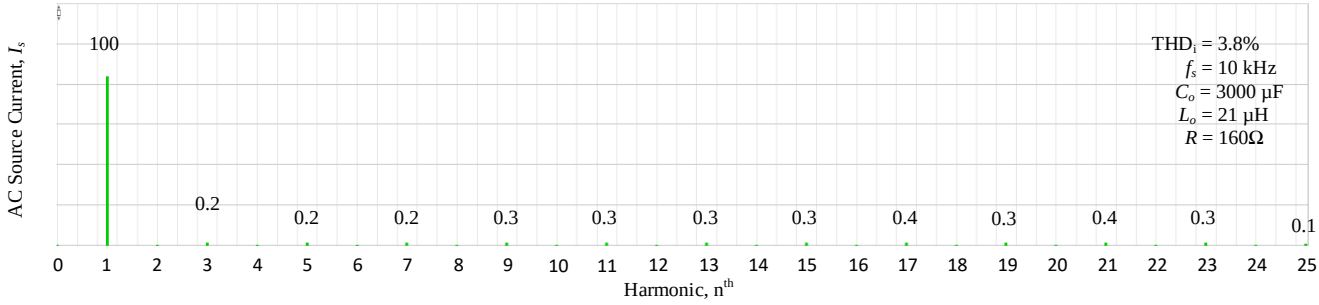
(b)

Figure 8 Output Waveform of BPFC Totem-Pole SEPIC Converter Circuit Structure (a) Simulation Result, (b) Experimental Result

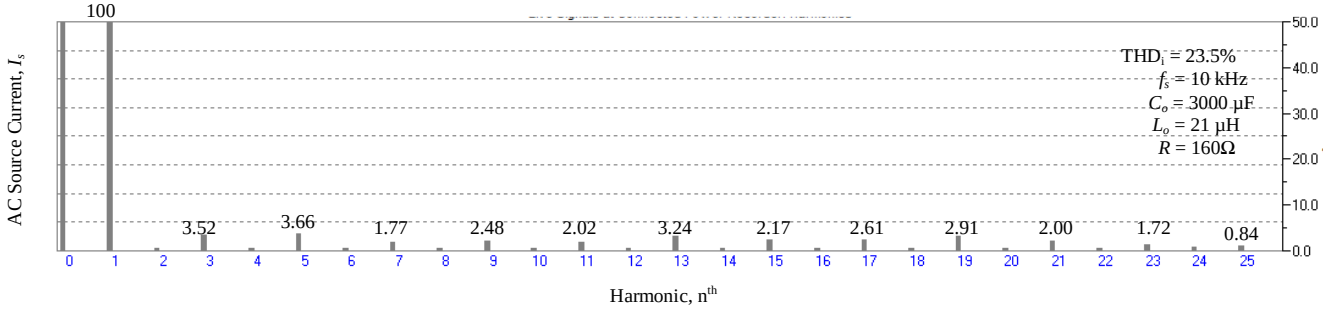
From the Figure 10 (a) it can be seen that the simulation results of the output capacitance of 470 µF show that the V_{AC} = 118 V, $V_{AC(pp)}$ =333 V, I_{AC} = 325 mA, $I_{AC(pp)}$ = 920 mA, V_{DC} = 48 V, I_{DC} = 299 mA and the ΔV_{DC} = 2.14 V.

From the Figure 10 (b) it is observed that the simulation results of the output capacitance of 3300 µF show that the V_{AC} = 118 V, $V_{AC(pp)}$ =333 V, I_{AC} = 325 mA, $I_{AC(pp)}$ = 920 mA, V_{DC} = 48 V, I_{DC} = 299 mA and the ΔV_{DC} = 0.37 V. From the Figure 10 (c) it the

experimental results of output capacitance of 470 µF show the V_{AC} = 114 V, $V_{AC(pp)}$ =325 V, I_{AC} = 207 mA, $I_{AC(pp)}$ = 588 mA, V_{DC} = 48 V, I_{DC} = 241 mA and the ΔV_{DC} = 4.4 V. From the Figure 10 (d) it can be seen that the experimental results of output capacitance of 470 µF show the V_{AC} = 114 V, $V_{AC(pp)}$ =322 V, I_{AC} = 217 mA, $I_{AC(pp)}$ = 614 mA, V_{DC} = 48 V, I_{DC} = 217 mA and the ΔV_{DC} = 2 V. Figure 10 (a) shows that from simulation of using the output capacitor of 3300 µF the output voltage ripple produced is 0.37 V while Figure 10 (b) shows from the simulation, output voltage ripple is 2.14 V from using the 470 µF output capacitor. Figure 10 (d) shows from the experiment using the output capacitor of 3300 µF, the output voltage ripple produced is 2 V and the Figure 10 (c) shows that from the experiment, the output voltage ripple is 4.4 V when the 470 µF output capacitor is used. By varying the output capacitance, the output voltage ripple can be changed. According to the circuit model based on simulation and experiment, the output voltage ripple can be increased as the output capacitor value is increased. Figure 10 (c) shows the output voltage ripple is 4.4 V at 48 V, compared to Figure 10 (d) that shows the output peak to peak voltage ripple is 2 V at 48 V. In addition, the low output voltage ripple can be achieved to be less than 10% for the converter to work properly. The output voltage ripple waveform can be reduced to 50% when using the output capacitance of 3300µF rather than 470µF. This is because the higher the output capacitance can reduce the output voltage ripple.

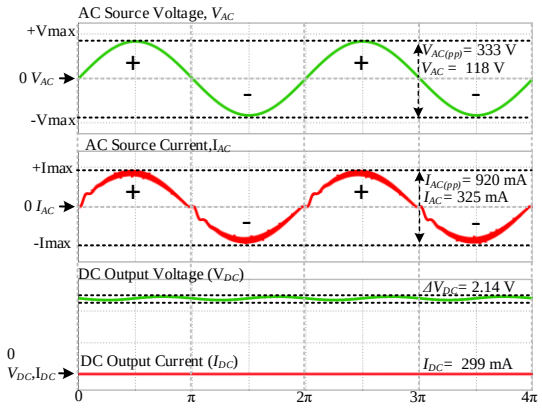


(a)

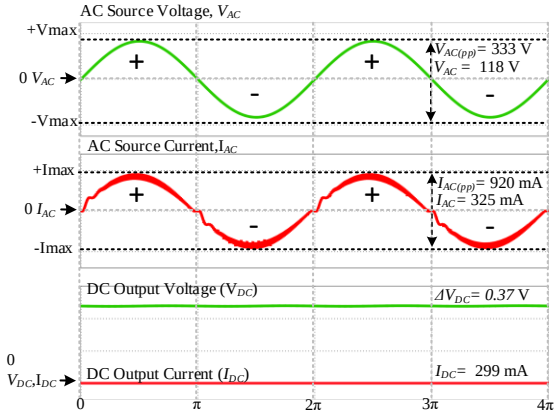


(b)

Figure 9 The *THDi* of BPFC Totem-Pole SEPIC Converter Circuit Structure (a) Simulation result, (b) Experimental result



(a)



(b)

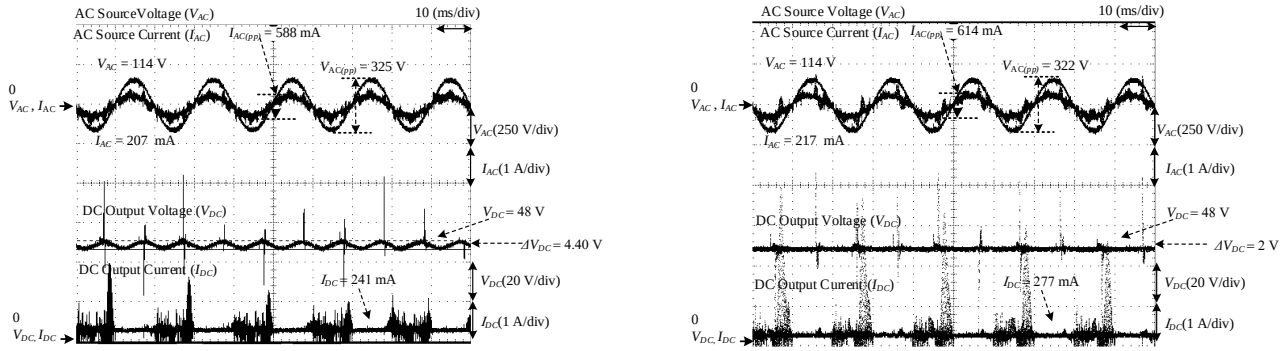


Figure 10 Output voltage ripple reduction based on (a) simulation with Co = 470 µF, (b) simulation with Co = 3300 µF, (c) experimental with Co = 470 µF, (d) experimental with Co = 3300 µF

4.0 CONCLUSION

In this paper, the BPFC Totem-Pole SEPIC Converter has been presented for power quality mitigation. The result from the simulation and the experiment shows a good agreement is met. A prototype of the BPFC Totem-Pole SEPIC converter is performed and validated with experimental results. The simulation result of the THD_i is 3.9% compared to the experimental result that shows the THD_i is 24% due to the parasitic component at the passive components. Besides, the simulation result of the output voltage ripple is 0.37 V with output capacitance of 3300µF compared to the output voltage ripple for 470 µF that is 2.14 V. Then, the experimental results of the output voltage ripple are 2 V with the output capacitance of 3300µF, compared to the output voltage ripple for 470µF that is 4.40 V. Therefore, the design of the proposed converter is confirmed with an approximate 14.4 W of output power. The experimental result of THD_i is less than 5% can be achieved when the output power is 100 W and above. Hence, in the future, a control method will be proposed for the BPFC Totem-Pole SEPIC Converter to regulate the output voltage, minimize voltage ripple, and improve power factor.

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Conflicts of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper.

References

[1] R. Ali, I. Daut, S. Taib, and N. S. Jamoshid. 2010. A New Proposal to Solar and Grid-connected Hybrid Electricity for Homes and Buildings in Malaysia. *2010 4th International Power Engineering and Optimization Conference (PEOCO)*. 445-448. Doi: 10.1109/PEOCO.2010.5559194.

[2] B. L. and R. Seyezhai. 2022. Reliability Prediction of Bridgeless AC-DC SEPIC with V-Fill for LED Applications. *2022 International Conference on Power, Energy, Control and Transmission Systems (ICPECTS)*. 1-6. Doi: 10.1109/ICPECTS56089.2022.10047352.

[3] X. Lin, S. Ding, D. Wu, and J. Luo. 2021. A Novel AC/DC Single-Phase Bridgeless SEPIC PFC Converter with Reduced Conduction Losses and Simple Structure. *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*. 127-131. Doi: 10.1109/WiPDAAsia51810.2021.9656085.

[4] X. Lin, J. Luo, and S. Ding. 2021. New Single-Phase Bridgeless High-Voltage-Gain SEPIC PFC Converters with Improved Efficiency. *2021 IEEE 3rd International Conference on Circuits and Systems (ICCS)*. 225-230. Doi: 10.1109/ICCS52645.2021.9697323.

[5] A. Prudenzi, U. Grasselli, and R. Lamedica. 2001. IEC Std. 61000-3-2 Harmonic Current Emission Limits in Practical Systems: Need of Considering Loading Level and Attenuation Effects. *Power Engineering Society Summer Meeting, 2001*. 1: 277-282. Doi: 10.1109/PESS.2001.970026.

[6] A. Agrawal, A. Shrivastava, K. C. Jana, S. Tripathi, and A. Rai. 2019. Single Stage High Brightness LED Driver with Improved Power Quality. *IOP Conf. Ser. Mater. Sci. Eng.* 594(1): 12012. Doi: 10.1088/1757-899X/594/1/012012.

[7] I. H. Hayirli, B. Kelleci, O. C. Kivanc, S. B. Ozturk, R. N. Tuncay, and M. O. Citci. 2019. Design and Analysis of 240 Watt SEPIC Converter for LED Applications. *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*. 804-809. Doi: 10.1109/ISIE.2019.8781396.

[8] L. Petersen. 2001. Input-current-shaper based on a Modified SEPIC Converter with Low Voltage Stress. *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*. 2: 666-671. Doi: 10.1109/PESC.2001.954194.

[9] P. Scalia. 1998. A Double-switch Single-stage PFC Offline Switcher Operating in CCM with High Efficiency and Low Cost. *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*. 2: 1041-1047. Doi: 10.1109/PESC.1998.703133.

[10] J. Chen, D. Maksimovic, and R. Erickson. 2001. A New Low-Stress Buck-boost Converter for Universal-input PPC Applications. *APEC 2001, Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*. 1: 343-349. Doi: 10.1109/APEC.2001.911670.

[11] H. Wei and I. Batarseh. 1998. Comparison of Basic Converter Topologies for Power Factor Correction. *Proceedings IEEE Southeastcon '98 Engineering for a New Era*. 348-353. Doi: 10.1109/SECON.1998.673368.

[12] P. F. de Melo, R. Gules, E. F. R. Romaneli, and R. C. Annunziato. 2010. A Modified SEPIC Converter for High-Power-Factor Rectifier and Universal Input Voltage Applications. *IEEE Trans. Power Electron.* 25(2): 310-321. Doi: 10.1109/TPEL.2009.2027323.

[13] E. H. Ismail. 2009. Bridgeless SEPIC Rectifier with Unity Power Factor and Reduced Conduction Losses. *IEEE Trans. Ind. Electron*. 56(4): 1147-1157. Doi: 10.1109/TIE.2008.2007552.

[14] C.-J. Tseng and C.-L. Chen. 1999. A Novel ZVT PWM Cuk Power-factor Corrector. *IEEE Trans. Ind. Electron*. 46(4): 780-787. Doi: 10.1109/41.778240.

[15] C.-J. Tseng and C.-L. Chen. 1998. A Novel Zero-voltage-Transition PWM Cuk Power Factor Corrector. *APEC '98 Thirteenth Annual Applied Power Electronics Conference and Exposition*. 2: 646-651. Doi: 10.1109/APEC.1998.653968.

[16] J. Chen, D. Maksimovic, and R. W. Erickson. 2006. Analysis and Design of a Low-stress Buck-boost Converter in Universal-input PFC Applications. *IEEE Trans. Power Electron.* 21(2): 320-329. Doi: 10.1109/TPEL.2005.869744.

[17] A. N. Kasiran, A. Ponniran, M. A. Harimon, and H. H. Hamzah. 2018. A Study of 4-level DC-DC Boost Inverter with Passive Component Reduction Consideration. *J. Phys. Conf. Ser*. 995(1): 012062. Doi: 10.1088/1742-6596/995/1/012062.

[18] M. K. . Noor *et al.* 2019. Optimization Parameter Design of SEPIC-Cuk Converter. *Int. J. Integr. Eng*. 11(1): 27-32. Doi: 10.30880/ijie. 2019.11.01.004.

[19] M. K. R. Noor *et al.* 2018. Optimization of PFC SEPIC Converter Parameters Design for Minimization of THD and Voltage Ripple. *International Journal of Engineering & Technology*. 7: 240-245. Doi: 10.11591/ijpeds.v10.i1.pp514-521.

[20] M. K. Romai Noor *et al.* 2019. Modified Single-switch Bridgeless PFC SEPIC Structure by Eliminating Circulating Current and Power Quality Improvement. *IET Power Electron.* 12(14): 3611–3858. Doi: 10.1049/iet-pel.2018.6076.

[21] M. K. Romai Noor *et al.* 2022. Improvement of Single-Switch Bridgeless PFC Cuk Converter for Circulating Current Elimination and Components Maximum Current Stress Reduction. *Int. J. Integr. Eng.* 14(1): 181-190. Doi: 10.30880/ijie.2022.14.01.016.

[22] A. Ponniran *et al.* 2023. Current THD and Output Voltage Ripple Characteristics of Flyback PFC Converters with LED Lamp and Nonlinear RL Loads. *Int. J. Integr. Eng*. 15(4): 193–200. Doi: 10.30880/ijie.2023.15.04.017.

[23] M. A. Z. A. Rashid, A. Ponniran, M. K. R. Noor, J. N. Jumadril, M. H. Yatim, and A. N. Kasiran. 2019. Optimization of PFC cuk Converter Parameters Design for Minimization of THD and Voltage Ripple. *Int. J. Power Electron. Drive Syst.* 10(1): 514–521. Doi: 10.11591/ijpeds.v10.i1.pp514-521.

[24] N. A. A. Isa *et al.* 2019. Performance between PFC Cuk and Bridgeless PFC Cuk Converter with Various Output Voltages. *Int. J. Recent Technol. Eng*. 8(2 Special Issue 2): 41-46. Doi: 10.35940/ijrte.B1008.0782S219.

[25] J. Jumadril *et al.* 2019. An Improved Two-Switch Bridgeless PFC SEPIC Structure for Total Harmonic Distortion Reduction and Circulating Current Minimization. *2019 International Conference on Electrical Engineering and Computer Science (ICECOS)*. 277-282. Doi: 10.1109/ICECOS47637.2019.8984500.

[26] M. N. A. Samat, A. Ponniran, M. A. N. Kasiran, M. H. Yatim, M. K. R. Noor, and J. N. Jumadril. 2021. Modular Multilevel DC-DC Boost Converter for High Voltage Gain Achievement with Reduction of Current and Voltage Stresses. *Int. J. Integr. Eng*. 13(2): 32-41. Doi: 10.30880/ijie.2021.13.02.005.