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MODELING AND CHARACTERIZATION OF MAJORITY (MAJ) TYPE SINGLE-ELECTRON FULL ADDER USING SIMON

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Abstract: Single Electron Transistor (SET), distinguished by a very small device size and low power dissipation, is one of the most promising nanoelectronic devices to replace conventional CMOS. It is based on controlling the transport of an individual electron. This paper focuses on the modeling and characterization of majority (MAJ) type SET full adder (FA) which is based on threshold logic gates (TLGs). An adder is very important, both as stand-alone unit and as a basis for other units such as program counters, multipliers, and memory addressing units. To model and characterize MAJ type SET full adder, few other circuits are modeled and analyzed which are single device SET, SET inverter and SET MAJ gate circuits. All the circuits are characterized using SIMON 2.0 simulator. The number of components for a MAJ type SET full adder circuit is 57 which consist of 37 capacitors and 20 tunnel junctions. The circuit is functioning as required for all the combination of input voltage. Since the full adder model is based on MAJ function, the stability of the SET inverter is an important aspect of the MAJ design because of the sensitivity of circuit tends to switch threshold value. In order to achieve stability, the input voltage must be in step function. The output waveform for this MAJ type FA is regular for all the combinations of inputs since the output-input (V_o/V_i) ratios is higher than 80% for both sum and carry-out outputs.

Keywords: Single electron transistor; full adder; quantum dot; tunnel junction; Coulomb blockade

Abstrak. Transistor elektron tunggal (SET) adalah salah satu peranti nano-elektronik bagi menggantikan CMOS yang mana dibezakan dengan saiz perantinya yang sangat kecil dan pelesapan kuasa yang rendah. Ia adalah berdasarkan kepada pengawalan pengangkutan satu elektron. Artikel ini menumpukan kepada pemodelan dan mendapatkan ciri-ciri litar penambah penuh SET jenis majority (MAJ) yang berdasarkan get logik ambang (TLGs). Litar penambah penuh adalah sangat penting kerana berfungsi sebagai unit yang boleh beroperasi dengan sendiri atau sebagai unit asas kepada reka bentuk yang lain seperti unit pembilang program, unit pendarab dan unit pengalamatan ingatan. Untuk memodel dan mendapatkan ciri-ciri litar penambah penuh SET jenis MAJ, beberapa litar lain perlu dimodel dan dianalisis yang terdiri daripada litar peranti SET, litar get TAK SET dan litar get MAJ SET. Semua litar dipercirikan menggunakan pensimulasi SIMON 2.0. Bilangan komponen bagi litar penambah penuh SET jenis MAJ ialah 57, yang terdiri daripada 37 pemuat dan 20 simpang terowong. Litar ini berfungsi seperti yang dikehendaki bagi semua kombinasi voltan masukan. Oleh kerana litar penambah penuh berdasarkan fungsi MAJ, kestabilan litar get TAK SET merupakan aspek penting dalam mereka bentuk MAJ kerana tahap kepekaan litar cenderung kepada nilai penukaran ambang. Untuk mencapai kestabilan, voltan masukan perlu diberi dalam bentuk langkah. Gelombang keluaran litar penambah penuh jenis MAJ ini adalah

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tetap bagi semua kombinasi masukan kerana nisbah keluaran-masukan (V_o/V_i) adalah lebih tinggi daripada 80% bagi kedua-dua keluaran jumlah (*sum*) dan pembawa (*carry-out*).

Kata kunci: Transistor elektron tunggal; litar penambah penuh; titik kuantum; simpang terowong; sekatan Coulomb

1.0 INTRODUCTION

Single electron transistor (SET) is a new type of switching device that uses controlled electron tunneling to amplify current. SET is distinguished by a very small device size and ultra-low power dissipation and based on controlling the transport of an individual electron. In 1987, Likharev has proposed a single-electron transistor in which the tunneling of the electrons is controlled by a bias applied at the center electrode [1]. Since then, various solutions have been developed on logic circuits, memory and other circuits.

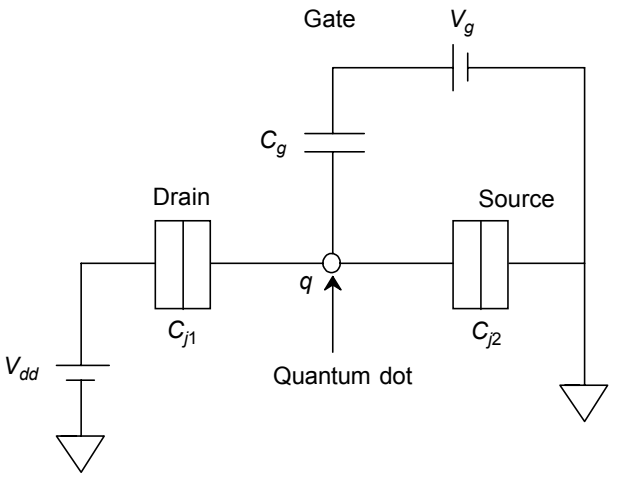
The first single electron inverter, made from two complementary SETs was proposed by Tucker *et al.* in 1992 [2]. This work explained the principles of designing complementary SETs, that corresponds to the PMOS and NMOS transistors, which can be used to design CMOS-style logic. In addition to the inverter, several SET logic gates and circuits such as SET majority (MAJ) logic gates were also proposed. A SET full adder (FA) based on the MAJ logic gates was proposed and presented by Iwamura *et al.* [3].

In this study, we perform analyses on the SET single device, SET inverter and SET MAJ gate circuits to determine the parameters values and requirement for the MAJ type SET FA circuit. All the circuits are simulated at temperature of 0 K using SIMON 2.0 simulator. This paper is organized as follows. A brief description of basic theory of SET single device and SET inverter and their characteristics are presented in section 2 and 3, respectively. After that a concept of majority gate circuit based on TLGs and its characteristics are demonstrated in section 4. Finally, the structure of FA circuit and its simulation results is described in section 5. Conclusions follow in section 6.

2.0 SET SINGLE DEVICE

A single device SET structure is similar to the MOSFET; it has a source, a drain and a gate. The main difference is that the MOS channel is replaced by an ultra-small conductive island separated by two tunnel barriers from source to drain. As shown in Figure 1, a SET consists of two tunnel junctions and a SET island (also called quantum dot), whose electrical potential is controlled by the gate [1].

The voltage applied to the gate electrode affects the amount of energy needed to change the number of electrons on the island (open or close of the SET). Basically a SET has three terminals like ordinary field-effect transistor and the gate capacitor



C_{j1}, C_{j2} : Tunnel junction capacitance for drain/source
C_g : Gate capacitance
V_g : Gate voltage
V_{dd} : Biasing voltage

Figure 1 Model of SET single device

may seem like a third tunnel junction, but it is much thicker than the others so that no electrons can tunnel through it.

For an electron to move into the system, its energy must equal to the coulomb energy, $E_C = e^2/2C$; where C is the total capacitance of this system. This E_C is also called coulomb blockade energy, which is the repelling energy of the previous electron to the next electron. For a tiny system, the capacitance C is very small, thus E_C can be very high, and the electrons cannot move simultaneously, but must pass through one by one. This phenomenon is called "coulomb blockade" [1].

When both the gate voltage and other biased voltages are zero, electrons do not have enough energy to enter the quantum dot and current does not flow. As the biased voltage between the source and drain is increased, an electron can pass through the quantum dot when the energy in the system reaches the coulomb energy, which is the Coulomb blockade effect, and the critical voltage needed to transfer an electron onto the quantum dot, equal to e/C, is called the coulomb gap voltage.

Coulomb gap voltage, V is the gap voltage needed to overcome E_C and to tunnel an electron onto the quantum dot and this condition is called tunneling phenomenon. In order to overcome the barrier (E_C), the applied voltage on the quantum dots should be; $V > e/C$ where by $(V/2) = V_g = V_{dd}$. Based on the analysis done on the circuit when V_{dd} is at 6.5 mV, all the capacitance and tunnel junction values are obtained [3]. Figure 2 shows the example of simulated characteristics of SET single device oscillation.

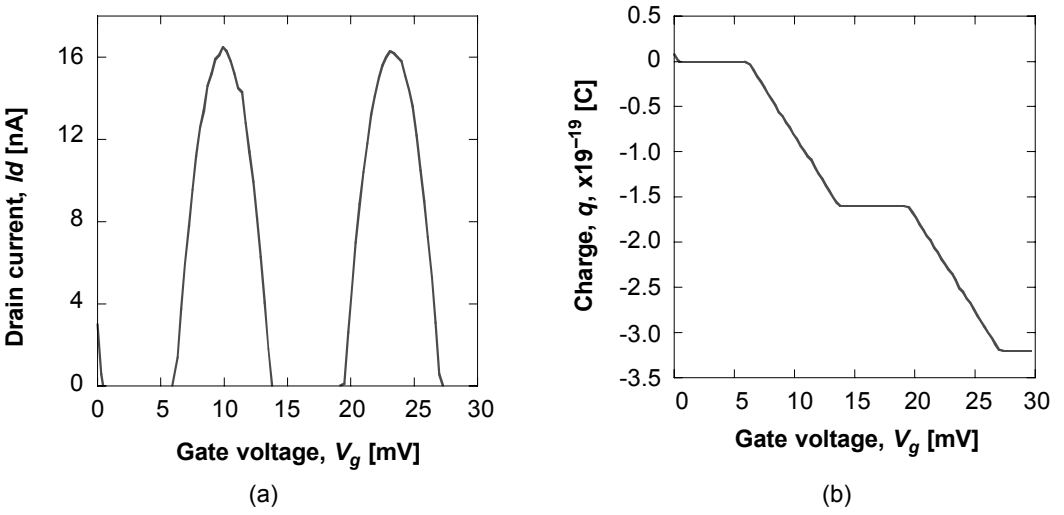


Figure 2 Simulated (a) drain current, *Id* versus gate voltage, *Vg*; (b) charge, *q* versus gate voltage, *Vg*

It can be observed that when drain voltage, V_{dd} is supplied at 6.5 mV, coulomb blockade effect occurs at quantum dot *q* when gate voltage increases from 6.5 mV to around 13 mV during the coulomb oscillation. It is clear that the drain current exhibits coulomb oscillation which is a unique characteristic of SET. During the coulomb oscillation period, one electron is charged at the quantum dot. Tunneling of one single electron occurs at the end of each current oscillation. Based on this phenomena, the characteristics of the single device circuits matches the theory of SET operation as explained in reference [1].

3.0 SET INVERTER

The SET inverter discussed in this paper is based on the SET inverter circuit proposed by J. R. Tucker [2]. It is basically a CMOS like inverter where SET transistors were substituted for the PMOS and NMOS transistors in the circuit. Based on Figure 3, the SET inverter circuit consists of four tunnel junctions (C_{j1}, C_{j2}, C_{j3} and C_{j4}), two gate capacitors (C_{g1} and C_{g2}), two biasing capacitors (C_{b1} and C_{b2}) and a load capacitor (C_L).

Each *SET 1* and *SET 2* consists of two tunnel junctions, a gate capacitor and a bias capacitor. The bias capacitor arrangement allows for the design of on/off digital switches and produces two complementary SETs. For *SET 1*, the bias capacitor (C_{b1}) is connected to ground while for *SET 2*, the bias capacitor (C_{b2}) is connected to V_{dd}. Following Figure 4 is the simulation result of SET inverter and shows that the output of the circuits matches the characteristic of an inverter operation. The V_m value is $\approx V_{in}/2$ which is the required value for switching threshold.

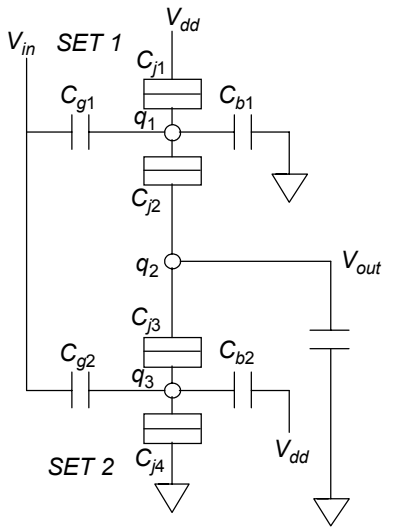


Figure 3 Model of SET inverter circuit

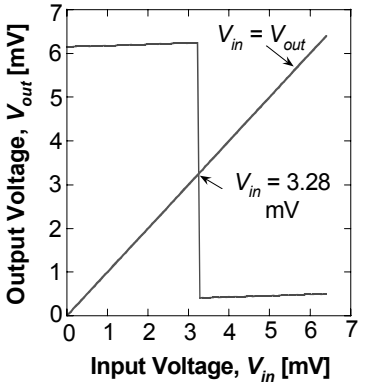


Figure 4 Output voltage, V_{out} versus input voltage, V_{in}

4.0 SET MAJORITY GATES

A majority gate is based on threshold logic gate (TLG) which was introduced by W. McCulloch and W. Pitts [4]. A TLG is the simplest artificial neuron which computes the weighted sum of its inputs ($\Sigma w_i x_i$), and compares this sum with a threshold value (θ). (*Where w_i is the weight associated with x_i, θ is the threshold and n is the number of weights/element.*) If the sum is larger than the threshold ($\Sigma w_i x_i > \theta$), the TLG output is one (high); otherwise ($\Sigma w_i x_i < \theta$) the output will be zero (low).

A MAJ gate is a particular TLG which has unity weights and a threshold equal to half the sum of weights. All the weights are equal, $w_1 = w_2 = ... = w_n = 1$, for $n = 2k + 1$

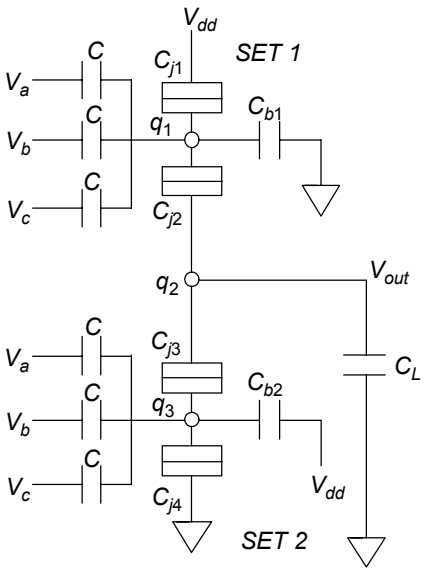


Figure 5 Model of inverter MAJ gate circuit

(for any integer $k \geq 1$). In practice, the (integer) threshold θ is reduced by 0.5 as the simplest method to improve on the noise margins. A MAJ can be represented by $(w_1, w_2...w_n; \theta - 0.5)$ with $\theta = n/2$.

In SET, both capacitor and resistor can be used to encode the weights (x_i). One of widely used approach for capacitive SET TLGs is a MOS-style implementation which was presented in [5] and known as C-SET MAJ gates. It is based on Tucker's inverter which is used for threshold. The inviter input capacitor is divided into n equal capacitor connected to the n inputs. This circuit is quite similar to SET inverter circuit. Based on Figure 5, each *SET 1* and *SET 2* consists of two tunnel junctions, three input capacitors ($n = 3$) and a bias capacitor. For the upper SET, the bias capacitor (C_{b1}) is connected to ground while for the lower SET, the bias capacitor (C_{b2}) is connected to V_{dd}. Following Figure 6 shows the simulation input voltages and the output voltage, V_{out}.

Based on the simulation result, boolean function of the circuit is obtained.

$$m = \overline{a} \bullet \overline{b} + \overline{a} \bullet \overline{c} + \overline{b} \bullet \overline{c} \text{ (linearly separable function)}$$

where following notation are used; '+' for logic OR and '•' for logic AND.

$$a = V_a,\ b = V_b,\ c = V_c \text{ and } m = V_{out}$$

From the function, it can be observed that it gives m = '1' (high) if

$$\Sigma abc \leq 1.5 \text{ and } m = \text{'0' (low) if } \Sigma abc > 1.5.$$

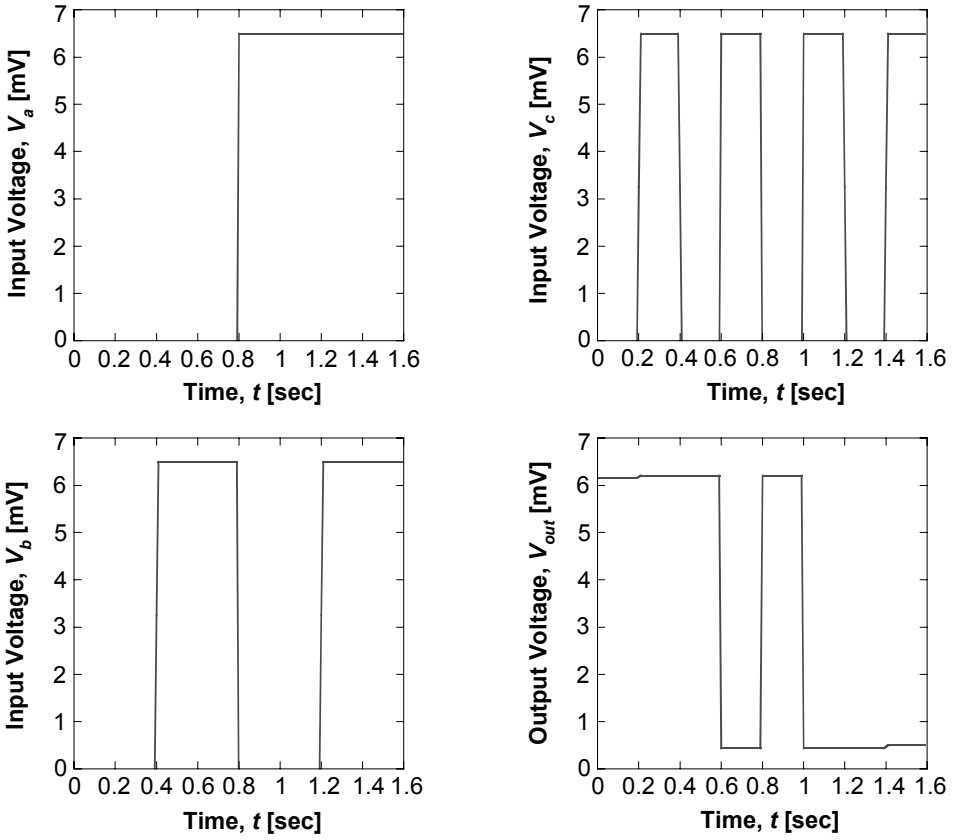


Figure 6 Simulated (a) input voltage V_a versus time; (b) input voltage V_b versus time; (c) input voltage V_c versus time; (d) output voltage V_{out} versus time

The function is exactly the complement of a MAJ gate function with $n = 3$. So a MAJ gate function can be constructed using SET inverter approach by adding an SET inverter circuit at V_{out}.

5.0 MAJ TYPE SET FULL ADDER

A full adder is a basic combinational logic circuit which has three inputs: the addend a, the augend b, and the carry-in c_i; and two outputs: the sum s, and the carry-out c_o. The boolean function of sum and carry out is:

$$s = a \oplus b \oplus c_i \tag{1}$$

$$c_o = a \bullet b + a \bullet c_i + b \bullet c_i \tag{2}$$

where the following notation are used: '$\oplus$' for logic XOR, '$\bullet$' for logic AND, '+' for logic OR.

To implement FA using only TLGs, the sum and carry-out functions have to be represented as linearly separable functions. The carry-out does satisfy this condition but the sum function not a linearly separable function. However, it can be represented in a linearly separable form by writing it in terms of both the *carry-in* (c_i) and *carry-out* (c_o) [6, 7]. And based on the analysis, the following circuit of MAJ type SET Full Adder model shown in Figure 7 is obtained. This model is simulated based on the parameter values obtained in the analysis and simulation in part 2, 3 and 4. The input voltages for the circuit are similar with possible combination of step function in Figure 6 (a), (b) and (c). Figure 8(a) and (b) show the simulation results at sum and carry-out, respectively.

Based on the simulation results, it can be observed that the output voltage is in correct step function for sum and carry-out. The circuit is functioning as required for all the combination of input voltage. The number of components for a MAJ type SET full adder as shown in Figure 7 is 57 which consist of 37 capacitors and 20 tunnel junctions.

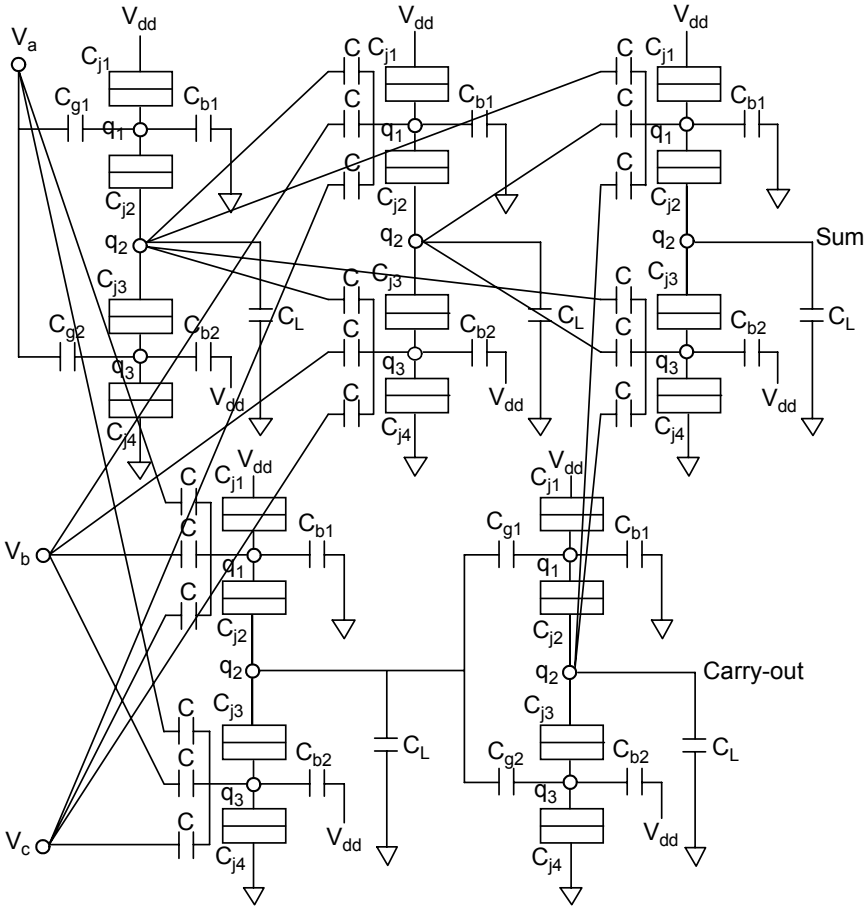


Figure 7 MAJ type SET Full Adder circuit

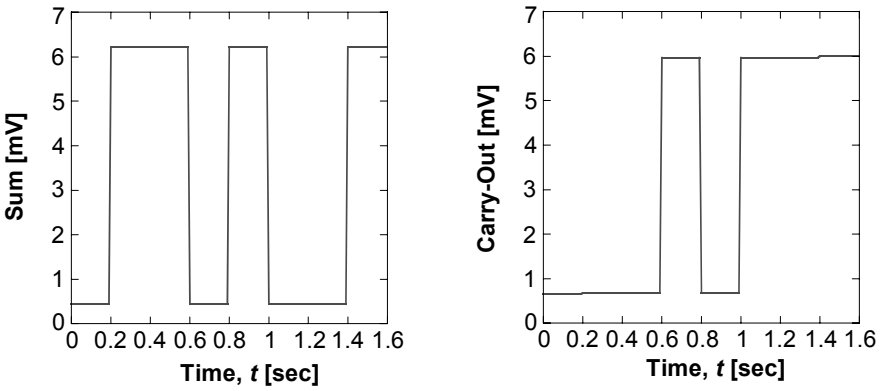


Figure 8 Simulated (a) sum voltage versus time; (b) carry out voltage versus time

For the input voltage of 0 V and 6.5 mV, the output swing for sum is 0.44 mV for low output and 6.22 mV for high output. For carry-out, the output swing is ~0.66 mV for low output and ~6 mV for high output. From these results, the output-input (V_o/V_i) ratios for sum and carry-out are 88.9% and 82.2%, respectively.

6.0 CONCLUSIONS

In summary, majority type single-electron full adder can be modeled and characterized by using SIMON simulator. This model is based on the research, calculation and analysis done on SET single device, SET inverter and SET majority gate circuits. The number of components for a MAJ type SET full adder is 57 which consist of 37 capacitors and 20 tunnel junctions. The input voltage is given in step function of all possible combination. Since the full adder model is based on MAJ function, the stability of the SET inverter is an important aspect of the MAJ design. Having an unstable region of intermediate values of input is a serious problem in MAJ and TLG application because of the sensitivity of circuit to switching threshold value. In order to achieve stability, the input voltage must be in step function. The output waveform for this MAJ type FA is regular for all the combinations of inputs since the output-input (V_o/V_i) ratios is higher than 80% for both sum and carry out outputs. SIMON simulator has proven to be an important tool to analyze and simulate SET circuit. It simulates the propagation of single electron through a network consisting of small tunnel junctions, capacitors, resistors, current sources and voltage sources. All the simulations in this paper are carried out by giving importance to all the stated parameters in order to realize SET circuits operation.

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