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CHARACTERIZATION OF BINARY DECISION DIAGRAM BASED SINGLE-ELECTRON BASIC LOGIC CIRCUIT USING SIMON

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Abstract. There has been a continuous trend in microelectronics to scale down device sizes during the last three decades. Several new nanoelectronic devices have already been proposed and one of the most promising devices is single-electron transistors (SETs). SET is being proposed as a new device for logic applications due to the drawback of further miniaturization of MOSFET. However, SETs are not suitable to be integrated using conventional architecture for digital logic operation due to low current drivability of SETs. Binary Decision Diagram (BDD) has been proposed for digital logic architecture to overcome a problem of low current drivability. In this paper, we review briefly the basic of SETs and then characterize some BDD-based single-electron logic circuits by using SIMON 2.0 simulator. Those circuits are BDD-based NOT logic circuit, AND logic circuit and 2-bit adder circuit. Simulation results show that those logic circuits perform logic operation correctly. SIMON simulator can serve as one of user-friendly simulators in designing and verifying larger BDD-based SET logic circuits with high accuracy and flexibility.

Keywords: Single-electron tunneling; Coulomb blockade; binary decision diagram; logic circuit; adder

Abstrak. Pengecilan saiz peranti elektronik ke skala yang lebih kecil telah berterusan sejak tiga dekad yang lalu. Beberapa peranti nanoelektronik baru telah dicadangkan dan salah satu daripadanya ialah transistor elektron tunggal (SET). SET telah dicadangkan sebagai peranti yang baru kerana terdapat kelemahan yang dihadapi dalam proses pengecilan MOSFET. Walau bagaimanapun, SET tidak sesuai disepadu menggunakan seni bina lazim untuk operasi logik digital disebabkan penghasilan arus yang kecil dalam SET. Kaedah rajah penentuan binari (BDD) telah diperkenalkan sebagai seni bina logik digital untuk mengatasi masalah arus yang kecil. Dalam artikel ini, kami menerangkan pengenalan asas-asas SET dan menyiasat beberapa litar logik elektron tunggal berdasarkan BDD dengan menggunakan pensimulasi SIMON. Litar-litar yang disimulasikan adalah litar logik TAK, litar logik DAN dan litar penambah 2 bit berdasarkan BDD. Keputusan simulasi menunjukkan litar-litar logik tersebut dapat memberikan operasi logik yang betul. Pensimulasi SIMON merupakan salah satu pensimulasi yang mesra pengguna dalam mereka bentuk dan menguji litar logik SET berdasarkan BDD yang besar dengan ketepatan dan kebolehlenturan yang tinggi.

Kata kunci: Penerowongan elektron tunggal; sekatan Coulomb; rajah penentuan binari; litar logik; penambah

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1.0 INTRODUCTION

The enormous success of semiconductor microelectronics during the past three decades was based on scaling down of silicon based metal-oxide-semiconductor field-effect transistors (MOSFETs) and resulting in increase of density of logic and memory chips [1]. However, the continuous shrinking of Si MOSFET size may fulfill the high integration demands, but not the low power consumption. Several new nanoelectronic devices have already been proposed and one proposed solution is the use of single-electron transistor (SET). Single-electron devices (SEDs) are the key to minimizing power consumption because they can control the transfer of individual electrons [2]. However, SETs are not suitable to be integrated using conventional architecture for digital logic operation due to low current drivability of SETs. Binary Decision Diagram (BDD) has been proposed to overcome this problem [3]. As a result, accurate and flexible SET simulators are needed for being able to quickly design and verify BDD-based SET logic circuits.

This paper is organized as follows. In Section 2, we present briefly the basic theory of SET and its basic operation. In Section 3, we review a single-electron logic device based on the concept of the BDD. While in Section 4, we will show the simulation results of NOT logic circuit, AND logic circuit and 2-bit adder as well by using SIMON 2.0 simulator. Conclusions follow in Section 5.

2.0 SET DEVICES

2.1 Basic Structure of SET

A single electron transistor consists of a metal or semiconductor island coupled to source and a drain by tunnel junctions and coupled to a gate as capacitance [4] as shown in Figure 1. Sometimes the island is referred as quantum dot (artificial atom).

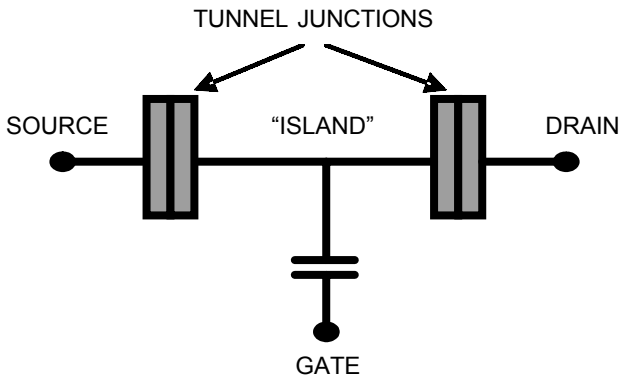

Figure 1 Schematic diagram of SET

2.2 Coulomb Blockade

Single-electron transistor devices are operating based on the coulomb blockade (CB) principle [5]. Coulomb blockade is known as electrostatic repulsion in the field of single-electronics where one electron blocks the movement of another.

The major characteristics of a SET is that the current flow in multiple number of electron charge, so we can make electrons flow one by one from source to drain while we are changing the gate voltage. Electrons are able to enter the island only one at a time. The electrons tunnel onto the island from the source and then leave the island via the drain. This flow of electrons produces a flow of current. The island is so small that the addition of just one electron in the island significantly changes the electrostatic energy of the island. The change of the electrostatic energy is known as charging energy and the equation is

$$E_C = \frac{e^2}{2C_\Sigma} \tag{1}$$

where C_Σ is the total capacitance of the island which is charged, e is the electronic charge and E_C is called the coulomb energy. The single electron tunneling phenomenon will only be observed under two conditions [5]:

(i) The charging energy must be greater than the thermal energy, k_BT, so the electrons can be fixed in the island if there is no energy applied between source and drain.

$$\frac{e^2}{2C_\Sigma} \gg k_BT \tag{2}$$

Here, k_B is the Boltzman constant and T is the temperature.

(ii) The tunnel resistance, R_T, must be larger than the fundamental resistance, R_q, so that the electrons will not be delocalized in the island.

$$R_T > R_q = \frac{h}{e^2} = 25813\Omega \tag{3}$$

3.0 SET DEVICE BASED ON BINARY DECISION DIAGRAM

BDD is a way of representing digital function by using a directed graph [3, 6]. Besides, its graphical representation is suitable for large digital functions. It has been proposed and developed as a convenient tool for computer-aided logic designs and has so far been associated only with symbolic Boolean manipulations. It provides a complete and concise representation for most digital functions encountered in logic design application.

3.1 Representing Digital Functions by BDD

In this section, we present briefly the basic operational theory of BDD [3]. A BDD is a graph composed of many nodes and two terminals, with each node labeled by a variable (*X1*, *X2*,...). In determining the value of the function for a given set of the variables, we enter at the root and proceed downward to a terminal. At each node, we follow the branch corresponding to the value of the variable. That is, we follow the 1 branch if $Xi = 1$ and the 0 branch if and $Xi = 0$. The value of the function is equal to the value of the terminal we reach. The function is 1 if we reach the terminal 1 and 0 for the terminal 0.

3.2 Device Element for Implementing BDD using Single Electron

A BDD is composed of many identical interconnected nodes, so the node is the unit element of a BDD. The function of this element is two-way switching controlled by an input variable as shown in Figure 2. This device element is a differential-input version of the single-electron switch [7]. It consists of four tunnel junctions ($J1$, $J2$, $J3$ and $J4$) and three capacitors ($C1$, $C2$ and $C3$) and is driven by a voltage clock, ϕ. It has an entry branch (A) and two exit branches (D, E). Voltage input, X (and its complement $\bar{x}$), specifying the value of a variable, is applied to island B (and C) through capacitor $C2$ (and $C3$) through the exit branch that corresponds to the binary value of the input. The path of the electron transport is $A \rightarrow B \rightarrow D$ (the 1 branch) if input X is a positive, and $A \rightarrow C \rightarrow E$ (the 0 branch) if X is a negative.

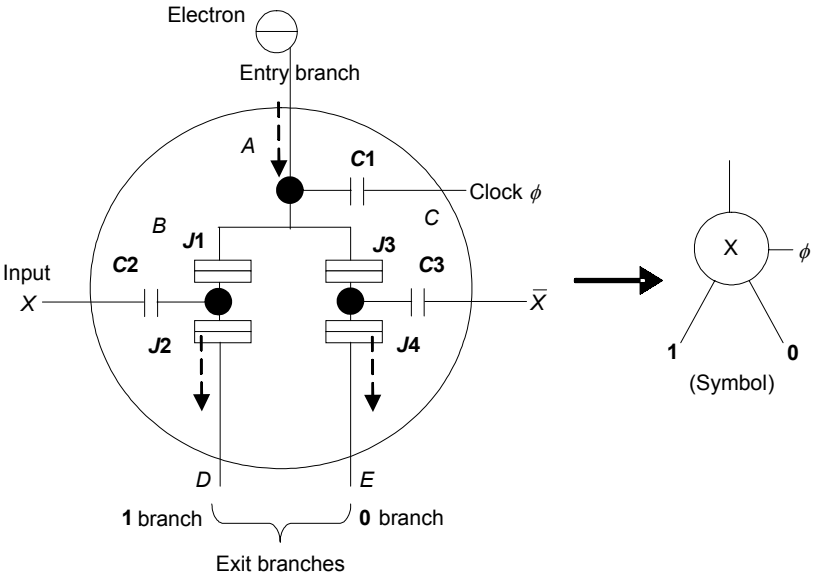

Figure 2 Unit device for single-electron BDD logic circuits

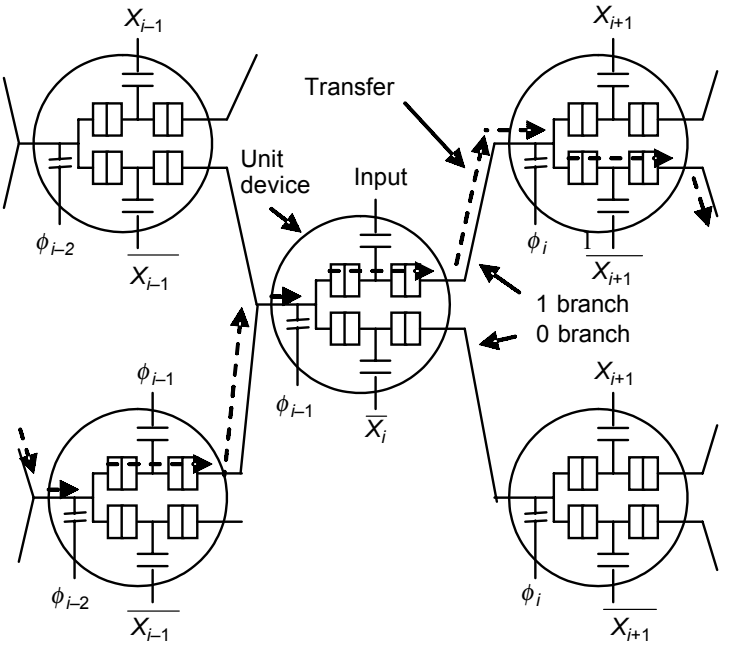

Figure 3 Unit devices cascaded to build the tree of a BDD graph. Dashed lines represent a typical path of a messenger - electron transfer

3.3 Constructing BDD Logic Circuit

A logic circuit is constructed by connecting many unit devices into a cascade to build the tree of a BDD graph, as illustrated in Figure 3. Each unit device corresponds to a node of the graph and operates as a two-way switch for the transport of a messenger electron. To transfer the messenger electron from the root to a terminal, we drive the circuit with a multiphase clock, based on the operation principle of a single-electron pump [7].

4.0 SIMULATION RESULT

Figure 4 shows the NOT logic based on BDD configuration [8]. A NOT logic circuit can be simply constructed from a unit device as illustrated in Figure 5. The device is represented by a symbol where A is the root node, B and C are the terminal nodes and $X1$ is a variable input. Node C is defined as the 1 terminal and node B as the 0 terminal. Four clocks and bias voltage are required to operate the circuit. Buffer node D is inserted into the circuit by using a tunnel junction $J1$ and $\phi 4$ clock capacitor. The buffer node acts as a delay element that holds a messenger electron. The parameters of the junction $J1$ (capacitor and resistor) are set equal to those in the unit device. For the capacitor, it is set to 1 aF and the resistance is set to 100 kΩ. We assume that the temperature is 0 K.

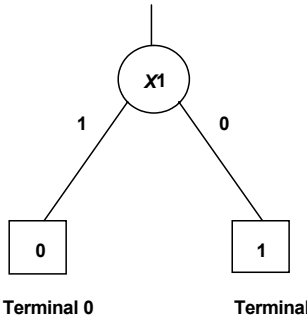

Figure 4 NOT logic circuit based on BDD configuration

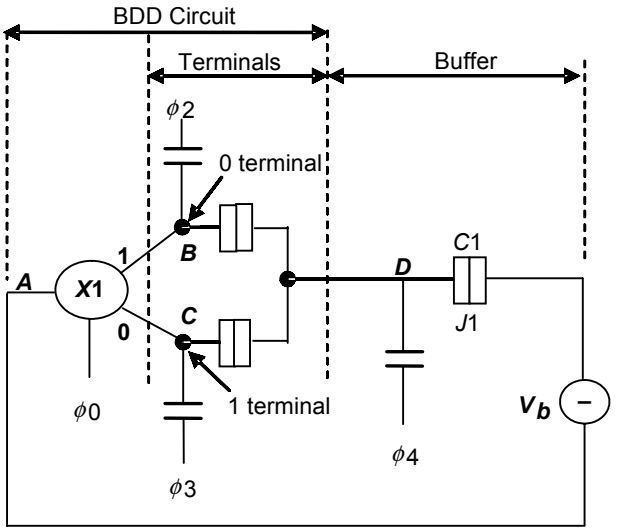

Figure 5 Circuit configuration of NOT logic

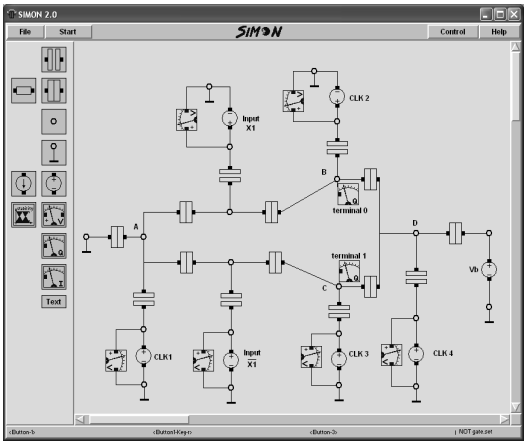

Figure 6 BDD based NOT logic circuit on SIMON 2.0 simulator interface

We used SIMON 2.0 as single-electron tunneling device and circuit simulator. Figure 6 shows the SIMON 2.0 interface with NOT logic circuit based on BDD architecture. The path of a messenger electron is expected to be $A \rightarrow B \rightarrow D$ (if input $X1 = 1$) or $A \rightarrow C \rightarrow D$ (if $X1 = 0$). At the first clock cycle, the path of electron is switched by clocking the CLK1, and then follows by input $X1$, CLK2 and lastly CLK4. At the second clock cycle, the path of electron is switched by clocking the CLK1, and then follows by input $X1$, CLK3 and lastly CLK4. The result of the simulation is illustrated in Figure 6.

The simulation data is obtained from Microsoft Excel that has been converted from SIMON 2.0. From the simulation results of NOT logic circuit, as shown in Figure 7, we could see that the electron reached at terminal once the CLK2 or CLK3

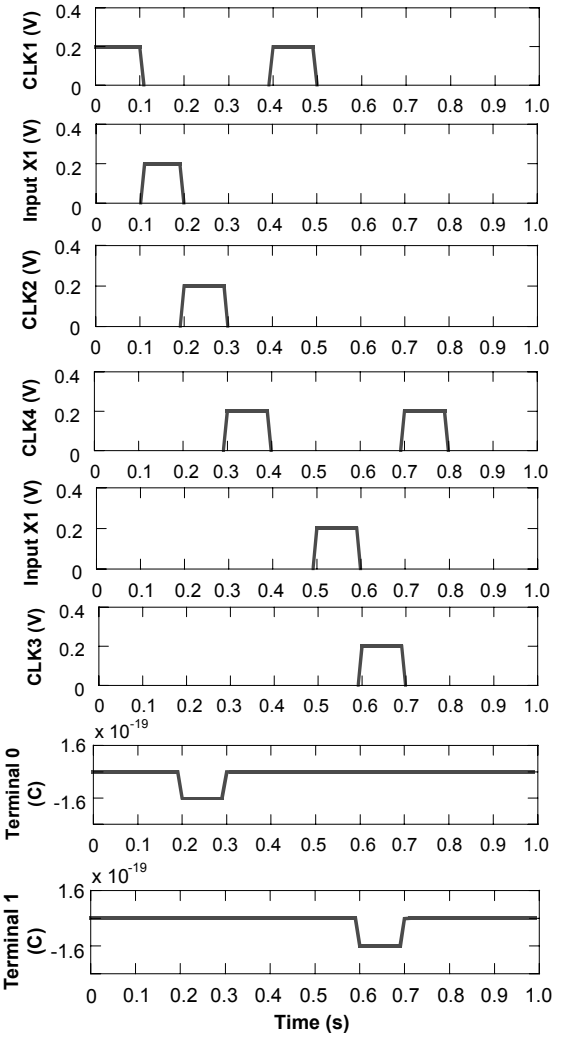

Figure 7 Simulation results for NOT operation

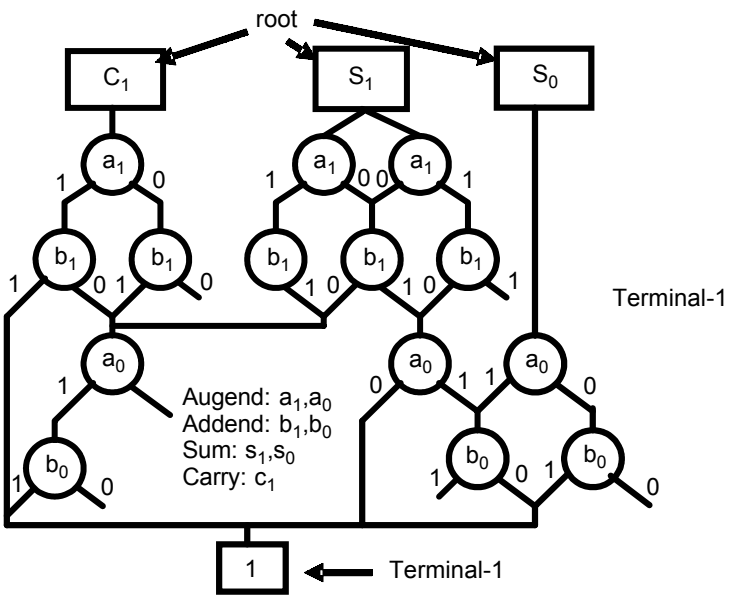

Figure 8 BDD 2-bit adder

is triggered. From this experiment, the input X is applied in sequence according to a binary code (1, 0), and the output charge on node C which is terminal 0 is observed as (0, 1). It can be seen that the circuit switched the path of the electron transported correctly, and thereby performed the expected NOT operation.

Besides NOT logic circuit, we also perform a construction and simulation of BDD based AND logic circuit which is presented in reference [9]. The circuit shows correct operation and by slightly modifying the same circuit, we can obtain NAND logic operation.

In the next task, we perform a circuit simulation for more complex circuit which is a BDD based 2-bit adder. Here, 2-bit adder single-electron logic is implemented by connecting unit devices into a cascade to build the tree of a BDD graph in a hexagonal way [8] as illustrated in Figure 8. This BDD consists of two output terminals which will determine the output operation. Terminal-0 was omitted from this circuit for simplicity. The full circuit configuration of 2-bit adder on SIMON 2.0 interface is shown in Figure 9. Here, the example operation of the adder is the addition of two bit number $a_1a_0 = 01$ and $b_1b_0 = 11$ where a_0 and b_0 are LSB while a_1 and b_1 are MSB and the result yields $c_1s_1s_0 = 100$ where c_1 is the carry bit and s_1 and s_0 are the sum bit. Figure (10a), (10b) and (10c) shows the results for the sum bit s_0, s_1 and carry bit c_1 of 2- bit adder, respectively. It is clearly shown that the adder give correct operation results.

After the present achievement, the study will be continued on constructing full adder (FA) circuit which is also based on the concept of BDD. This circuit is also known as hexagonal BDD full adder [8]. The purpose of implementing on hexagonal

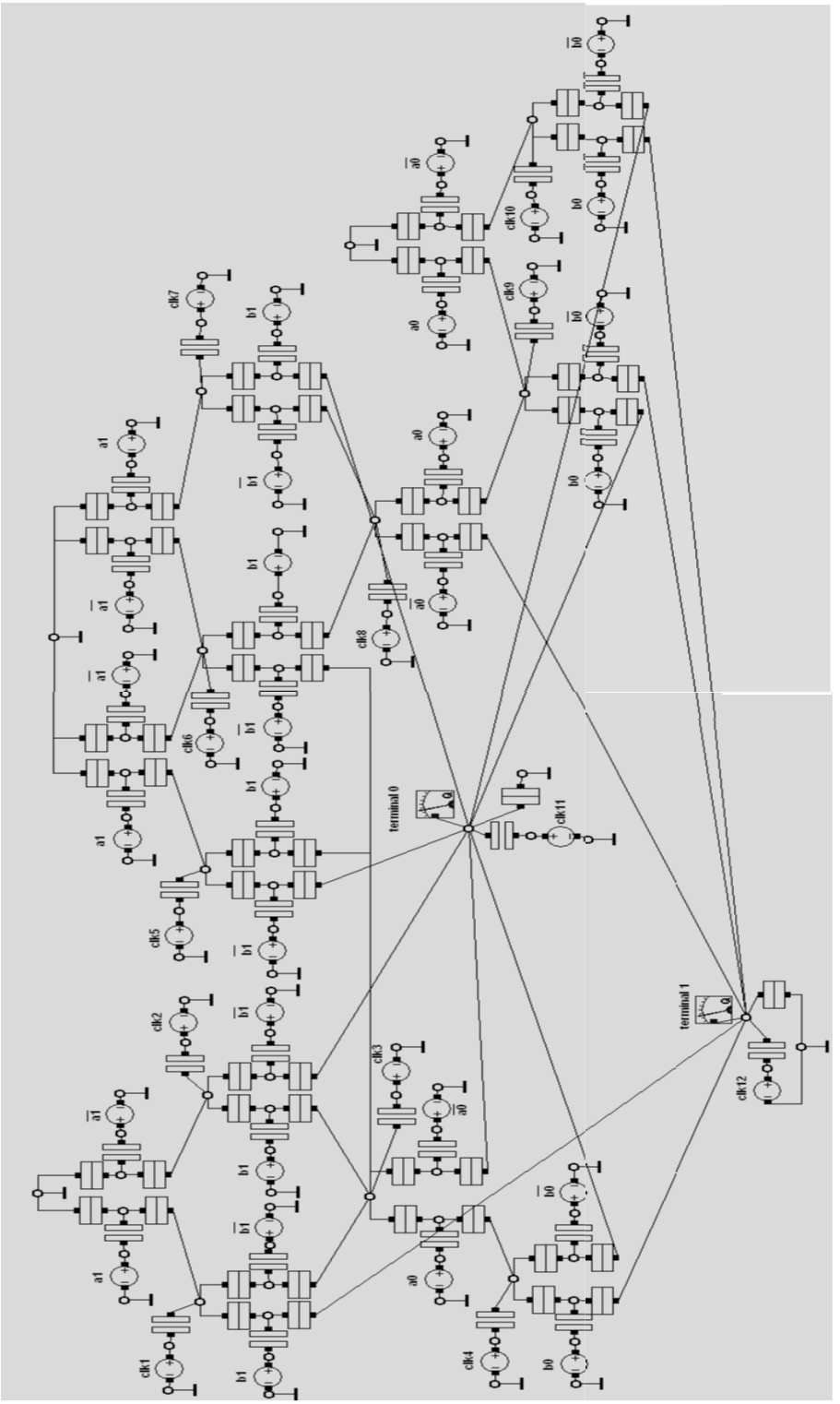

Figure 9 BDD 2-bit adder on SIMON 2.0 interface

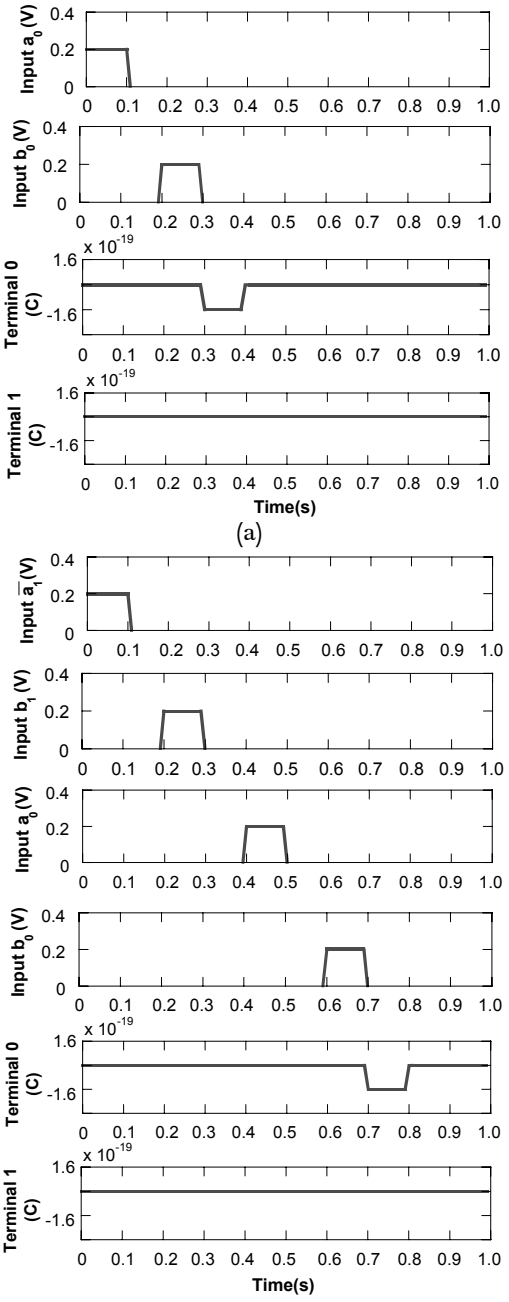

Figure 10 Output (a) sum s_0 (b) sum s_1 and (c) carry c_1 of 2-bit adder

is because hexagonal is closely packed structure, small device count and high density integration. Figure 11 illustrates the hexagonal BDD full adder which is going to be constructed and then simulated using SIMON 2.0 simulator in the future.

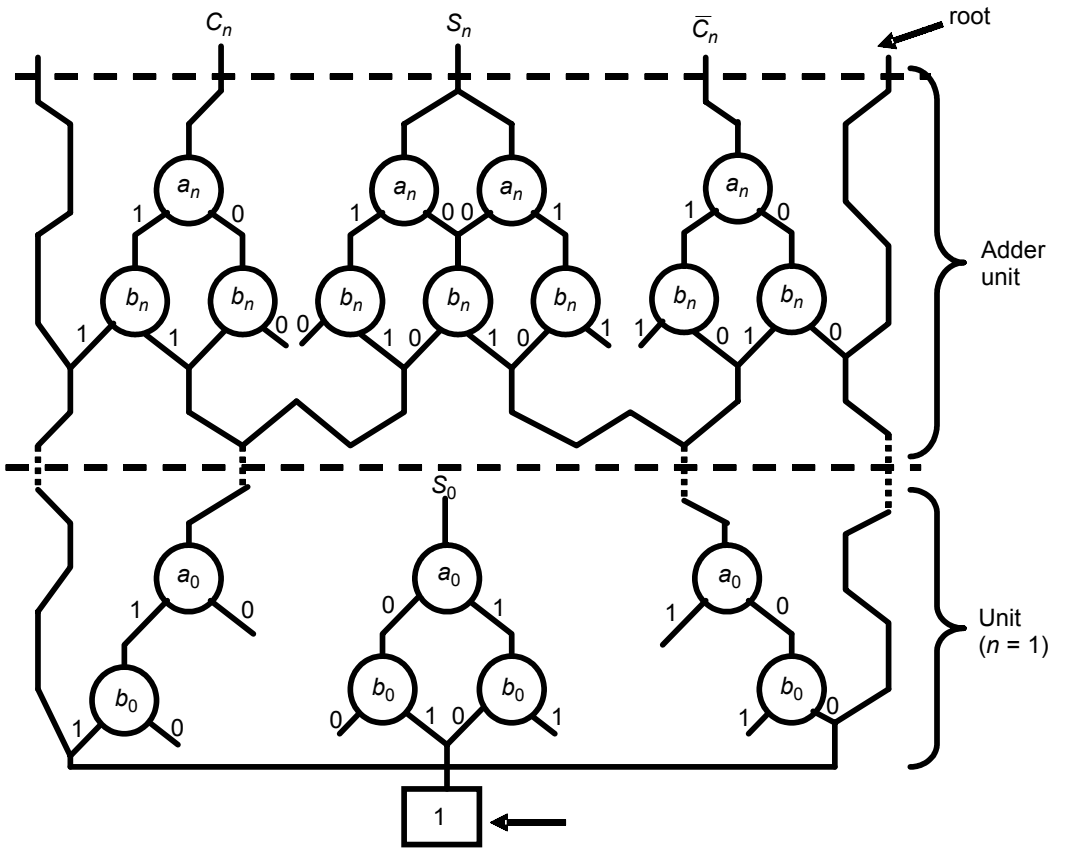

Figure 11 Hexagonal BDD full adder

5.0 CONCLUSION

Single-electron transistors have high potential for future large-scale integration because of their low power consumption and small size. In this paper, we started the work by reviewing the single-electron logic device based on the binary decision diagram. Lastly, we simulated basic logic NOT circuit, AND circuit and 2-bit adder based on BDD architecture using SIMON 2.0 simulator and the simulation shows that those circuit performs the logic operation correctly. This simulator might provide high accuracy and flexibility in simulating larger BDD based circuits such as nanoprocessor. By using the BDD devices, a high-density and low-power LSI's can be constructed. This device has a good possibility of becoming a key element in future LSI's.

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