Jurnal Teknologi, 49(D) Dis. 2008: 129–141
© Universiti Teknologi Malaysia

CHARACTERIZATION OF MOSFET-LIKE CARBON NANOTUBE FIELD EFFECT TRANSISTOR USING MATLAB BASED PROGRAMMING

ABDUL MANAF HASHIM[1*] HNG HUI PING[2] & CHUAH YEN PIN[3]

Abstract: The downscaling of metal-oxide-semiconductor field-effect transistor (MOSFET) has been taking place since decades ago for enhancing circuit functionality and also for extending Moore's Law. As the downsizing of MOSFET continues, it faces the challenge of size limitation and severe short-channel effects (SCEs) appear to affect the performance of nanoscale-MOSFET. Some novel nanoelectronic devices are proposed, hoping to overcome those MOSFET limitations. One of the novel nanoelectronic devices is carbon nanotube field-effect transistor (CNFET). Simulation work using MATLAB based programming on CNFET is carried out in this paper to investigate the dependence of current-voltage (I-V) characteristics on various carbon nanotube (CNT) diameters, insulator thicknesses and temperatures as well as their transconductances, gate delays and energy delay products (EDPs). The simulation results are presented and then compared with conventional nanoscale-MOSFET. From the simulated results, CNFET seem to provide better performance than MOSFET in term of high speed capability and lower switching power consumption.

Keywords: MOSFET; carbon nanotube; energy delay product; nanostructure; field-effect transistor

Abstrak: Pengecilan skala metal-oksida-separa pengalir transistor kesan medan (MOSFET) telah dijalankan sejak sedekad yang lalu untuk meningkatkan fungsi litar dan juga meneruskan hukum Moore (Moore's Law). Penurunan saiz MOSFET secara berterusan telah mencapai tahap pembatasan saiz dan menghasilkan kesan saluran pendek (SCE), yang mana memberi kesan kepada prestasi MOSFET berskala nano. Beberapa peranti nano-elektronik baru telah dicadangkan dengan harapan mampu mengatasi pembatasan MOSFET ini. Salah satu peranti nanoelektronik baru ialah transistor kesan medan tiub nano karbon (CNFET). Kerja simulasi menggunakan atur cara berteraskan MATLAB ke atas CNFET telah dijalankan dalam kajian ini untuk menyiasat kebergantungan sifat-sifat arus-voltan (I-V) ke atas pelbagai diameter, ketebalan penebat, suhu, kebolehaliran, tunda get dan produk tunda tenaga (EDP) transistor kesan medan tiub nano karbon ini. Keputusan simulasi dibentangkan dan dibandingkan dengan sifat yang dihasilkan oleh MOSFET skala nano. Hasil daripada keputusan simulasi, CNFET dilihat mampu untuk mrnghasilkan prestasi yang lebih baik daripada MOSFET dari segi kebolehan halaju tinggi dan penggunaan kuasa pengsuisan rendah.

Kata kunci: Tiub nano karbon; MOSFET; kepengaliran; produk tunda tenaga

[1,2&3] Material Innovations and Nanoelectronics (MINE), Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 UTM Skudai, Johor Bahru, Malaysia

[1] Ibnu Sina Institute for Fundamental Science Studies, Universiti Teknologi Malaysia, 81310 UTM Skudai, Johor Bahru, Malaysia

* Corresponding author: Tel: +607-553-6230; Fax: +607-556-6272 Email: manaf@fke.utm.my

1.0 INTRODUCTION

The electronic devices with small size, light weight, low power consumption, high performance and rich in functionalities are highly demanded to realize ubiquitous network society [1]. For the past 40 years, the semiconductor industry and academia have pushed the downscaling of metal-oxide-semiconductor field-effect transistor (MOSFET) to achieve those requirements. However, the continuous shrinking of Si MOSFET size may fulfill the high integration demands, but not the low power consumption [2]. It was suggested that MOSFET device scaling might not be extended to below 10 nm because of physical limits caused by leakage current in devices. In addition, once electronic devices approach the nanoscale, the bulk properties of solids are replaced by the quantum-mechanic properties of a relatively few atoms such as energy quantization and tunneling. It is therefore important to search for alternative devices for Si MOSFET devices. Some novel nanoelectronic devices have been suggested to replace the MOSFET to overcome those limitation challenges. The nanoelectronic devices that have been proposed include carbon nanotube field-effect transistor (CNFET) [3], single electron transistor (SET) [4] and resonant tunneling devices [5].

Among the options suggested, CNFET appears to be the most promising nanostructure devices in realizing the nanotransistors and replacing current Si MOSFET, due to the superior electrical and mechanical properties of carbon nanotube (CNT) [6 – 7]. For examples, nanotubes have a lightweight and record-high elastic modulus, and they are predicted to be by far the strongest fibers that can be made. Their high strength and high flexibility are unique mechanical properties. The electronic properties depend drastically on both the diameter and the chirality of the hexagonal carbon lattice along the tube [8 – 9]. Since the first demonstration of CNFET in 1998 [10], significant progress has been achieved in understanding device physics and in improving transistor performance.

In a CNT, low bias transport can be nearly ballistic across distances of several hundred nanometers [3]. In addition, deposition of high-k gate insulators does not degrade the carrier mobility because the topological structure results in an absence of dangling bonds [11]. The conduction and valence bands in CNT are symmetric, which is advantageous for complementary applications. The band-structure is direct, which enables optical emission, and finally, CNT is highly resistant to electromigration [11]. Because of these attractive features, CNTs are receiving much attention for possible device applications.

This paper investigates the dependence of current-voltage (I-V) characteristics of CNFET on various carbon nanotube (CNT) diameter, insulator thickness and temperature as well as their transconductances, gate delays and energy delay products (EDPs). The theoretical analysis procedure based on the model proposed by A. Rahman *et al.* [12] will applied in this study.

To gauge the possibility of CNFET as a new candidate for high-performance and low-power logic applications, it is important that this new device be benchmarked against the best nanoscale Si MOSFET data using a set of well-known device metrics. In this paper, three metrics include: (1) transconductance; (2) gate delay; and (3) energy-delay product were used. These three metrics capture the fundamental device parameters for logic applications, namely: (1) speed and (2) switching energy. The simulation results are presented and then compared with conventional nanoscale-MOSFET. From the simulated results, CNFET seem to provide better performance than MOSFET in term of high speed capability and lower switching power consumption.

2.0 THEORETICAL ANALYSIS OF CNFET

2.1 Structures of MOSFET-like CNFET

The structure of CNFET is almost the same with silicon MOSFET except the CNT is attached in the transistor and acts as the channel. CNFET operates on the same principle operation of MOSFET. The electrons travel from the source terminal to the drain terminal, which in other words, the current is flowing from the drain terminal to the source terminal. In this study, we will focus on MOSFET-like CNFET structure as shown schematically in Figure 1. The source and drain are heavily doped and hence, exhibits substantially improved performance [12]. MOSFET-like CNFET operates on the principle of modulation the barrier height by gate voltage application. The drain current is controlled by number of charge that is induced in the channel by gate terminal.

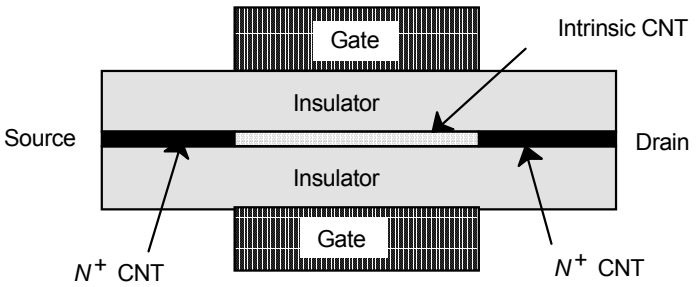

Figure 1 Diagram of MOSFET-like CNFET

2.2 Simulation Model of CNFET

For accurate benchmarking, the dielectric constant, ε_r of 3.9 was applied in the simulated model. We have assumed ballistic transport in the CNFET channel. The

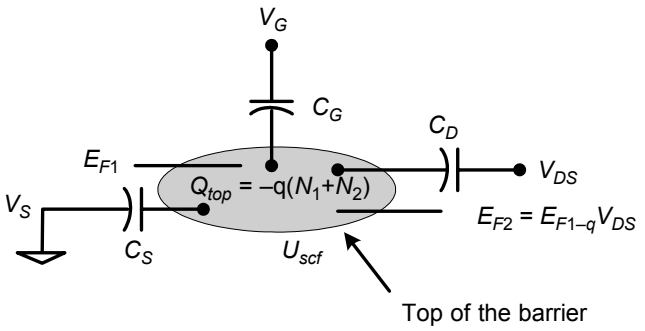

Figure 2 The 2D MOSFET-like CNFET model used for simulation study

two-dimensional (2D) MOSFET-like CNFET model used in this study as schematically shown in Figure (2), which is based on the CNFET model proposed by A. Rahman *et al.* [12]. A brief description of the theoretical analysis procedure is given as the following.

It consists of three capacitors, which represents the effect of the three terminals on the potential at the top of the barrier. The shaded region indicates the mobile charge. The mobile charge is determined by the local density of states at the top of the barrier, location of the source and drain Fermi levels, E_{F1} and E_{F2} and self-consistent potential at the top of the barrier, U_{scf}.

When the terminal biases are zero, the equilibrium electron density at the top of the barrier is

$$N_o = \int_{-\infty}^{+\infty} D(E) f\left(E - E_F\right) dE \tag{1}$$

where $f(E-E_F)$ is the equilibrium Fermi function and $D(E)$ is the local density of states at the top of the barrier. When a bias is applied to the gate, $V_{GS}(=V_G)$ and drain, V_{DS} terminals, where in this work source terminal is always grounded, there are two things that happens:

(i) the self-consistent potential at the top of barrier becomes U_{scf},
(ii) the states at the top of the barrier are now populated by two different Fermi levels which are N_1 and N_2.

The positive velocity states are filled by the source,

$$N_1 = \frac{D(E)}{2} \int_{-\infty}^{+\infty} f\left(E + U_{scf} - E_{F1}\right) dE \tag{2}$$

while the negative velocity states are filled by the drain,

$$N_2 = \frac{D(E)}{2}\int_{-\infty}^{+\infty} f\left(E + U_{scf} - E_{F2}\right) dE \tag{3}$$

where $E_{F1} = E_F$ and $E_{F2} = E_F - qV_{DS}$.

For self-consistent potential, U_{scf}, is obtained by making two assumptions of conditions. The first part of solution is the Laplace potential at the top of the barrier due to the terminal biases,

$$U_L = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S\right) \tag{4}$$

where $\alpha_G = \frac{C_G}{C_\Sigma}, \alpha_D = \frac{C_D}{C_\Sigma}, \alpha_S = \frac{C_S}{C_\Sigma}$

The second part of solution is computing the potential due to the mobile charge at the top of the barrier,

$$U_P = \frac{q^2}{C_\Sigma}\left(\left(N_1 + N_2\right) - N_0\right) \tag{5}$$

By solving Equation (1), (2), (3) and (5), we can integrate the two unknowns, N and U_{scf} into the drain current and we get

$$I_D = \frac{4qk_BT}{h}\left[\ln\left(1 + exp\left(E_{F1} - U_{scf}\right) - \ln\left(1 + exp\right)\right)\right] \tag{6}$$

where k_B is the Boltzman constant, T is operating temperature and h is Plank's constant.

3.0 SIMULATION RESULTS AND DISCUSSION

3.1 Current-voltage (I-V) Characteristics

3.1.1 Effect of Insulator Thickness

Now we look into the effect of insulator thickness on CNFET performance. The CNT diameter is set constant at 1 nm, while the operating temperature is at 300 K and the insulator thickness varies from 1 nm to 4 nm. Figure (3a) and (3b) shows the plot of $I_{DS} - V_{GS}$ dependence with insulator thickness in linear and logarithmic scale, respectively. From both figures, we noticed that the conductivity is inversely proportional to insulator thickness. Thinner insulator thickness will produce larger gate-source voltage effect to the CNT, since the modulating of barrier height is controlled by the gate-source voltage, so the conductivity will increase when the insulator thickness decrease.

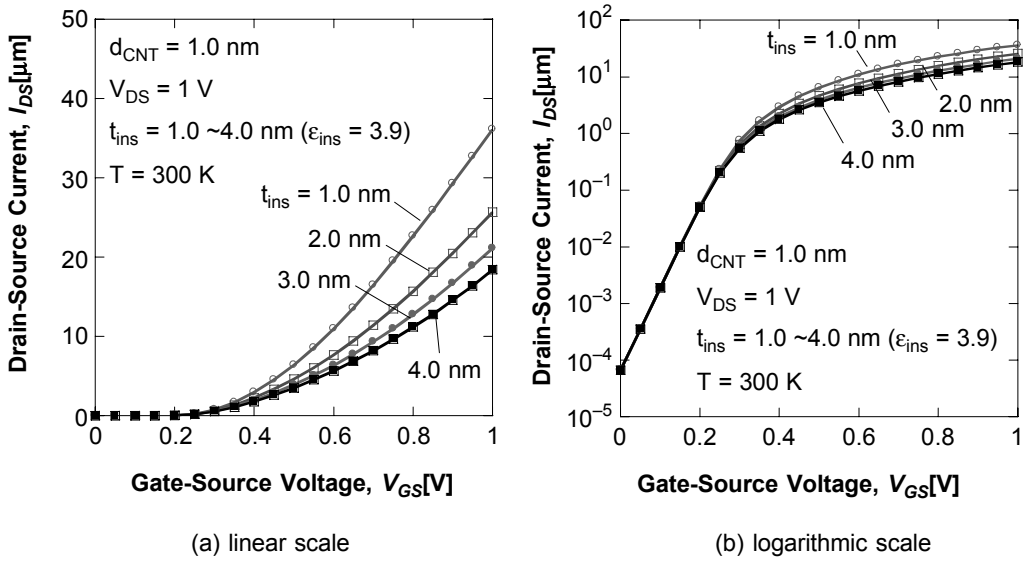

Figure 3 Effect of insulator thickness on I_{DS} vs. V_{GS}

From the figures, they are sharing a same threshold voltage, V_{TH} and off-state current, $I_{DS(OFF)}$ although the insulator thicknesses are varying from 1 nm to 4 nm. This showed that the MOSFET-like CNFET had suppressed the ambipolar characteristics in which the leakage current is not increasing significantly when the oxide thickness is thin. Hence, if a MOSFET-like structure with heavily doped source and drain regions of CNT can be produced, then the leakage current is reduced and ambipolar conduction is suppressed.

3.1.2 Effect of CNT Diameter Size

Diameter size of CNT is known could affect the bandgap on CNT and since the drain-source current of CNFET is dependent on the total charge that filled up the first sub-band, therefore it is possible that the drain-source current depends on the diameter of CNT. For this case, the insulator thickness is set constant at 1.5 nm, while the operating temperature is at 300 K and the CNT diameters vary from 1nm to 3 nm. Figure (4a) and (4b) shows the plot of I_{DS} – V_{GS} dependence with CNT diameters in linear and logarithmic scale, respectively. The results show that the conductivity is proportional to the CNT diameter and it is correct as the hypothesis stated above. Both figures show that they are sharing the same V_{TH} and $I_{DS(OFF)}$ for different CNT diameters. Due to the proportional characteristics, the drain-source current conductivity increase enormously with slightly increase in the CNT diameter. Hence, we can say that larger diameter size of CNT will give larger current.

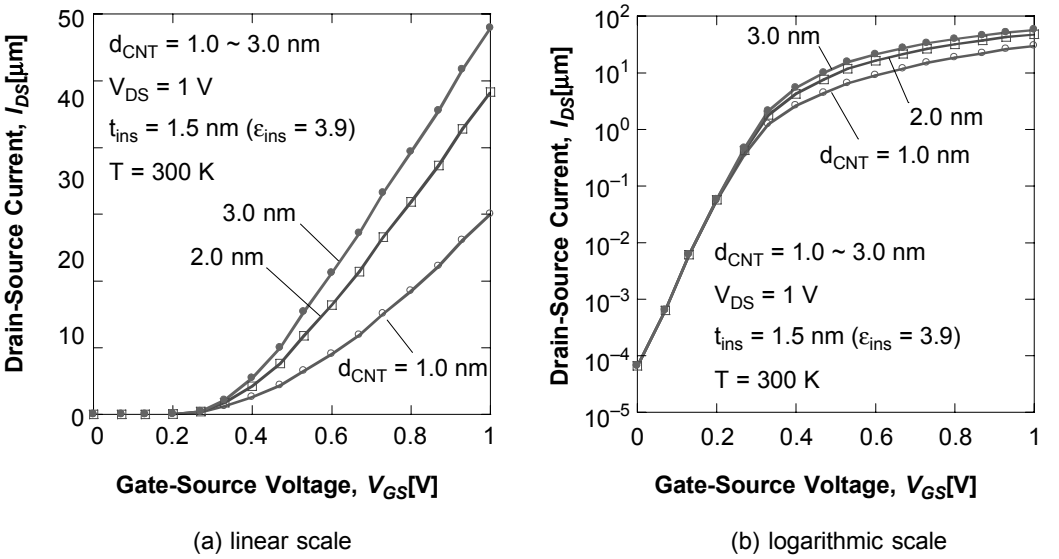

Figure 4 Effect of CNT diameter on I_{DS} vs. V_{GS}

3.1.3 Effect of Temperature

The CNT diameter is set constant at 1 nm, while the insulator thickness set at 1.5 nm and the temperatures vary from 100 K to 500 K. Figure (5a) and (5b) shows the I_{DS} vs. V_{GS} with temperatures vary in linear and logarithmic scale, respectively. Here,

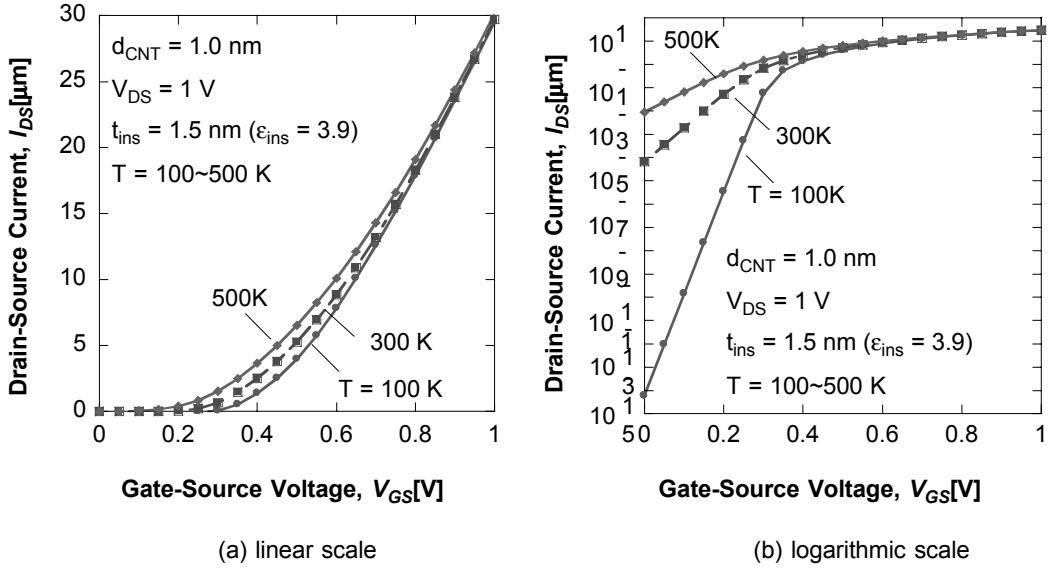

Figure 5 Effect of temperature on I_{DS} vs. V_{GS}

V_{TH} is varying with temperatures and $I_{DS(OFF)}$ also varies with temperatures. At the higher temperature, the electron inside the CNT have higher thermal equilibrium energy, this make them easier to flow as free electron inside the CNT. So, we can see that higher temperature will produce the lower V_T and higher $I_{DS(OFF)}$.

3.2 Transconductance

Transconductance, g_m, is defined as the change in drain-source current with respect to the corresponding change in gate-source voltage as illustrated in Equation 7. It is a function of the geometry of the device as well as of the carrier mobility and threshold voltage.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}. \tag{7}$$

We have estimated the transconductance of 20 nm N-MOSFET presented by R.Chau *et al.* in reference [13]. From calculation, the transconductance for this device is ~1440 S/m.

While the transconductance calculated from this simulation work as shown in Figure 6 with parameter used are 2.0 nm of insulator thickness, 1 nm of CNT diameter and temperature of 300 K, shows a value of ~50000 S/m, which is much higher than the on presented by 20 nm N-MOSFET.

Figure (7a), (7b) and (7c) shows the effect of insulator thickness, diameter and temperature on transconductance, respectively. From the figures, it is observed that

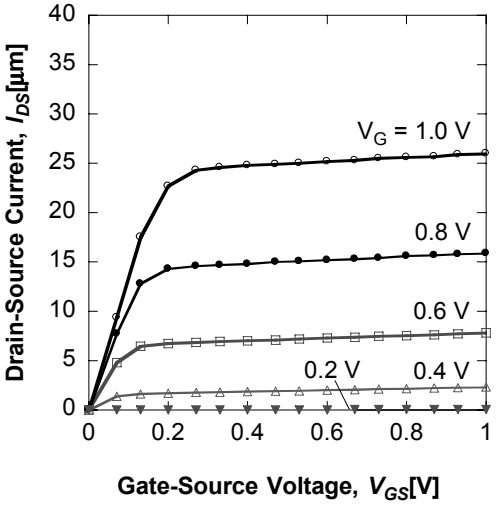

Figure 6 $I_{DS} - V_{DS}$ characteristics of MOSFET-like CNFET

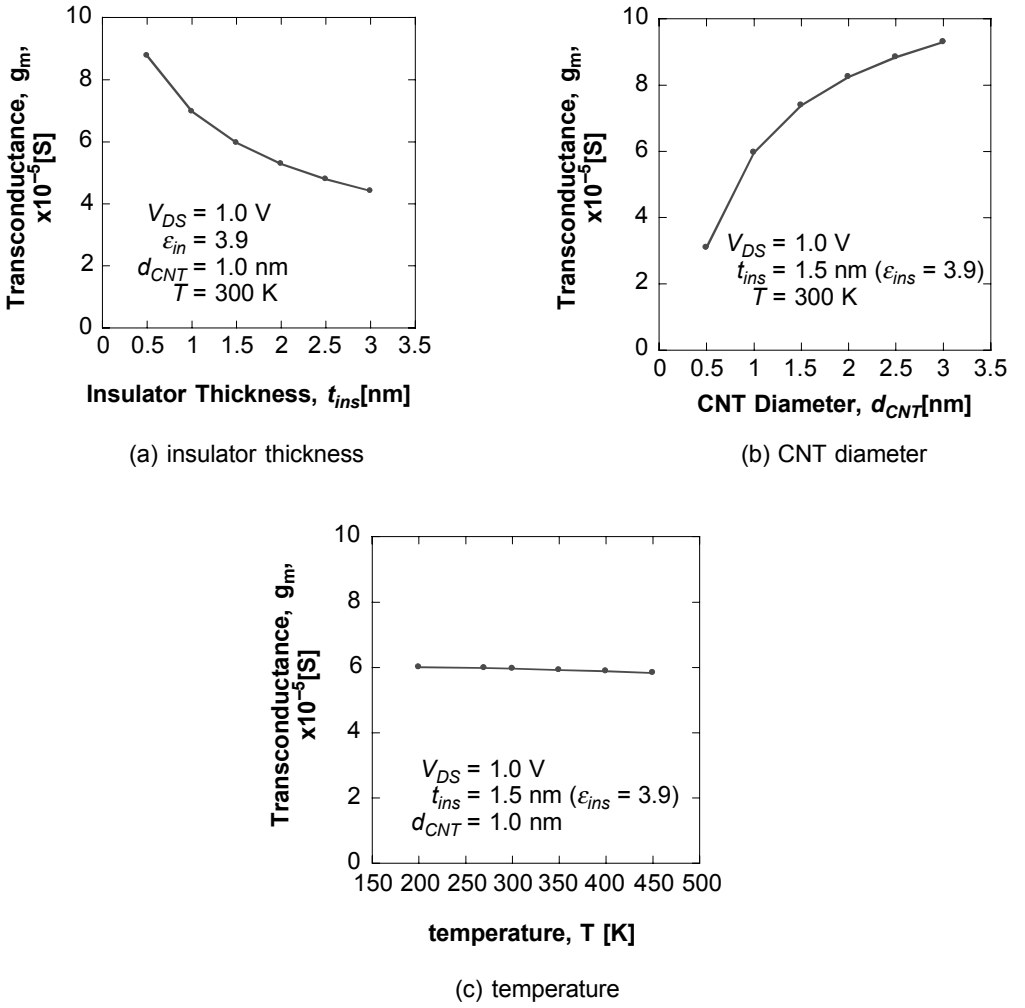

Figure 7 Transconductance characteristics as a function of (**a**) insulator thickness (**b**) CNT diameter and (**c**) temperature

smaller insulator thickness and larger CNT diameter shows higher g_m while temperature does not show much effects on the transconductance.

3.3 Gate Delay

The gate delay is translated as the amount of time starting from when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. Often this refers to the time required for the output to reach 50% of its final output level when the input changes. In other words, the gate delay shows the speed of a device. It can be determined by using the following equation.

$$gate\ delay = \frac{C_G V_{DS}}{I_{DS}} \tag{8}$$

where C_G is the gate capacitance, V_{DS} is the drain-source voltage and I_{DS} is the drain-source current at on-state. Figure 8 shows the gate delay comparison in between the Si MOSFET, III-V devices and CNFET. Here, the data for the MOSFET and III-V devices are the published data from the R. Chau *et al.* [14].

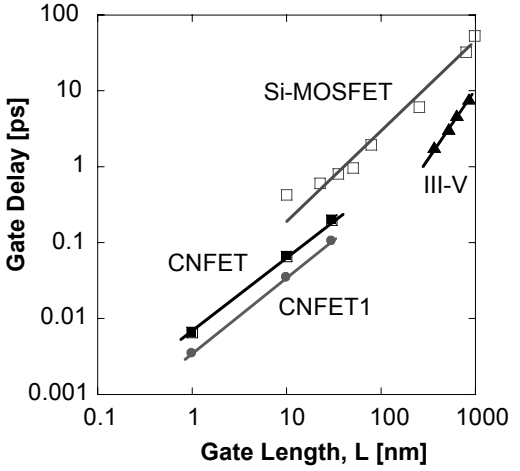

Figure 8 Gate delay as a function of gate length

It is noted here that there are two type of C_{TOTAL} which have been considered in this study. As shown in Figure 8, the C_{TOTAL} for the CNFET is only considering the insulator capacitance, C_{ins} (=C_G), while the C_{TOTAL} for the CNFET1 include both the insulator capacitance, C_{ins} and quantum capacitance, C_{QM} [14]. The C_{TOTAL} is determined by using the following equation.

$$C_{TOTAL}^{-1} = C_{ins}^{-1} + C_{QM}^{-1} \tag{9}$$

$$C_{ins} = \frac{2\pi\varepsilon_0\varepsilon_r}{ln\left(\frac{2h}{R}\right)} \tag{10}$$

where ε_r is the dielectric constant of gate insulator, R is the radius of the CNT and (h-R) is the thickness of gate insulator. The C_{QM} is the capacitance per unit length related to quantum mechanical effects and is equal to ~4 pF/cm [14].

It is clearly seen in Figure 8 that the calculated gate delay for carbon nanotube FETs shows small delay values compared to the other devices.

3.4 Energy Delay Product

The Energy Delay Product (EDP) shows the relationship between the total power consumption and speed of a device which means that the lower EDP shows the better performance. The EDP can be calculated through the equation as follows:

$$\mathrm{EDP} = C_G V_{GS}^2 x \frac{C_G V_{DS}}{I_{DS}} \tag{11}$$

Figure 9 shows the comparison of EDP in between Si MOSFET, III-V devices and CNFET. It can be seen that low EDP down 10^{-29} [Js/μm] can be achieved by CNFET. Figure (10a) and (10b) shows the importance of low drain bias, V_{DD}(=V_{DS}). Basically, smaller channel length will need smaller bias voltage. In the other word, the EDP will be smaller if the V_{DD} voltage is smaller.

From Figure (10a), the EDP of 35 nm with V_{DD} = 1.5 V is 3.5X higher than the 30 nm with V_{DD} = 0.85 V. Meanwhile, the 30 nm CNFET with adjusted V_{DD} = 0.85 V produces slightly higher EDP than 30 nm MOSFET which EDP supposing lower than the 30 nm MOSFET if the appropriate V_{DD} is applied. This shows that it is important in controlling the V_{DD} bias according to the channel length. The bias V_{DD} should be at the optimum value in order to prevent the extra waste of power consumption.

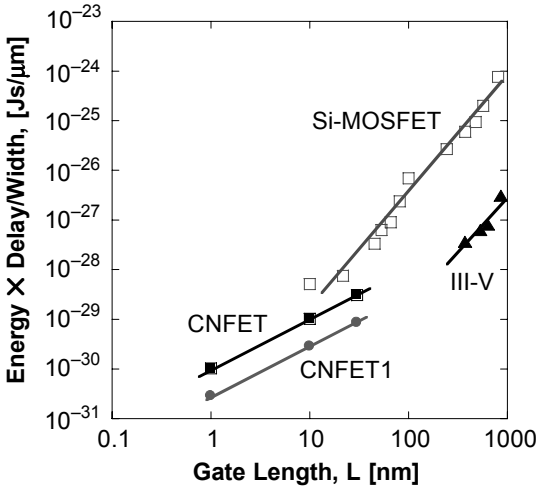

Figure 9 Energy delay product as a function of gate length

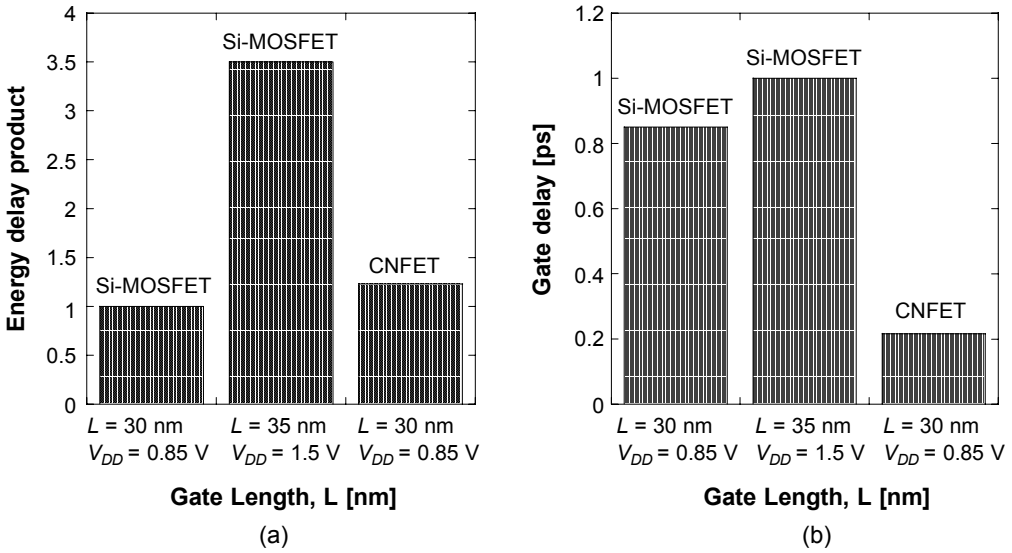

Figure 10 Effect of drain bias on (a) EDP (b) gate delay

4.0 SUMMARY

This paper investigates the I-V characteristics, transconductance and EDP of CNFET. From the simulation results, it is concluded that CNFET's transconductance performance is affected by nanotube diameter and oxide thickness but not temperature. Temperature displays the effect on the threshold voltage where higher temperature shows lower threshold voltage. While in the comparison of transconductance between CNFET and 20 nm n-MOSFET, transconductance of CNFET is considered very high compared to 20 nm N-MOSFET. The calculated energy delay product (EDP) and gate delay of CNFET also shows very small values compared to MOSFET. The obtained device performance and their general characteristics suggest that they can be a successor to replace current Si MOSFET for digital applications.

REFERENCES

[1] Hasegawa, H., S. Kasai and T. Sato. 2004. Hexagonal Binary Decision Diagram Quantum Circuit Approach for Ultra-low Power III-V Quantum LSIs. *IEICE Trans. Electron.* E87-C(11): 1757-1768.

[2] ITRS Roadmap, http://www.itrs.net, 2005.

[3] McEuen, P. L., M. S. Fuhrer and H. Park. 2002. Single-walled Carbon Nanotube Electronics. *IEEE Trans. Nanotechnology.* 1(1): 78-85.

[4] Devoret, M. H. 1998. *Single-electron Transistors.* Physic World.com.

[5] Ellenbogen, J. C. 1998. *A Brief Overview of Nanoelectronic Devices. The MITRE Coorperation.* Mclean, VA. www.nanoworld.org/NanoLibrary/brief.pdf .

[6] Dresselhaus, M. S. 1998. Carbon Nanotubes. Physics World.com.

[7] Forró, L. 2001. Physical Properties of Multi-wall Nanotubes, in: M. S. Dresselhaus, G. Dresselhaus and Ph. Avouris (Eds). *Carbon Nanotubes: Synthesis, Structure, Properties, and Applications*. New York: Springer-Verlag. 329-390.

[8] Iijima, S. and T. Ichibashi. 1993. Single-shell Carbon Nanotubes if 1-Nm Diameter. *Nature*. 363: 603-605.

[9] Bethune, D. S., C. H. Kiang, M. S. Devries, G. Gorman, R. Savoy, J. Vazquez and R. Beyers. 1993. Cobalt-catalyzed Growth of Carbon Nanotubes with Single-atomic-layerwalls. *Nature*. 363: 605-607.

[10] Tans, S. J., R. M. Vershueren and C. Dekker. 1998. Room-temperature Transistor Based on a Single Carbon Nanotube. *Nature*. 393: 49-52.

[11] Javey, A., H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom and H. Dai. 2002. High K Dielectrics for Advanced Carbon Nanotube Transistors and Logic. *Nature Materials*. 1-6.

[12] Rahman, A., J.Guo, S. Datta and M. Lundstrom. 2003. Theory of Ballistic Nanotransistors. 2003. *IEEE Trans. Electron Devices*. 50(9): 1853-1864.

[13] Chau, R. 2000. *30 nm and 20 nm Physical Gate Length CMOS Transistors*. Extended Abstracts of Silicon Nanoelectronics Workshop, Kyoto, Japan. 2-3.

[14] Chau, R. 2005. Benchmarking Nanotechnology for High-Performance and Low Power Logic Transistor Applications. *IEEE Transactions on Nanotechnology*. 4(2): 153-158.