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# The Development of FPGA-based Wireless Channel Simulator using LabVIEW

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#### Graphical abstract



#### Abstract

The development of channel model for wireless communication system is currently becoming important to fulfill the entire user's requirements and increasing demand where to provide a good communication link between the users at everywhere and anytime. An accurate techniques or operator is needed to model a very flexible channel for wireless communication application. Previous channel model is developed based on the time-frequency operator which is limited to Narrowband signaling. This operator uses Doppler shift to account for mobility in propagation space. This paper proposes a Wideband channel model which is valid for all kind of signaling and conditions. Mathematical channel model is used to represent a generic channel simulator which is implemented as channel simulator. The development and measurement of channel simulator is using LabVIEW. The LabVIEW can be used as basic software and can be turned into hardware part by connecting to other devices for real-time channel simulation. The illustration and snapshot of the channel simulator modeling in term of LabVIEW code program are presented.

Keywords: Channel; simulator; time-frequency; time-scale; LabVIEW

#### Abstrak

Pembangunan model saluran bagi sistem komunikasi tanpa wayar kini penting untuk memenuhi keperluan pengguna keseluruhan dan permintaan yang semakin meningkat disamping menyediakan pautan komunikasi yang baik antara pengguna di setiap tempat dan pada setiap masa. Satu teknik yang tepat atau operator yang diperlukan untuk model saluran yang sangat fleksibel untuk aplikasi komunikasi tanpa wayar. Model saluran sebelum ini dibangunkan berdasarkan pengendali masa kekerapan yang terhad kepada isyarat jalur sempit. Pengendali ini menggunakan anjakan Doppler ke akaun untuk mobiliti dalam ruang pembiakan. Kertas ini mencadangkan satu model saluran Wideband yang sah untuk semua jenis isyarat dan keadaan.Model saluran matematik digunakan untuk mewakili simulator saluran generik yang dilaksanakan sebagai saluran simulator. Pembangunan dan ukuran saluran simulator menggunakan LabVIEW. The LabVIEW boleh digunakan sebagai perisian asas dan boleh dijadikan sebahagian perkakasan dengan menyambungkan kepada peranti lain untuk masa sebenar saluran simulasi. Ilustrasi dan gambar model simulator saluran dari segi program kod LabVIEW dibentangkan.

Kata kunci: Saluran; simulator; kekerapan masa; skala masa; LabVIEW

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# **1.0 INTRODUCTION**

Much of the efforts have been contributed and focused in designing and modeling the reliable communication system on choosing an appropriate techniques and method for the proposed design including the modulation, coding, programming, the basicdesign software, as well as the design structure and architecture. In designing wireless channel simulator is essentially known the basic behavior of the radio channel at different operating environment then the effective and reliable wireless communication system is produced. Most of the wireless communication system is inherently inconvenient to the multipath phenomenon, time-varying nature, and the interference/ distortion that caused by the users or objects surrounding hence contribute to the channel impairment and system performance. Sometime, to solve this problem, the high transmitted power is used to overcome the system problem.

To design the wireless channel for a reliable communication system, the statistical and mathematical method is employed that play and offer an exclusive design which can generate the channel model as desired design. The channel modeling is the first step in the design that is important to compute, estimate and modify the possibility of the channel parameter that is parallel to the channel design. Therefore, the channel parameters such as the Doppler spread, Doppler shift, and the amplitude changes then coherence bandwidth can be evaluated.

To evaluate and simulate the channel modeling for wireless communication system is mostly required and desired a real time measurement or evaluation. In some case, the experiment can be directly done in vehicles or other mobility device at various condition and environment but unfortunately, it will take a long time and higher cost to make this evaluation. To presence the real time measurement for the reliable wireless communication system designs, the basic-design software which suitable to the generic channel modeling is used. This paper is used the LabVIEW as the basic-design software to model the proposed channel design based on time-scale operator. The time-scale operator is parallel operator to the Affine group which is contain a feature of time scaling know as time dilation and translation. Based on this affine group, the signal is analyzed in term of time changing which is compressing and expending signal at the specific value/parameter.

Based the Affine group, the wavelet offers a great properties to match well to the proposed channel model based on time-scale operator. This wavelet represents as the eigenfunction in the channel modeling. As mentioned, the LabVIEW offers a great interface for the real time channel modeling as well as has the function and tools for the proposed channel design. The LabVIEW has many properties and features that are required by all the designer beside it can be used directly for the hardware implementation.

LabVIEW from the national instrument products has been seen as the great platform to be used as based-design software to model and build an effective graphical system design. This software is defined as the combination of the user-defined software and hardware with component or device for data acquisition, processing, or analysis. In the LabVIEW software, the interface knows as virtual instrument which the designers can build and create their own design/model that can apply real time of mathematic and numeric for modeling, processing, analysis and controlling data. In virtual instrument, the design can be focused more to the needed application.

Moreover, the virtual instrument approach in LabVIEW is a tool for the development. The researcher can use the LabVIEW software for the modeling and simulation. After that, the prototype is approached to prove the concept whether the system modeling is valid or not. Then, the deployment is required for the field implementation which is to compile or transfer the modeling in hardware.

The graphical system design is the combination of three steps/methods of system design, prototype and deployment as shown in Figure1. It is used to increase and improve the system performance and the productivity of experimental research. Therefore, this paper focus more to the software based-design for channel modeling that has been proposed in [1-3]. The channel development in LabVIEW can be implemented into hardware by installing the complete modeling code in field programmable gate array (FPGA). The execute FPGA is represented as the channel simulator for wireless communication system [4-15].

The rest of the paper is organized as follow. In section 2 presents the experimental of work then the result and discussion is described in section 3. Then, the future works is presented in section 4 and finally, the conclusion is shown in section 5.

# **2.0 EXPERIMENTAL**

Since this work is our first experience in LabVIEW for the software and hardware development, it is necessary and good to

know the basic and general environment about the LabVIEW background as a basic-design that can be used for the software and/or hardware platform. The basic programming in LabVIEW is simple and straightforward.

The programming in LabVIEW makes the design can be developed and simulated in the software separately before it transfers to hardware that means, we not build the channel simulator design directly on FPGA until the channel simulator is able to successfully develop and simulate in LabVIEW for the entire system design without modifying any device on FPGA. LabVIEW also offers which component that needs to be determined and placed in software, on hardware, and on FPGA.

Moreover, this software has the graphical system design or graphical interface with the inclusion of FPGA and digital signal processing (DSP) related modules then this combination make it a greatly suitable and convenient to be applied for the developing system with many components [15].

Based on Figure 1, the graphical system design platform fundamentally can be used for modeling, prototyping and implementing. For channel modeling in this work, we approach these methods to design our channel simulator.

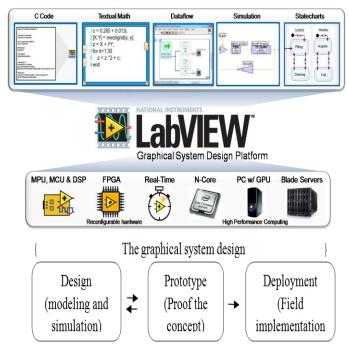


Figure 1 Computational model and the graphical system design of LabVIEW  $% \left( \mathcal{A}_{n}^{\prime}\right) =\left( \mathcal{A}_{n}^{\prime}\right) \left( \mathcal{A}$ 

Using the LabVIEW as the software based-design for the proposed channel modeling gives a wonderful advantages to the researchers. It offers for the environment deployment and programming language which is easily can combine the mathematical equation, numbers, transfer function, digital signal processing and algorithm with the real-time measurement of real-world signals for example the FPGA since this work is based mathematical and algorithm, the LabVIEW suits well as based-design software for channel modeling and simulation.

The Figure1 shows the basic interface of LabVIEW which offer to researchers which platform they want to use to build their design. There are different a computational model or platform then the researcher can choose among the variety of computational model/platform where the design is developed in LabVIEW software. The application include in LabVIEW consist of the Data Flow, Simulation, Statechart, Textual Math And C Code that can be mixed for the design development as presented in Figure 1.

For this work, the channel modeling is developed based on data flow and simulation before it turns to hardware by FPGA target. LabVIEW modules provide the FPGA module that makes building and developing the system on FPGA at the desire parameters.

When we designed our channel simulator in LabVIEW, our target is should be used for the FPGA implementation. Therefore, the design must meet and match to the FPGA language programming then the implemented channel simulator design should be able to apply for various signals such as Narrowband, Wideband and others that related to large bandwidth.

The proposed time-scale channel model is generated mathematically that correspond to the channel parameter at specific application. The generic channel simulator for wireless communication is generally presented in Figure 2. Based on Figure 2 the channel modeling is designed and developed in LabVIEW. The channel is developed by characterizing the channel response which is analyzing the behavior of channel system that interacts with the travelling signal. According to the proposed generic wireless channel simulator in Figure 2 the channel simulator is modeled by generating first the eigenstructure.

The eigenstructure is build to generate the eigenfunction that has properties matching to the time-scale operator; wavelet gives and acts as the input signal or the travelling signal which can react with the channel system. As mentioned, the channel is developed based on time-scale operator approach not the time-frequency. In the wireless communication system application, the timefrequency is being function in both time and frequency point. As general, this functionality is invalid to account the larger bandwidth range which is needed to measure and compute the signal changing in the system. For example, for the Narrowband system the time-frequency is valid to be applied to analyze the signal due to its narrow bandwidth.

The snapshot of the eigenstructure development that has been generated in the LabVIEW can be seen in Figure 3 then the eigenstructure will be simulated to give the result of the eigenfunction. This eigenfunction is presented as the input signal that sends by the transmitter. The transmitter supposedly sends a single signal but at the receiver, obtained the multiple of signals. This is because of the propagation in the system environment. To account the effect of the propagation in the system environment, then the valid parameter that cause the change of the input signal is approached and generated. Theoretically, the propagation in the system environment can cause the multipath problem. Based on this phenomenon, the multipath components are obtained. Therefore, the generating channel parameter such delay, scale, amplitude as well as spatial displacement as present in Figure 2 are to analyze and obtain the multipath values due to the propagation environment.

The multipath components generators are build in LabVIEW based on the specific parameter that parallel to the desired

environment. The generated values will be multiplied with the input signal to see the behavior of travelling signal in channel medium. The LabVIEW offers the graphical programming language which is ideally to create and build a flexible, scalable and sophisticated design that meet the specific need or desire of the proposed channel model. Then, the complex or larger code programming can be reduced and increase performance of the code/algorithm. Besides that, this can minimize the cost development and time measurement by easily changing and modifying the algorithm or developing a new algorithm.

When the multipath components are obtained that can be called as channel coefficient, the values are convoluted with the input signal then the convolution output will be added together. This convolution output present as the received signal. The mathematical model of the convolution process for wireless channel simulator design is developed shown in Figure 5.

The LabVIEW is the visual programming language that offers a data flow while MATLAB is the text based programming language therefore the LabVIEW suits well for the hardware integration. When the channel simulator is completely design, the channel simulator modeling will be installed in hardware, FPGA. Although the FPGA is a friendly hardware which can be used for many applications unfortunately, when do the FPGA implementations for channel simulator we might face some challenges or problems. One of the challenges is the implementation of the design should be on virtex FPGA at the specific name of FPGA for example PCI783R that is used for this work.

Generally, the implementation of channel simulator in FPGA is done directly to the parallel software consideration which is LabVIEW. The visual code or block programming in LabVIEW will be implemented in the PC that has been done inside LabVIEW software and the channel coefficient will be implemented in FPGA.

The channel modeling in LabVIEW is done on the virtual instrument (VI) panel/interface which is visualized as block diagram. During the FPGA compilation, the VI is converting to HDL code using the FPGA module. The compilation times is typically taken at range 10 to 40 minutes depend on the size and complexity of the VI design. The entire channel simulator is developed based on the fixed point arithmetic not the floating point because the FPGA can support the fixed point only, if there is any floating point, required to extra component or function to solve the operation problem [4-8]

Figure 2 shows the steps that have been approached for channel simulator development. Firstly, the eigenfunction is generated to present as a signal in transmission. Secondly, the multipath environment is generated to account the operating environment as well as to obtain the multipath coefficient to be convoluted with the eigenfunction to characterize the signal in the propagation medium. Last but not least, the convolution process and summation of each signal coming at receiver is developed. All the design for every steps of channel simulator development in LabVIEW is presented in Figure 3, Figure 4 and Figure 5.

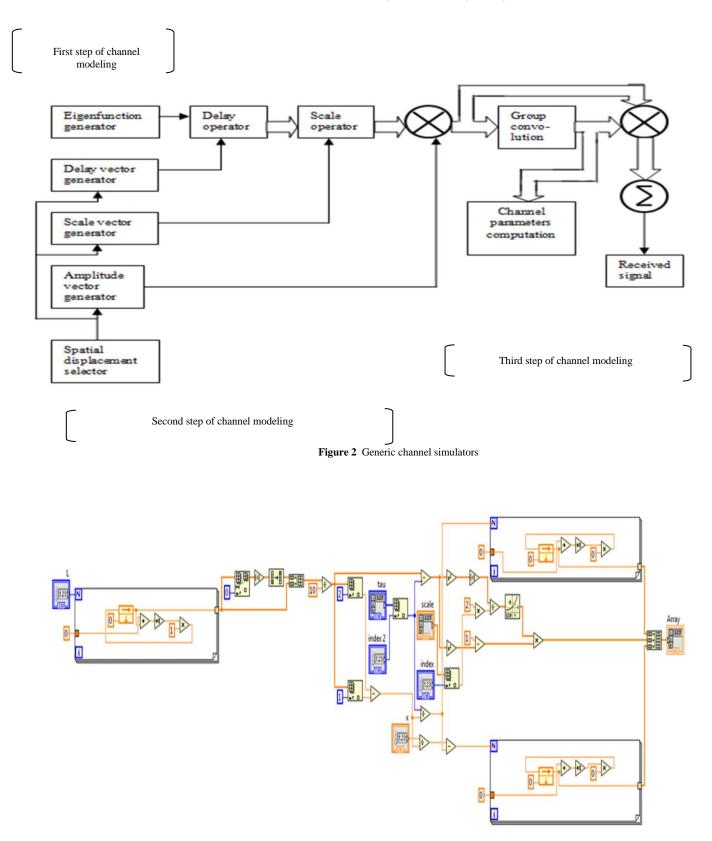


Figure 3 First channel modeling of eigenstructure generator

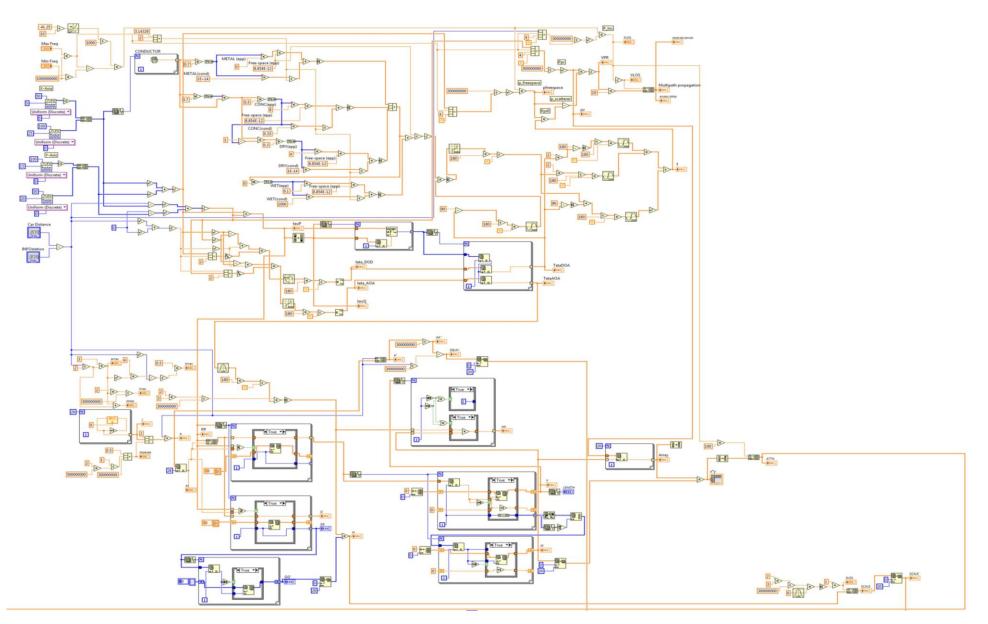


Figure 4 Second channel modeling of multipath generator

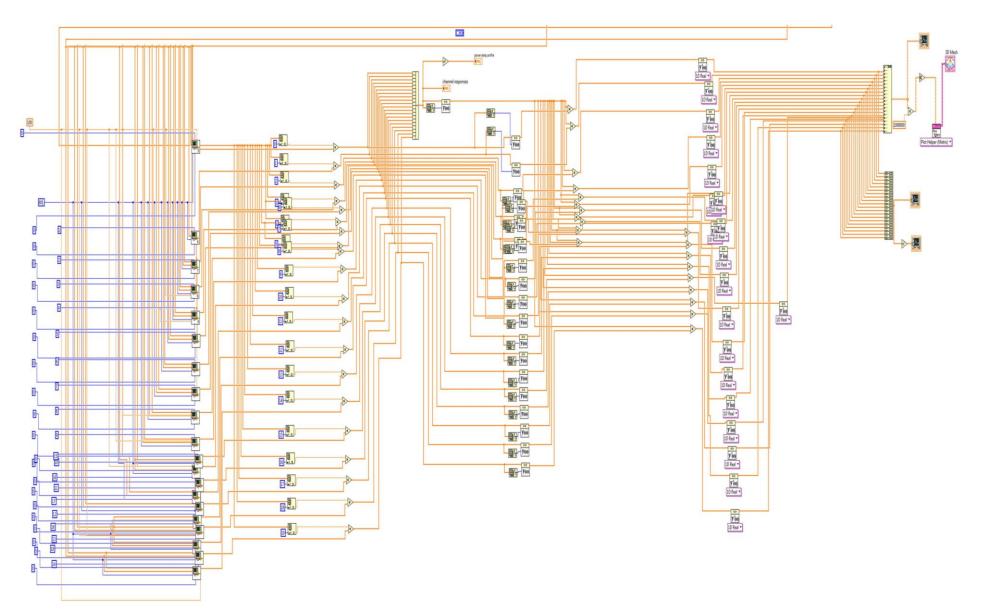


Figure 5 Third channel modeling of convolution process

Figure 4 is the development of multipath phenomenon which is to obtain the multipath component of attenuation, delay, and scale. Then, the data obtained will be inserted and used to the next development of convolution process as shown in Fig.5. These values will be multiplied with the transmitted signal therefore; the output of multiplication presents the interaction between the transmitted signal and the channel. For the complete channel simulator the illustration shows in Fig.4 will be combined to the illustration in Fig.5. After the convolution process, the convolution outputs are added together and present as the received signal.

# **3.0 RESULTS AND DISCUSSION**

The channel simulator for wireless communication system application has been completely implemented on hardware in FPGA on the virtex which is a Xilinx FPGA is presented in Figure 7. This presents an exclusive and efficient hardware implementation at the small time execution. Besides, the FPGA plays a great hardware performance for the algorithm evaluation.

This FPGA can act and play role as efficient channel simulator for the wireless channel communication system by applying at different environment. It is because, the FPGA as channel simulator offers a higher flexibility for adaptive coding such as the bandwidth availability, channel characteristic as well as the quality of service requirements by large group of users.

Moreover, the FPGA able to perform a specific computational task that meet the design specifications and parameters where has rapidly in design iteration and prototyping. Due to its flexibility, the FPGA can be reprogrammable whereas if the channel simulator modeling in LabVIEW needs to be change or modify to match to the specific operating system. This can be made through the hardware description language inside FPGA called as VHDL and Verilog HDL.

Although the LabVIEW has its own programming language, which is a quite different to the FPGA language but this not need to be the main issues because there is module for FPGA to synthesizes the VHDL code for the FPGA during the compilation and installation. The channel simulator that has been built in LabVIEW is capable in taking place and synthesizing the HDL code when compiling the channel modeling onto FPGA directly [6-7]

The completed compilation summary of FPGA is shown in Figure 6. The implementation of FPGA takes several times which for this proposed channel simulator is about 12 minutes depending on the complexity of the design. The compilation takes several processes to transfer the channel simulator design in LabVIEW to FPGA such as the synthesizing, translating, mapping, placing/routing, generating program file and finally generating a Bitfile. After the process is completely done report of compilation obtain that can be seen in Figure 6.

Build Specifications	Status	End time
€ fpga (FPGA TARGET, lvproj/FPGA Targ	Complete	12:43:09 PM
	Reports Summary	
	Compilation completed successfully. Device Utilization Total Silces: 77.2% (370 out of 5120) Silce Registers: 77% (375 out of 10240) Silce LUTs: 5.1% (527 out of 10240) Biock RAMs: 0.0% (0 out of 40) Timing MiteClk (Used by non-diagram components): 33.00 MHz (76.22 MHz maxid 40 MHz Onboard Clock: 40.02 MHz (212.22 MHz maximum)	mum)
	Start Time: 12:38:32 PM End Time: 12:43:09 PM Total Time: 00:04:37	ŝ
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Figure 6 Report summary of compilation FPGA



Figure 7 FPGA as channel simulator

# **4.0 FUTURE WORKS**

Future work is required to optimize the time-scale channel simulator for communication system application by analyzing the data rate, symbol rate or frequency selection and others. Moreover, more parameter and specification need to be considered for wider applications.

# **5.0 CONCLUSION**

The time-scale channel simulator was designed and implemented on virtex of FPGA. The mathematical and statistical model based is employed to define the channel modeling and matching the channel design in LabVIEW software to the hardware FPGA. The implementation of FPGA takes several time and it done directly and automatically without requiring and connecting to the additional devices. The implementation of FPGA is successfully completed.

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