Jurnal Teknologi

Full Paper

DESIGN OF A 24.5 GHZ CMOS LOW NOISE AMPLIFIER USING 0.13-µM TECHNOLOGY FOR 6G WIRELESS APPLICATIONS

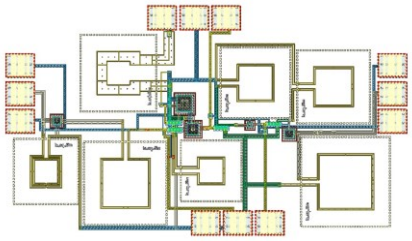
Sohiful Anuar Zainol Murad[a,b]*, Asrulnizam Abd Manaf[c], Nuha A. Rhaffor[c], Ruhaifi Abdullah[c]

[a]Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis, Arau, 02600, Perlis, Malaysia
[b]Centre of Excellence for Micro System Technology (MiCTEC), Universiti Malaysia Perlis, Arau, 02600, Perlis, Malaysia
[c]Collaborative Microelectronic Design Excellence Centre, Universiti Sains Malaysia, Gelugor 11800, Malaysia

Article history
Received
29 April 2024
Received in revised form
24 May 2024
Accepted
10 July 2024
Published Online
22 December 2024

*Corresponding author
sohiful@unimap.edu.my

Graphical abstract



Abstract

The need for high-performance circuit designs is growing as wireless communication technologies continue to advance and support newer generations of wireless applications. Much emphasis has been focused on the possibility of the 24 GHz frequency band in next-generation wireless networks, including 5G and beyond. Designing a low noise amplifier (LNA) operating at 24 GHz presents several challenges. The primary concerns include achieving high gain, low power consumption, low noise figure, and while maintaining good linearity and stability. This paper presents the design, simulation, and layout of a CMOS LNA optimized for operation at 24.5 GHz frequency, targeting 6G and beyond wireless communication applications. The proposed LNA employs three stages with a cascode topology at the first stage and follow by a common source stage at second and third stage. The three stages help to achieve high gain, and the source degeneration inductor at the first stage helps to improve linearity. Extensive simulations were conducted using a 0.13-µm CMOS technology, demonstrating a peak gain of 21 dB and a noise figure of 5.6 dB at 24.5 GHz. The LNA also exhibits good linearity and stability over a wide bandwidth. The performance metrics were validated through simulation and comparison, showcasing the feasibility of the designed LNA for 6G applications. This work contributes to the advancement of CMOS-based radio frequency (RF) front-end designs for next-generation wireless communication systems.

Keywords: Low noise amplifier, CMOS, 6G, RF front-end, wireless communication

Abstrak

Keperluan untuk reka bentuk litar berprestasi tinggi semakin berkembang apabila teknologi komunikasi tanpa wayar terus maju dan menyokong aplikasi tanpa wayar generasi baharu. Mereka bentuk penguat hingar rendah (LNA) yang beroperasi pada 24 GHz memberikan beberapa cabaran. Kebimbangan utama termasuk mencapai gandaan tinggi, angka hingar yang rendah, dan penggunaan kuasa yang rendah sambil mengekalkan kelelurusan dan kestabilan yang baik. Kertas kerja ini membentangkan reka bentuk, simulasi dan susun atur LNA CMOS yang dioptimumkan untuk operasi pada frekuensi 24.5 GHz, menyasarkan 6G dan seterusnya aplikasi komunikasi tanpa wayar. LNA yang dicadangkan menggunakan tiga peringkat dengan topologi kaskod pada peringkat pertama dan diikuti dengan peringkat punca sepunya pada peringkat

kedua dan ketiga. Tiga peringkat membantu untuk mencapai gandaan yang tinggi, dan pengaruh kemorosotan sumber pada peringkat pertama membantu meningkatkan kelelurusan. Simulasi ekstensif telah dijalankan menggunakan teknologi CMOS 0.13-µm, menunjukkan gandaan puncak 21 dB dan angka hingar 5.6 dB pada 24.5 GHz. LNA juga mempamerkan kelelurusan dan kestabilan yang baik pada lebar jalur yang luas. Metrik prestasi telah disahkan melalui simulasi dan perbandingan, mempamerkan kebolehlaksanaan LNA yang direka bentuk untuk aplikasi 6G. Kerja ini menyumbang kepada kemajuan reka bentuk bahagian depan frekuensi radio (RF) berasaskan CMOS untuk sistem komunikasi tanpa wayar bagi generasi akan datang.

Kata kunci: Penguat rendah hingar, CMOS, 6G, bahagian depan RF, komunikasi tanpa wayar

1.0 INTRODUCTION

Wireless communication technologies have evolved rapidly over the past few decades, from the early days of 1G analog systems to the current era of 5G networks, enabling unprecedented connectivity and innovation [1]. The internet of everything (IoE), three-dimensional (3D) media, virtual reality (VR), artificial intelligence (AI), enhanced mobile broadband (eMBB), machine-to-machine (M2M) communication and other developing applications and industries have evolved rapidly [2]. Significant limitations to the 5G mobile communication system are continually being revealed by its ongoing development. The idea behind it was to give the IoE more power. Nevertheless, the 5G system cannot provide a completely automated and intelligent network that allows IoE as a service due to capacity constraints [3]. By 2030, 5G will have reached its limit, which will force the creation of new paradigms to address the shortcomings of earlier generations of mobile networks. Therefore, the 6G wireless communication is predicted to surpass the limitations of fifth-generation (5G) with boosted data rates and speeds of wireless systems [3]. The significant data traffic fuelled by the rapid increase in connected devices demands higher bandwidth and low-latency data center interconnects [4], [5], [6].

The spectrum is a critical resource for wireless communication, providing the foundation for transmitting and receiving data wirelessly. As the demand for higher data rates and more efficient communication systems continues to rise, the allocation and utilization of spectrum become increasingly important, particularly in the context of future technologies like 6G [2]. While the exact frequency bands for 6G have yet to be fully defined, researchers and industry stakeholders are exploring various frequency ranges to accommodate the diverse requirements of 6G networks and applications. Unlike previous generations of wireless technology, which primarily focused on millimeter-wave (mmWave) and sub-6 GHz bands, 6G is expected to leverage a much broader spectrum, including terahertz (THz) frequencies.

Table 1 shows the spectrum overview for future generation wireless communication for 6G applications. Clearly, compared with the crowded sub-6 GHz band, the spectrum beyond 24 GHz has the feature of broad bandwidth, making it possible to realize high speed throughput in 5G new radio (NR) and future 6G applications [7]. 6G will utilize frequency range 1 (FR1) up to 7.125 GHz and frequency range 2 (FR2) mmWave from 24.25 GHz to 71 GHz, much to the 5G New Radio standard. Moreover, THz frequencies and frequencies between 7.125 GHz and 24.25 GHz, often referred to as FR3 or FR2-0 seem to be used by 6G, according to recent study [8].

The bandwidth of 6G wireless communications is still under development and specification, as 6G technology is expected to be commercially available around 2030 [2]. However, according to current research and early projections, 6G is expected to offer significantly higher bandwidths than earlier generations. Although 6G's precise specifications are still being worked out, it is clear that the bandwidth of 6G wireless communications will be significantly higher than that of 5G, utilizing sub-THz and THz frequency bands to provide channel bandwidths potentially up to 100 GHz or more. This will represent a significant advancement in wireless communication technology by enabling previously unheard-of data speeds and supporting a broad range of cutting-edge applications and services.

An essential part of the mm-wave front-end, the LNA is the first active component in the RF wireless receiver. Due to its simultaneous need for high gain, low noise, and high operating frequency, the LNA is one of the most important and difficult blocks of a mm-wave front-end [9]. As a result, the LNA significantly affects the receiver's overall system performance [10]. The RF performances of the LNA are significantly influenced at mm wave frequencies by the passive components that make up the LC load, matching network, and degenerative inductor. Since the LNA controls the radio sensitivity, it is always anticipated to achieve a particular gain without adding much noise as a crucial component of the radio frequency front-end module [8]. Lately, more researchers have focused on LNA for 5G applications

[11-14]. However, the development of CMOS LNAs for 6G applications is still in its early stages and more research is necessary. While CMOS technology has made significant advancements in recent years, achieving the stringent performance requirements, such as high linearity, low noise figure, and wide bandwidth, for 6G LNAs remains a challenge [15]. Traditional CMOS processes have limitations in terms of intrinsic noise and linearity compared to other semiconductor technologies like GaAs or InP. Moreover, the push towards higher frequencies and data rates in 6G exacerbates these challenges.

Table 1 Spectrum overview for future generation wireless communication

Frequency range type	Technology	Frequency range	Applications
FR1 (low-band)	4G/5G/6G	600, 700, 800, 900 MHz	Broad coverage & IoT
	6G	470-694 MHz	
FR1 (mid-band)	4G/5G/6G	1.5,1.8, 2.1, 2.3, 2.6 GHz	
	5G/6G	2.5-7.1 GHz	
FR2 (mmWave)	5G/6G	24-52 GHz, 57-71 GHz	Medium coverage and capacity enhacement
FR3 (Upper mid-band)	5G-Adcanced / 6G	7-24 GHz	Urban macro & micro coverage
FR THz (sub-THz)	6G	130-174.8 GHz 92-114.25 GHz	Peak capacity, high precision sensing, communication on-chips

In this paper, we propose a design of CMOS LNA at 24.5 GHz for 6G applications aimed at achieving higher gain. The proposed LNA employs three stages which the first stage is a cascode structure, while the second stage and the third stage are common source topologies to achieve sufficient gain. Section 2.0 describes the proposed CMOS LNA, detailing the architecture and circuit topology. Section 3.0 provides the comparative analysis with simulation results of the LNA, followed by a discussion and comparison results with similar works. Further, the layout is describes in Section 4.0. Finally, the paper concludes with Section 5.0, summarizing the key findings and contributions of this work.

2.0 METHODOLOGY

In LNA design, transistor sizing is a critical aspect that involves trade-offs between noise, gain, linearity, power consumption, and bandwidth. Designers often use smaller transistors to achieve higher frequency performance and lower noise figures but must be cautious about linearity and power handling capabilities. Conversely, larger transistors might be chosen for their robustness and better performance at lower frequencies and higher power levels. Ultimately, the optimal transistor size is determined by the specific requirements of the application, necessitating a careful balance of these factors.

Therefore, the transistor size needs to be properly optimized to achieve high performance. Figure 1 shows the transistor model 1.2V RF NMOS model with 5 terminals in the PDK 130 nm CMOS technology process with the nwell tap connected to VDD. This model has geometries range width 1 µm to 10 µm and number of fingers 1 to 64. The maximum supply voltage for this transistor model is 1.2 V, while the biasing voltage is more than 0.5 V for the transistor to work in a saturation region.

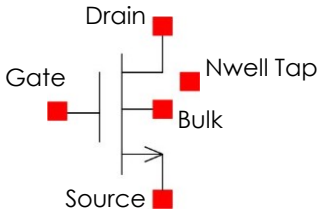


Figure 1 Transistor model 1.2V RF NMOS

The proposed LNA aims for 6G applications that offer ultra-fast data rates, low latency, high reliability, and wide coverage. This LNA design is intended to achieve high gain specification. The higher the gain, the better the signal transmission from LNA to another device in the receiver chain. Meanwhile, the NF value should be reduced to reduce losses and improve performance. The input third-order intercept point (IIP3) needs to be set close to zero for better performance. Meanwhile, the power consumption should be low. Table 2 shows the design specification of the proposed LNA. All the parameters' values are set based on the literature review in [1-6]. There will, however, will be trade-offs between all parameters. These specifications guide the design process to ensure the CMOS LNA meets the performance requirements for 6G wireless applications.

Table 2 Design specification of the proposed LNA for 6G

Parameter	Specification
Operating frequency	Up to 30 GHz
Gain (S21)	> 20 dB
Noise Figure (NF)	< 5 dB
Input matching (S11)	< -10 dB
Output matching (S22)	< -10 dB
Reverse isolation (S12)	< -20 dB
Third-order intercept point (IIP3)	> -10 dBm
Power consumption	< 50 mW
Stability factor (Kf)	> 1

The proposed CMOS low noise amplifier (LNA) for 6G technology is shown in Figure 2. The proposed LNA is designed using CMOS 0.13-µm process technology. The LNA employs three stages to achieve high gain at 24.5 GHz. The first stage is a cascode structure where the output of common source (CS) is connected to the input of common gate (CG). The cascode structure has a very high reverse isolation factor and provides a sizable output gain. Because of its higher input-output isolation, higher gain with bandwidth, and higher input-output impedance, the cascode topology is more resilient [16]. Meanwhile, the second and third stages are common-source amplifiers. The combination of cascode and cascade structure provides significant advantages, including enhanced gain, improved noise figure, increased stability, flexibility in design, better linearity, and improved impedance matching especially at higher frequency. These benefits make the cascode and cascade structures has been chosen for LNA design at 24.5 GHz.

The gain for a cascode structure is the product of the gains of the CS and CG stage as expressed in equation (1) as follows:

$$A_{v1} = g_{m1} \times r_{01} \times \left(\frac{g_{m2} \times r_{02}}{1 + g_{m2} \times r_{02}}\right) \quad (1)$$

where r_{01} and r_{02} are the output resistances of the CS and CG, respectively. Meanwhile, the gain of a cascade structure can be determined by the gain contributions from each of the cascade. The gain of a single CS amplifier stage is given by:

$$A_{v,i} = -g_{mi} \times (r_{0i} // R_{L,i}) \quad (2)$$

where r_{0i} is the output resistance of the transistor in stage $\boldsymbol{i}$ and $R_{L,i}$ is the load resistance seen by stage $\boldsymbol{i}$. The overall gain of a cascade CS amplifier is the product of the gains of each individual stage is given by equation (3):

$$A_{v,total} = A_{v1} \cdot A_{v2} \cdot \cdots \cdot A_{vn} \quad (3)$$

where $\boldsymbol{n}$ is number of stages. Therefore, the overall gain of the cascade is:

$$A_{v,total} = A_{v2} \cdot A_{v3} = (-g_{m2} \times (r_{02} // R_{L,2})) \cdot (-g_{m3} \times (r_{03} // R_{L,3})) \quad (4)$$

where A_{v1} and A_{v2} is a gain at stage 2 and stage 3, respectively. Therefore, the overall gain consists of three stages are given as:

$$A_{v,overall} = A_v \cdot A_{v,total} = g_{m1} r_{01} \times \left(\frac{g_{m2} r_{02}}{1 + g_{m2} r_{02}}\right) \cdot (-g_{m2} \times (r_{02} // R_{L,2})) \cdot (-g_{m3} \times (r_{03} // R_{L,3})) \quad (5)$$

As illustrated in Figure 2, M1 and M2 transistors makes the first cascode stage of the three stage LNA. The total width of M1 and M2 200 µm and 150 µm, respectively. Both transistors are set at 64 fingers. In order to minimize the Miller effect of M1 and achieve strong reverse isolation, the cascode topology is utilized in the initial stage. The transistor size is optimized to achieve high trasconductance, g_m for maximum gain.

Ls is employed at the source of M1 to supply the input more resistive and lower ohmic for impedance matching in order to improve the circuit linearity and stability. Furthermore, Ls can accomplish the design objectives of noise and input impedance matching at the same time. Moreover, Ls does not significantly impair the NF performance. Nevertheless, the amplifier's gain decreases as Ls increases. As a result, 80 fH is the value of Ls in this design.

The input matching network is designed using inductors L1, L2 and capacitors C1, C2 to be matched at 50 Ω. S-parameter analysis is used to optimize the values so that the input matching (S11) is targeting to be less than -10 dB. Therefore, the values of L1, L2, C1 and C2 are 890 pH, 479 pH, 170 fF and 400 fF are chosen. The RF choke inductor L3 with a value of 0.14 nH is connected to the supply voltage (Vdd) at 1.2 V and the M2 is biased through resistor R3. In order to separate bias (supply) noise from entering the LNA and stabilize the bias voltage (supply voltage), the bypass capacitor C3 is put between the gate of M2 and ground.

The second and third stages is designed to increase more gain. Therefore, a common source was chosen to offer adequate gain at 24.5 GHz. The M3 and M4 transistors with sizes of 75 µm / 0.13 µm and 64 µm / 0.13 µm, respectively are chosen to boost the gain. The number of fingers for both transistors is set at 64. The RF choke inductors L4 and L5 are optimized to be resonant at 24.5 GHz. Therefore, both L4 and L5 are tuned at 0.3 nH.

The capacitors C4 at 1 pF and C5 at 80 fF are integrated into the interstage matching network at the second and third stages to deliver maximum gain in the output stage. The output-matching network is designed using the LC network. Similar with the input matching, the output matching (S22) is optimized, typically targeting S22 to be less than -10 dB. Therefore, C6 and L6 is optimized at 0.5 pF and 0.56 nH, respectively. A parallel LC resonant network replaces the traditional transmission line in the output matching, enabling proper output matching at 50 Ω with high gain at the desired frequency. The biasing resistor is optimized to set the desired gate to source voltage (Vgs) and drain current (ID) for transistors properly operate. Thus, the resistors R1 and R2, which are set at 2.5 kΩ and 528 Ω, respectively, make up the entire biasing network. While both R3 and R4 are 1 kΩ. The optimized components parameters of the proposed LNA are given in Table 3.

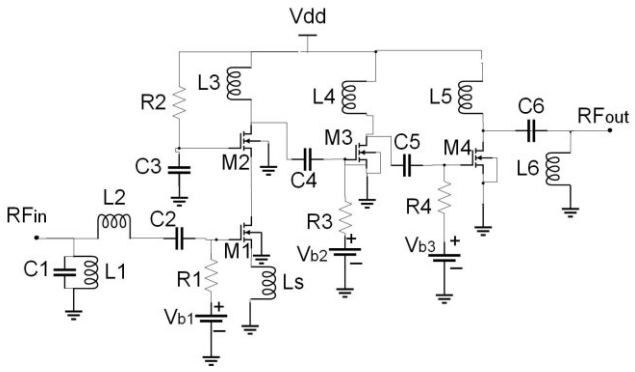


Figure 2 The proposed LNA at 24.5 GHz for 6G

Table 3 Component parameters for LNA

Components	Values	Components	Values
M1*	200 µm/130 nm	C3	2 pF
M2*	150 µm/130 nm	L3	0.3 nH
M3*	75 µm/130 nm	C4	1 pF
M4*	64 µm/130 nm	L4	0.3 nH
R1	2.5 kΩ	C5	80 fF
R2	582 Ω	L5	332.5 pH
R3	1 kΩ	C6	0.5 pF
R4	1 kΩ	L6	0.56 nH
C1	170 fF	Vdd	1.2 V
L1	890 pH	Vb1	500 mV
Ls	80 fH	Vb2	650 mV
C2	400 fF	Vb3	600 mV
L2	479 pH		

* Number of fingers = 64

3.0 RESULTS AND DISCUSSION

The cadence virtuoso tool is used to simulate the proposed LNA. The proposed LNA's supply voltage is set at 1.2 V to reduce power consumption. Meanwhile, the biasing at the first stage, second stage, and third stage is 500 mV, 650 mV, and 600 mV, respectively. The LNA draws a total current of 26 mA.

Figure 3 shows the small-signal gain S21 of the transistor model 1.2V RF NMOS. The width's size is varied from 1 µm to the maximum value of 10 µm and the number of fingers is fixed at 64. It can be seen that the gain of 8 dB is achieved at 24.5 GHz with 1.2 V supply voltage. The gain is decreased when the frequency is increased. Therefore, the size of the transistors is optimized between 1 µm and 5 µm in order to achieve high gain in the proposed LNA as depicted in Table 3.

Meanwhile, Figure 4 shows the gain characteristics for the cascade and cascode structures of the circuit design. The cascode structure achieved higher gain as compared to the cascade structure from 5 GHz to 50 GHz. As can be observed, the cascode structure gain is 8 dB and the cascade structure gain is only 4 dB at 24.5 GHz. Therefore, the cascode structure is used in the proposed LNA design at the first stage to achieve high gain and improve stability. Meanwhile, the cascade structure is employed at the second and third stages to improve linearity and achieve low power consumption. By properly optimizing the input and output matching, transistor size, and biasing in the LNA circuit, a total gain of more than 16 dB is expected to be achieved at targeted frequency.

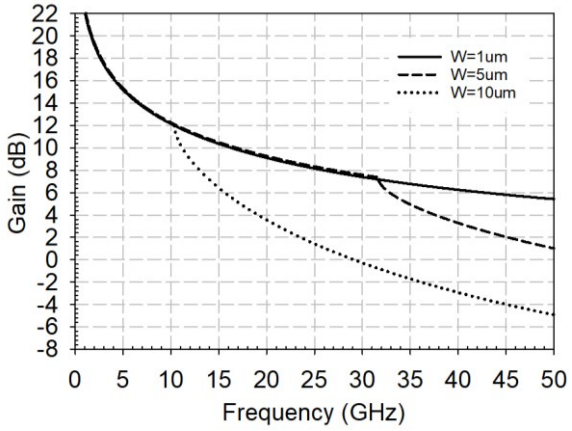


Figure 3 Gain versus transistor's width (number of fingers = 64)

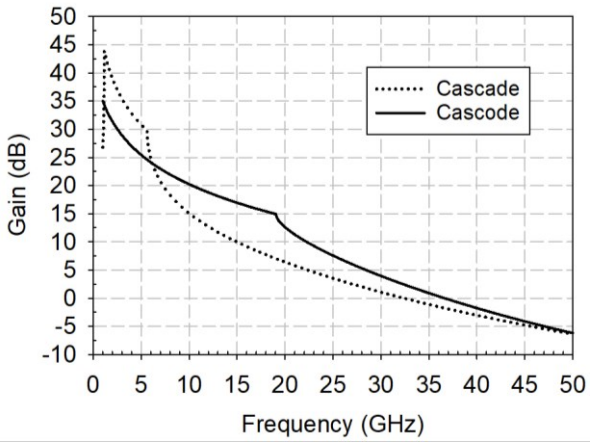


Figure 4 Gain characteristics of cascade and cascode structures for circuit design

The s-parameter results are depicted in Figure 5. As can be seen, the proposed LNA has demonstrated 21 dB gain (S21) at the peak gain frequency of 24.5 GHz. Furthermore, the input return loss (S11) and output return loss (S22) of -27 dB and -25 dB is achieved, respectively. The appropriate impedance matching of the input and output matching networks is shown by the curves S11 and S22, respectively.

In LNA design, S12 is one of the scattering parameters (S-parameters) that characterize the behavior of the amplifier in the frequency domain. Specifically, S12 represents the reverse isolation of the amplifier. Low values are desirable as they indicate minimal reverse transmission, which is crucial for stability, performance, and ensuring that the amplified signal remains clean and undistorted.

Figure 6 shows S12 of the proposed LNA at 24.5 GHz. The S12 of -45 dB is achieved which is very low indicating good reverse isolation.

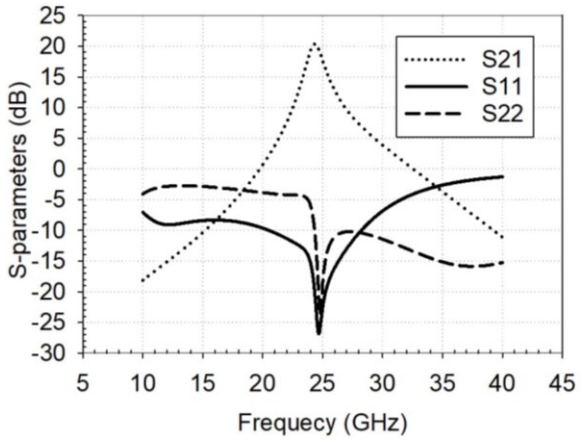


Figure 5 S-parameter of the proposed LNA at 24.5 GHz

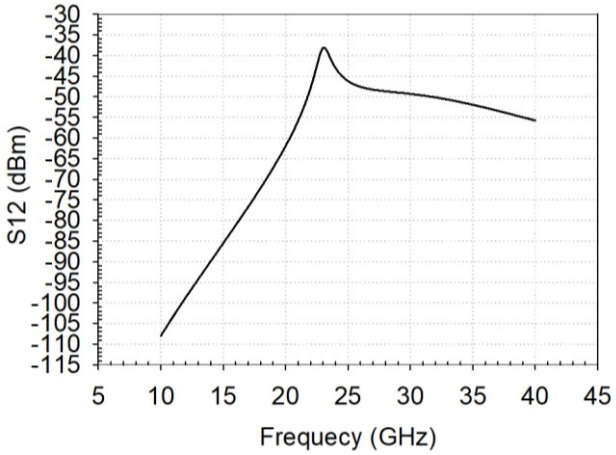


Figure 6 Reverse isolation S12 of the proposed LNA

The noise figure (NF) of an RF amplifier provides information about its noise performance. The NF displays the distorted signal. A higher NF results in more signal corruption. As a result, while creating an LNA, a lower NF is always considered. Decibels are used to measure it. The NF can be represented by the equation (6) [17].

$$NF=10logF\ dB \quad (6)$$

where F is noise Factor. Figure 7 shows the noise figure curve of the LNA achieved in the simulation. The curve shows a dip at 24.5 GHz frequency. As can be seen, the noise figure of 5.6 dB is achieved at the frequency 24.5 GHz. The noise is quite high due to the trade-off between the gain and the number of stages as given in equation (7).

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} \quad (7)$$

where *F* and *G* are the noise factor and gain at each amplifier stage.

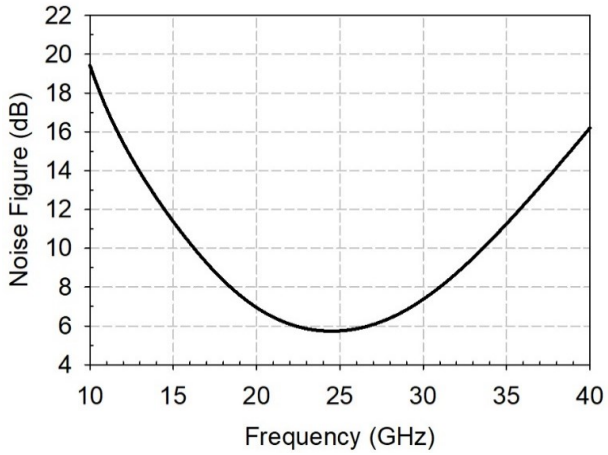


Figure 7 Noise figure of the proposed LNA

Determining the linearity of an LNA involves evaluating its ability to amplify signals without introducing significant distortions or nonlinearities. A commonly used methods and techniques to assess the linearity of an RF CMOS LNA is two-tone test of third-order intercept point (IIP3) and 1 dB compression point (P1dB) [18]. Higher IIP3 and P1dB values indicate better linearity.

To verify that the LNA met the linearity criteria, a two-tone test for the third-order intercept point (IIP3) was run. Equal power was supplied to the two tones at 24.50 GHz and 24.51 GHz, respectively. The IIP3 is shown in Figure 8 in relation to the swept input power, which ranges from -40 dBm to 10 dBm. The simulation findings indicate that an IIP3 of -2 dBm is attained. The design has been optimized to obtain the best IIP3 value by fine tuning the inductor Ls in the circuit.

Figure 9 shows 1 dB compression point. As can be seen, the 1 dB point is achieved at -14 dBm which the gain of LNA decreases by 1 dB from its linear region.

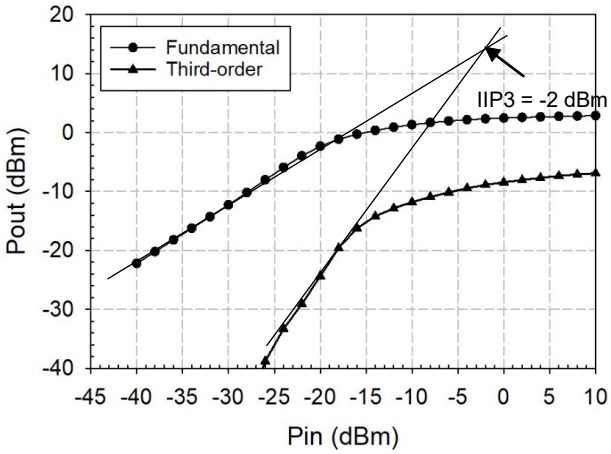


Figure 8 IIP3 of LNA

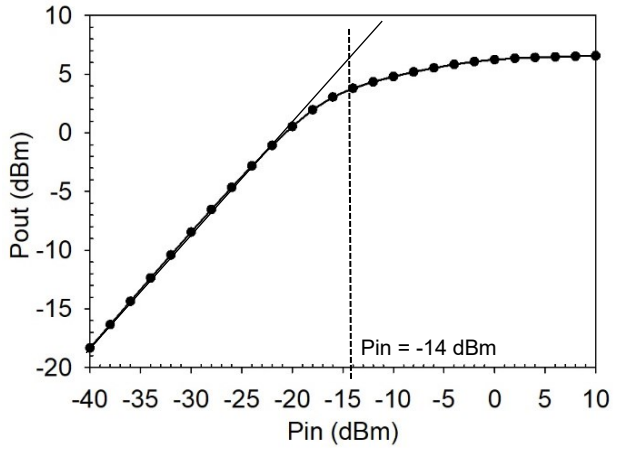


Figure 9 1dB compression point of LNA

For LNAs, stability is a critical concern. Major features including as bandwidth, noise, gain, linearity, power consumption, and impedance matching can be severely compromised in an unstable LNA, rendering it worthless. By using the S-parameter and signal flow theory, which demonstrate the Rollet's factor, provided by [1], there is good stability (unconditionally stable) for this design:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \times |S_{12}||S_{21}|} \quad (8)$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. Figure 10 illustrates the unconditional stability requirements of LNA, which are K >1 and $|\Delta| < 1$.

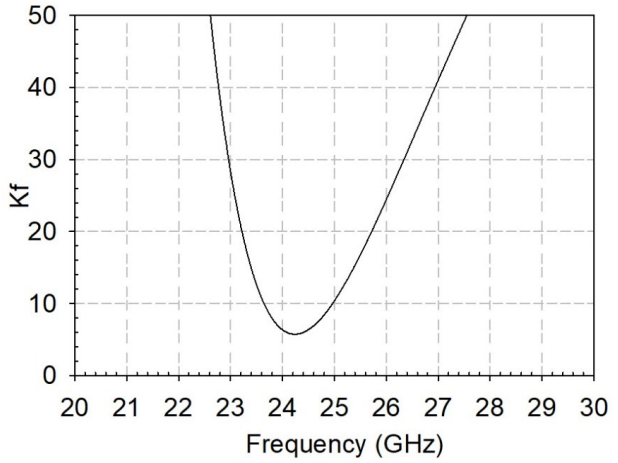


Figure 10 Stability of LNA

Table 4 compares the state-of-the-art LNA's performance. The three-stage LNA for 6G outperforms other circuits in terms of gain and linearity when compared to earlier studies as indicated in Table 4. The proposed work in [19] and [20] achieved the lowest gain and high linearity among other works, respectively. Meanwhile, linearity is not measured in [23]. In addition, [19] and [23] used differential architecture which required input and output balun. The gain achieved in [22] is 21.8 dB with a low IIP3. Therefore, the proposed LNA achieved high gain and good linearity while other performances are comparable with other works. However, the proposed LNA achieved high noise compared to other works due to the implementation of three stages LNA. The current reused is employed in [22] to reduce noise and a simple input matching network consisting of parallel line and series line was used to optimum noise in [20].

Table 4 Performance summary and comparison of CMOS LNA

Reference	[19]	[20]	[21]	[22]	[23]	This work
CMOS Tech. (nm)	180	22	40	55	45	130
Freq. (GHz)	24	28	28	22.6	27.4	24.5
Vdd (V)	3.0	1.6	1.0	1.2	1.8	1.2
Gain (dB)	10.27	24.8	20.3	21.8	12	21
S11 (dB)	-15.6	-8	-15	-40	-17	-27
S22 (dB)	-11.7	-20	NA	-15	-13	-25
NF (dB)	3.3	3.6	2.86	4.04	2.9	5.6
IIP3 (dBm)	11.68	-15	-7	-15	NA	-2
Pdc (mW)	17.8	13.6	7.4	3.05	17.3	31.2
Area (mm^2)	0.37	0.31	0.19	0.34	NA	0.71
No. of stages	1*	3	2	3	1*	3

*Differential topology

In practice, extra attention needs to be taken during the layout stage in order to get the appropriate LNA performance. Several helpful techniques can be used to increase the degree of similarity between the estimated and experimental performance parameters. The connector lines are a crucial layout element that must be kept to a minimum. In addition, the cross line needs to be avoided in order to reduce the parasitic capacitance. If it is not possible to prevent this, then the cross lines should be shielded from one another to prevent unpleasant feedback. The top metal layer (Mettop) is used whenever possible to further reduce the connection loss, as is stacking the top two metal layers because of its low resistivity.

The layout of the proposed LNA is depicted in Figure 11. The chip occupies a total area of 0.71 mm^2 including pads. The RF GSG pads on left and right side are the input and output pads. The biasing voltages are arranged on the top and bottom sides. To prevent unintended coupling, guard rings were positioned at each inductor in this design. The transistors were organized with the lowest finger width allowed by the technology. Furthermore, in order to reduce access poly resistance and raise the cascode cell's noise figure, the gates were connected on both sides. The connection between the M2 transistor's gate and Vdd pad was done with

extra caution since the LNA may become unstable if the gate detects an inductive impedance.

Iterative layout design was used to make the design compact. To minimize loss, all signal routings were minimized. Because of its low resistance, the top metal layer is employed for routing whenever practical. MIM capacitors are used in supply decoupling to create a strong AC ground. The self-resonant frequencies of these MIM capacitors are higher than the desired frequency due to their unique construction.

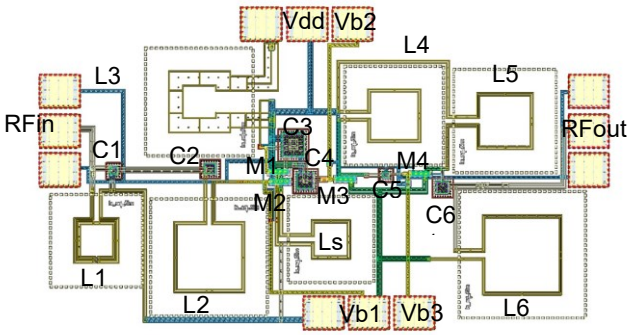


Figure 11 Layout of the proposed LNA in 0.13-µm technology

4.0 CONCLUSION

In this paper, three stage LNA for 24.5 GHz frequency is successfully designed and simulated. The circuit is designed in cadence virtuoso using 0.13-µm CMOS technology and simulated using a spectre simulator. A cascode single-stage amplifier with inductive degeneration load has been designed first. Then, two CS stage is connected in cascaded manner to make the three stage LNA. The designed LNA achieves a power gain of 21 dB at 24.5 GHz, the minimum noise figure of 5.6 dB, with 31.2 mW power consumption at 1.2 V supply voltage. A complete layout of LNA occupies a total area of 0.71 mm^2 including pads. These results provide staunch support for the effectiveness of the proposed work in 24.5 GHz receiver designs and can be extended to include electrostatic discharge (ESD) protection circuit for reliability. This 6G LNA is primarily intended for usage in a variety of wireless applications in cellular phones, GPS devices, wireless local area networks (Wi-Fi), and satellite communications.

Acknowledgement

The authors would like to express their sincere gratitude to Universiti Malaysia Perlis for granting Sohiful Anuar Zainol Murad a sabbatical leave for completing this research. This dedicated time away from regular duties provided invaluable opportunity and flexibility to focus on this work. We would also like to acknowledge the generous support and resources provided by the Center of Excellence for Microelectronics Design Collaboration (CEDEC) USM. The facilities and expertise available at CEDEC significantly contributed to the successful completion of this study.

Conflicts of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper.

References

[1] Giordani, M., Polese, M., Mezzavilla, M., Rangan, S. and Zorzi, M. 2020. Toward 6G Networks: Use Cases and Technologies. *IEEE Communications Magazine*. 58: 55–61. Doi: http://dx.doi.org/10.1109/MCOM.001.1900411

[2] Banafaa, M., Shayea, I., Din, J., Azmi, M. H., Alashbi, A., Daradkeh, Y. I. and Alhammadi, A. 2023. 6G Mobile Communication Technology: Requirements, Targets, Applications, Challenges, Advantages, and Opportunities. *Alexandria Engineering Journal*. 64: 245–274. Doi: http://dx.doi.org/10.1016/j.aej.2022.08.017.

[3] Saad, W., Bennis, M. and Chen, M., 2019. A Vion of 6G Wireless Systems: Applications, Trends, Technologies, and Open Research Problems. *IEEE Network*. 34: 134–142. Doi: http://dx.doi.org/10.1109/MNET.001.1900287.

[4] Boccardi, F., Heath, R. W., Lozano, A., Marzetta, T. L. and Popovski, P. 2014. Five Disruptive Technology Directions for 5G. *IEEE Communications Magazine*. 52: 74–80. Doi: http://dx.doi.org/10.1109/MCOM.2014.6736746.

[5] Heydari, P. 2021. April. Transceivers for 6G Wireless Communications: Challenges and Design Solutions. 2021 *IEEE Custom Integrated Circuits Conference (CICC)* (pp. 1–8). IEEE. Doi: http://dx.doi.org/10.1109/CICC51472.2021.9431450.

[6] Rodwell, M. W., Ahmed, A. S., Seo, M., Soylu, U., Alizadeh, A. and Hosseinzadeh, N. 2022. IC and Array Technologies for 100-300GHz Wireless. *2022 IEEE Custom Integrated Circuits Conference (CICC)*. (pp. 01–05). IEEE. Doi: http://dx.doi.org/10.1109/CICC53496.2022.9772844.

[7] Hong, W., Jiang, Z. H., Yu, C., Hou, D., Wang, H., Guo, C., Hu, Y., Kuai, L., Yu, Y., Jiang, Z. and Chen, Z. 2021. The Role of Millimeter-wave Technologies in 5G/6G Wireless Communications. *IEEE Journal of Microwaves*. 1: 101–122. Doi: http://dx.doi.org/10.1109/JMW.2020.3035541.

[8] Fu, J., Bardeh, M. G., Paramesh, J. and Entesari, K. 2022. A Millimeter-Wave Concurrent LNA in 22-nm CMOS FDSOI for 5G Applications. *IEEE Transactions on Microwave Theory and Techniques*. 71: 1031–1043. Doi: http://dx.doi.org/10.1109/TMTT.2022.3219869.

[9] Xu, X., Schumann, S., Ferschischi, A., Finger, W., Carta, C. and Ellinger, F. 2021. A 28 GHz and 38 GHz High-gain Dual-band LNA for 5G Wireless Systems in 22 nm FD-SOI CMOS. *2020 15th European Microwave Integrated Circuits Conference (EuMIC)*. (pp. 77–80). IEEE.

[10] Azizan, A. and Murad, S. A. Z. 2016. A 0.3 mW 2.4 GHz Low Power Low Noise Amplifier Using Forward Body Bias Technique for Wireless Sensor Ard Body Bias Technique for Wireless Sensor Network. *Jurnal Teknologi*. 78(1). Doi: http://dx.doi.org/10.11113/jt.v78.4172.

[11] Roobert, A. A., Rani, D. G. N., Divya, M. and Rajaram, S. 2018. February. Design of CMOS based LNA for 5G Wireless Applications. *Proceedings of the 6th International Conference on Communications and Broadband Networking*. (pp. 43–47). Doi: http://dx.doi.org/10.1145/3193092.3193095

[12] Chang, J. F. and Lin, Y. S. 2021. A 13.7-mW 21–29-GHz CMOS LNA with 21.6-dB gain and 2.74-dB NF for 28-GHz

5G Systems. *IEEE Microwave and Wireless Components Letters.* 32: 137–140.
DOI: http://dx.doi.org/10.1109/LMWC.2021.3121020.

[13] Choi, H. W., Choi, S. and Kim, C. Y. 2020. A CMOS Band-pass Low Noise Amplifier with Excellent Gain Flatness for mm-wave 5G Communications. *2020 IEEE/MTT-S International Microwave Symposium (IMS)*. (pp. 329–332). IEEE.
Doi: http://dx.doi.org/10.1109/IMS30576.2020.9224097.

[14] Roobert, A. A. and Rani, D. G. N. 2021. Design and Analysis of a Sleep and Wake-up CMOS Low Noise Amplifier for 5G Applications. *Telecommunication Systems*. 76: 461–470.
Doi: http://dx.doi.org/10.1007/s11235-020-00729-y.

[15] R. Zhang, Y. Huang, and W. Ng. 2020. CMOS Low Noise Amplifiers for 5G and Beyond: Challenges and Opportunities. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems.* 10: 455–468.

[16] Sathya, R. and Ambulker, S. 2023. Analysis of Three-Stage LNA Architecture for CMOS RF Front End. *Journal of Physics: Conference Series*. 2466(1): 012017. IOP Publishing.
Doi: http://dx.doi.org/10.1088/1742-6596/2466/1/012017.

[17] Mugadhanam, R. and Uppara, E. 2022. Design and Analysis of Improved 3-Stage LNA Architecture for CMOS RF Front End Receiver Systems. *International Journal of Intelligent Engineering & Systems*. 15.

[18] Zhang, H., Fan, X. and Sinencio, E. S. 2009. A Low-power, Linearized, Ultra-wideband LNA Design Technique. *IEEE Journal of Solid-State Circuits*. 44: 320–330.
Doi: http://dx.doi.org/10.1109/JSSC.2008.2011033.

[19] Ajabi, S. and Kaabi, H. 2022. A 24GHz High Dynamic Range Low-Noise Amplifier Design Optimization Methodology and Circuit Configuration. Iranian Journal of Science and Technology. *Transactions of Electrical Engineering.* 46: 225–234.
DOI: http://dx.doi.org/10.1007/s40998-021-00450-9.

[20] Xu, X., Li, S., Szilagyi, L., Testa, P.V., Carta, C. and Ellinger, F. 2020. A 28 GHz and 38 GHz dual-band LNA using Gain Peaking Technique for 5G Wireless Systems in 22 nm FD-SOI CMOS. *2020 IEEE Asia-Pacific Microwave Conference (APMC)*. (pp. 98–100). IEEE.
DOI: http://dx.doi.org/10.1109/APMC47863.2020.9331333.

[21] Roobert, A. A., Arunodhayamary, P. S., Rani, D. G. N., Venkatesh, M. and Julus, L. J. 2022. Design and Analysis of 28 GHz CMOS Low Power LNA with 6.4 dB Gain Variability for 5G Applications. *Transactions on Emerging Telecommunications Technologies.* 33: p.e4486.
DOI: http://dx.doi.org/10.1002/ett.4486.

[22] Liang, C., Tang, B., Zhao, Y., Xie, Y. and Geng, L. 2023. High Gain and Low Power K-Band LNA With Reversed Current-Reuse Topology. *IEEE Microwave and Wireless Technology Letters.*
Doi: http://dx.doi.org/10.1109/LMWT.2023.3317781.

[23] Lammert, V., Weigel, R. and Issakov, V. 2020, May. A Highly Linear Low-Power 28 GHz LNA in 45nm SOI-CMOS using the Modified Derivative Superposition Method for IM3-Cancellation. *2020 IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)*. (pp. 1–3). IEEE.
DOI: http://dx.doi.org/10.1109/WMCS49442.2020.9172390.