Jurnal Teknologi

Full Paper

OPTIMIZATION OF PROCESS PARAMETERS FOR GOLD-DOPED SILICON IN RF APPLICATION

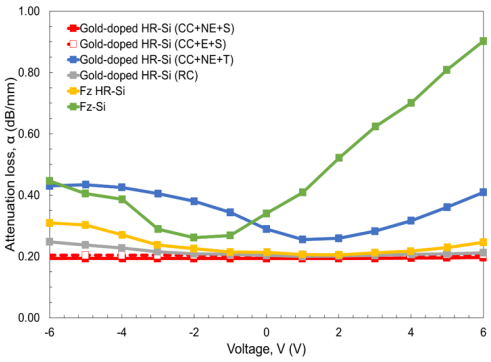
Nur Zatil Ismah Hashim[a]*, Sofiyah Sal Hamid[b], Nuha A. Rhaffor[b], Mohamad Adzhar Md Zawawi[a]

[a]School of Electrical and Electronic Engineering, Engineering Campus, USM, 14300, Nibong Tebal, Penang, Malaysia
[b]Collaborative Microelectronic Design Excellence Centre (CEDEC), USM, 11900, Bayan Lepas, Penang, Malaysia

Article history
Received
17 September 2024
Received in revised form
23 December 2024
Accepted
12 February 2025
Published Online
24 October 2025

*Corresponding author
zatil.hashim@usm.my

Graphical abstract



Abstract

Gold-doped high resistivity silicon has shown potential as advanced RF substrate through improved substrate resistivity and RF performances. However, the substrate demonstrates non-linear behavior, indicating insufficient traps to fully pin the Fermi level to intrinsic level. To date, charge-trapping mechanism of the substrate has not been fully understood. This study aims to highlight the effects of process variations in the development of gold-doped high resistivity silicon on the DC and RF performances to gain a deeper insight into the charge-trapping mechanism associated with the substrate. Double-stage activation annealing consists of controlled cooling and rapid cooling illustrates higher resistivity compared to single-stage annealing, with more than 50% increase. In addition to that, CPW losses demonstrate lower dependency on DC bias, reflected by its $\alpha_{max}/\alpha_{min}$ ratio of 1.01 as compared to 1.24 for single-stage annealing. Through this work, it was also found that the substrate is sensitive to high-temperature processing, indicated by the higher $\alpha_{max}/\alpha_{min}$ loss ratio on thermally oxidized substrate, most likely due to the insufficient traps to compensate for the additional thermal generated carriers. Additionally, the removal of gold layer at the silicon surface was unwarranted from the RF perspective, portrayed by the higher CPW losses.

Keywords: High resistivity silicon, gold-doped silicon substrate, RF substrate, parasitic surface conduction (PSC)

Abstrak

Silikon kerintangan tinggi dop emas telah menunjukkan potensi sebagai substrat RF termaju melalui kerintangan substrat dan prestasi RF yang lebih baik. Walau bagaimanapun, substrat menunjukkan tingkah laku bukan linear, menunjukkan perangkap tidak mencukupi untuk menyemat sepenuhnya tahap Fermi kepada tahap intrinsik. Sehingga kini, mekanisme penangkapan cas substrat belum difahami sepenuhnya. Kajian ini bertujuan untuk menyerlahkan kesan variasi proses dalam pembangunan silikon kerintangan tinggi dop emas pada prestasi DC dan RF untuk mendapatkan gambaran yang lebih mendalam tentang mekanisme perangkap cas yang dikaitkan dengan substrat. Penyepuhlindapan pengaktifan dua peringkat terdiri daripada penyejukan terkawal dan penyejukan pantas menggambarkan kerintangan yang lebih tinggi berbanding penyepuhlindapan satu peringkat, dengan peningkatan lebih daripada 50%. Di samping itu, kerugian CPW menunjukkan pergantungan yang lebih rendah pada bias DC, dicerminkan

oleh nisbah $\alpha_{max}/\alpha_{min}$ 1.01 berbanding 1.24 untuk penyepuhlindapan satu peringkat. Melalui kerja ini, ia juga didapati bahawa substrat adalah sensitif kepada pemprosesan suhu tinggi, ditunjukkan oleh nisbah kehilangan $\alpha_{max}/\alpha_{min}$ yang lebih tinggi pada substrat teroksida terma, kemungkinan besar disebabkan oleh perangkap yang tidak mencukupi untuk mengimbangi pembawa terjana haba tambahan. Selain itu, penyingkiran lapisan emas pada permukaan silikon adalah tidak wajar dari perspektif RF, yang digambarkan oleh kerugian CPW yang lebih tinggi.

Kata kunci: Silikon berintangan tinggi, substrat silikon didopkan emas, substrat RF, konduksi permukaan parasit (PSC)

1.0 INTRODUCTION

The continuous development on high resistivity substrates in analog, digital and mixed signals RF integrated circuits have been discussed in the International Roadmap for Devices and Systems (IRDS) under Emerging Materials Integration section [1]. High resistivity substrate in the context of RFIC application is defined as substrates with resistivity values greater than 4 kOhm.cm [2,3]. Due to its maturity, plentitude and compatibility with CMOS processes, elemental silicon (Si) technology observes never-ending advancements as potential RFIC substrate candidate, offering high resistivity option (HR-Si) [4-6].

Despite its growing potential, HR-Si suffers from parasitic surface conduction (PSC) [7]. It is a non-ideal phenomenon originated from the formation of highly conductive layer at the silicon surface. Under electric field application, charge carriers move towards or away from the surface, depending on the polarity of the applied field and the type of substrate used (whether N-type or P-type), inducing accumulation, depletion and inversion at the surface. The conductive layer is formed when the substrate is under accumulation and inversion, due to the movements of majority carriers and minority carriers towards the surface, respectively. The existence of this conductive layer contributes towards RF device interface losses and reduces the overall effective resistivity of the substrate [8]. The magnitude of the losses increases with increasing electric field [9]. Given the bias-dependent nature of the losses, passivating the HR-Si surface is essential to prevent the formation of parasitic charges. This is achieved by establishing a charge-trapping mechanism at silicon-insulator interface which traps the moving carriers in the substrate from accumulating at silicon surface [10].

Several passivation mechanisms have been proposed to address the issue, including proton implantation [11,12], deposition of trap-rich layers such as polycrystalline Si [13,14] and amorphous Si [15], deposition of porous Si [16] and integration of post-process porous Si [17], deposition of non-Si layer such as nitrated SiC, AlN and incorporation of buried P-N junction [18-22]. Except for [16] and [17] which involved porosification, all other mentioned techniques involved introduction of local passivation layers on silicon, which can potentially induce fabrication complexities and design challenges. An alternative approach focusing on bulk passivation technique was introduced, by employing a method known as deep-level doping compensation [23].

Deep-level doping compensation method was developed by introducing deep-level impurities into Czochralski-grown silicon (Cz-Si) to produce high-resistivity substrates [24]. It is achieved by compensating for background carrier concentration in silicon using co-doping techniques with deep acceptor and/or deep donors. Among all other deep-level dopants, gold was studied further due to its potential to become both deep acceptor and deep donor, offering flexibility in the compensation process [25,26]. Additionally, extensive research works have been published on gold in silicon to elucidate its behavior in silicon substrates [27-29]. The potential of gold-doped HR-Si as RF substrate was first evidenced by the enhancement of Cz-Si bulk resistivity from nominal value of 50 Ohm.cm to up to 100 kOhm.cm and improved performances of microwave devices [30,31]. Potential of PSC suppression was first reported through bias-independent CPW losses fabricated on the substrate [32,33]. However, based on the effective resistivity and harmonic distortion measurements, the substrate demonstrated bias-dependent and temperature-dependent non-linear behavior, suggesting insufficient traps to fully pin the Fermi level at the intrinsic level [34,35].

To gain a deeper understanding of the charge-trapping mechanism in gold-doped HR-Si, it is crucial to comprehend the two primary processes involved in its development; (1) the introduction of gold dopants through ion-implantation and (2) the activation of implanted gold in silicon through argon-annealing procedures [30]. The effects of varying the implantation processes have been discussed in previous works [30] however, there has been no reported works on the effects of other process variations such as the annealing procedures, gold surface-etching and oxidation processes on the resistivity and RF performances of devices fabricated on the substrates. This paper aims to highlight these effects and provides better insights into the behavior of gold-doped HR-Si and its potential as advanced RF substrates. In this work, the effects of activation

annealing procedures on the substrate resistivity are measured and compared, followed by the analysis on the MOS structures fabricated on the substrates in terms of their DC and RF characteristics.

2.0 METHODOLOGY

Six-inch <100> N-type Czochralski silicon wafers with resistivities 50 –60 Ohm.cm were used as the starting wafers. Gold atoms were first implanted through the backsides with implantation dose and energy of 4 x 10^{13} cm^{-2} and 100 keV, respectively. After implantation, the wafers were subjected to an Ar-annealing process for 1 hour at 950°C in the furnace. These parameters were optimized based on four-point-probe (FPP) and coplanar waveguide (CPW) attenuation measurements reported in [30]. This specific combination of implantation dose and annealing temperature yields the maximum enhancement in resistivity. Whilst maintaining similar annealing temperature, time and treatment gas, this work further optimizes the annealing conditions by adjusting the temperature gradient of the cooling process in the furnace after which the annealing process is completed. There are three different approaches considered in this work; (1) Rapid cooling, (2) Controlled and (3) Controlled + rapid cooling. Rapid cooling refers to almost-immediate cooling-down process after the annealing ends and before the wafer boat is taken out from the furnace. This approach has been utilized in all previous works related to the gold-doped HR-Si. The controlled cooling refers to steady cooling-down temperature gradient after the annealing ends and before the wafer boat is taken out from the furnace. The third approach refers to the combination of controlled and rapid cooling, by which the wafers need to undergo two stages of annealing. The first one with the controlled cooling, and the second one with the rapid cooling. The time separation between these two stages is 24 hours to ensure the wafers were sufficiently cooled down at room temperature before performing the second annealing stage.

Figure 1 further illustrates the process flow. In rapid cooling, the furnace temperature ramps up from 500^0C to annealing temperature of 950°C whereas in controlled cooling, the ramping-up starts at 200^0C before climbing to annealing temperature of 950°C. Regardless, both ramps up at the same rate of 10°C/min. Then, in both conditions, the annealing process is conducted for 1 hour at 950°C under argon atmosphere. After annealing completes, ramping-down temperature process in rapid cooling happens at much greater rate compared to the one in controlled cooling, i.e. 15°C/min for the former as compared to 5°C/min for the latter. Another unique point of the rapid cooling is that the unloading of the wafers happens at T = 850°C, after which the actual ramping down of the furnace temperature occurs at a rate of 85°C/min instead of the initial recipe of 15°C/min.

Following annealing, four-point prober were used to measure the resistivity of the wafers at five different locations on both the front and back surfaces of each wafer, ensuring comprehensive coverage of the entire surface area. Table 1 summarizes the average resistivity of the wafers developed under the three different approaches. In all three cases, the resistivity measured at the front side and the back side of the wafers give out almost similar values i.e. rapid cooling with values between 20-30 kOhm-cm, controlled cooling with values between 1-2 kOhm-cm and combined approach with values between 30 – 40 kOhm-cm. This result indicates that the kick-out mechanism is present in all cases [30], showing potentials of gold as deep level dopant in this compensation technique. In addition to that, it is prominently evident that all approaches provide resistivity enhancement to the silicon, from nominal values between 50-60 Ohm-cm to values above 1 kOhm-cm. However, the highest resistivity enhancement is shown by the gold-doped HR-Si wafers developed through the third annealing approach, combining both controlled cooling and rapid cooling, with values above 30 kOhm-cm. Significant enhancement is also seen in wafers developed through rapid cooling, with values above 20 kOhm-cm, reflecting the results reported in previous works. The least enhancement is shown by the wafers developed through controlled cooling approach, with values less than 3 kOhm-cm.

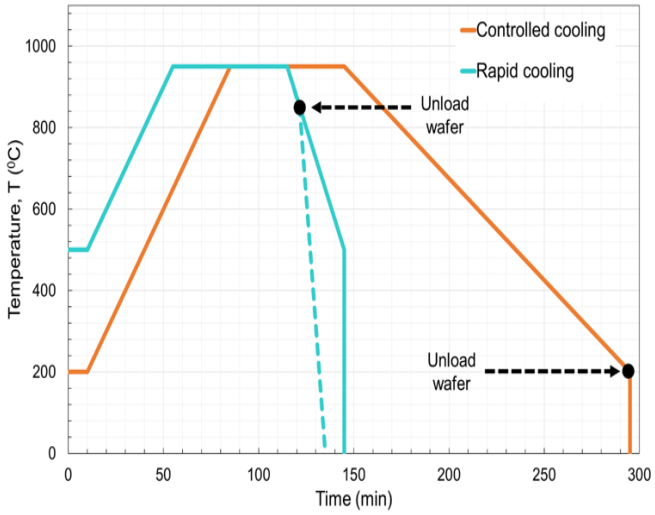


Figure 1 Ar-annealing process flow for three different approaches considered in this work. (1) controlled cooling (2) rapid cooling (3) controlled cooling + rapid cooling (24-hour cooling period between the first and second annealing process).

Table 1 FPP resistivity measurements

Cooling approach	Resistivity (kOhm-cm)		Average resistivity (kOhm-cm)	Kick-out Mechanism	Suitability for RF application
	Front	Back			
Rapid cooling	22.6	21.7	22.15	YES	YES
Controlled	1.54	2.00	1.77	YES	NO
Combined (Controlled + rapid cooling)	37.0	32.0	34.5	YES	YES

The differences in the resistivity enhancement values can be explained further through the behaviour of the gold atoms under different cooling condition. In all cases, gold diffuse into silicon as interstitial atoms at T = 600^{0}C [36]. As soon as the temperature hits 800^{0}C, the interstitial gold atoms kick out the silicon atoms to occupy the substitutional sites, causing the kicked-out silicon atoms to become self-interstitials [37]. The substitutional gold atoms then compensate for the shallow impurities and dopants that exist in silicon, resulting in an increase in the bulk resistivity of the silicon substrate. Above this temperature, the kick-out mechanism continues to occur, and more substitutional gold atoms are created with peak activity happening at 950°C. After this process, furnace temperature is brought down gradually from 950^{0}C to 200^{0}C before the wafers were unloaded, in the case of controlled cooling. This causes thermal donors to be generated, especially when the temperature falls below 500^0 C [38], reducing the resistivity of the silicon. Despite that, it does not reach its nominal value, indicating that substitutional gold atoms remain electrically active and able to compensate for the additional generation of impurities. In the case of rapid cooling approach, any non-ideal activities such as the generation of thermal donors are limited, due to two reasons; (1) rapid fall of furnace temperature after annealing and (2) unloading of the silicon wafers at T = 850^{0}C, a temperature at which the event is unlikely to occur. Hence, the resistivity enhancement is maintained. When the two approaches are combined, as in the third approach, controlled cooling enhances the activation of the substitutional gold atoms in the first annealing process. In the subsequent annealing phase, which employs rapid cooling, additional substitutional gold atoms are formed, supplementing those created during the first annealing process. Consequently, the resistivity of the silicon is further increased.

Although all approaches have successfully shown potential in resistivity enhancement, the gold doped silicon substrate developed through single controlled cooling approach is deemed as unsuitable to be used in RF application, since the average resistivity is less than 4 kOhm-cm. Additionally, given that the combined approach demonstrates higher resistivity values than the single rapid cooling method, the gold-doped silicon generated through the former will be utilized in the next phase of this study.

Parasitic surface conduction in the substrates were analysed using metal-oxide-silicon (MOS) structures. It involved design and fabrication of two types of device; capacitors and coplanar waveguides. The structures incorporated back metallization to enable back-biasing during DC and RF characterizations. Capacitance-voltage (CV) characterizations of the capacitor structures were employed to evaluate the charges associated with gold-doped high-resistivity silicon, whilst bias-dependent RF characterizations of the coplanar waveguides facilitated the observation of potential suppression of parasitic surface conduction.

Before device fabrication takes place, gold surface-etching process was conducted to eliminate any possible conductive layer resulting from residual gold left during the implantation on the silicon surface [30]. Observing the effects of gold surface-etching on RF device behavior was part of this work's objectives, hence having the non-etched substrate option was also considered. Then, a 20-nm silicon dioxide was deposited on the silicon surface to provide DC isolation in the fabricated devices. Two oxidation processes were considered. The first one was thermal oxide, grown using dry oxidation method in the furnace, another one is sputtered oxide, deposited through reactive sputtering method. The purpose is to determine the temperature sensitivity of the substrates, as the former is conducted in high-temperature environment (T>900^{0}C) whereas the latter is conducted in room temperature environment. Following oxide deposition, a 1-µm aluminum layer was evaporated onto silicon dioxide to form the front contact. Subsequently, photolithographic patterning of the MOS devices was performed, followed by the deposition of a 500-nm aluminum back contact using reactive sputtering.

3.0 RESULTS

C-V measurements were conducted under high frequency environment on all fabricated wafers. For each measurement, a DC voltage was applied, and the voltage was swept from -6V (inversion) to +6V (accumulation), with illumination provided to mitigate deep depletion effects. Figure 2 presents the C-V characteristics of gold-doped HR-Si. For comparison, C-V characteristics of Float-zone silicon (Fz-Si) (resistivity: ~360 Ohm.cm) were also included. Fz-Si exhibits typical high-frequency behavior characteristic of an N-type substrate, with maximum capacitance (C_{MAX}) observed in the positive bias region, indicating charge accumulation, and minimum capacitance (C_{MIN}) observed in the negative bias region, indicating surface inversion. The observed C_{MAX} is slightly lower than the oxide capacitance (C_{OX}, calculated to be 1.73 x 10^{-3} F/m²), which can be attributed to the Debye length exceeding the oxide thickness (t_{OX}). When the

Debye length is larger than t_{OX}, the free carrier response to the electric field occurs at a distance from the oxide-silicon interface, resulting in a reduced C_{MAX} in the accumulation region.

For gold-doped high-resistivity silicon (HR-Si) substrates, similar trends are observed in substrates with thermal oxides, where the C_{MAX} and C_{MIN} appear in the positive and negative bias regions, respectively. The reduced C_{MAX} compared to Fz-Si can be attributed to the higher resistivity of the HR-Si substrates, which corresponds to an increased Debye length. Furthermore, the gold-doped HR-Si substrates without etching exhibit higher capacitance values than their etched counterparts, likely due to the lower resistivity induced by the gold conductive layer present at the substrate surface. In contrast, substrates with sputtered oxides, etched and non-etched, did not display distinct high-frequency C-V characteristics, instead showing flat trends. The flat trend indicates that the substrate charges do not respond to DC voltages, hence the absence of accumulation, depletion and inversion behavior in the C-V graph. While similar observations are made for both non-etched and etched substrates, the capacitance values across all voltages are lower than those of gold-doped HR-Si with thermal oxides. These results are particularly interesting, given that the substrate resistivity is identical for both thermal and sputtered oxides, which would ordinarily lead to comparable C_{MAX} values for each etched and non-etched substrate.

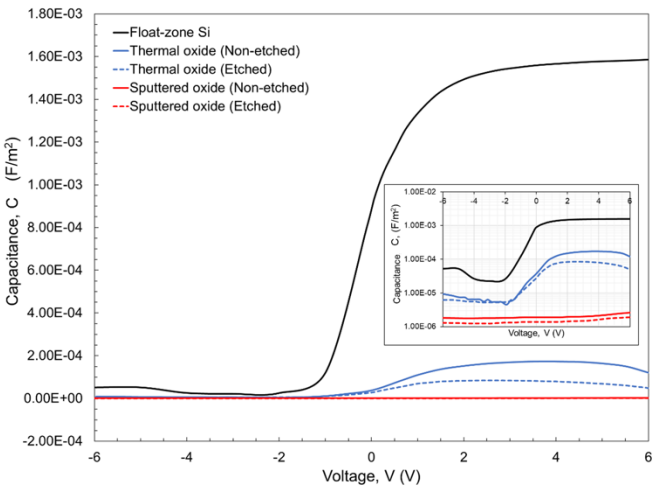


Figure 2 High-frequency C-V characteristics for gold-doped HR-Si. Inset graph illustrates the comparison in log scale

RF measurements were then conducted with the incorporation of constant DC voltage at the similar range mentioned in the C-V. CPW attenuation loss was calculated using the following expression [39]:

$$\alpha = -\frac{10}{l} log_{10}\left[\frac{|S_{21}|^2}{1-|S_{11}|^2}\right] \quad (1)$$

where l is the CPW length and α is measured in dB/mm. S_{11} and S_{21} refer to the return loss and the transmission loss of the CPW, respectively. Attenuation losses on all gold-doped HR-Si substrates increases gradually with frequency, which is expected due to conductor and dielectric losses (results not shown here) [40]. Figure 3 shows the loss comparison between substrates with thermal oxide and sputtered oxide. It can be seen that the losses for the thermal oxide exhibit a distinct variation with voltage. At negative voltages, the attenuation loss are relatively high (~0.45 dB/mm) and decreases as the voltage approaches 0V and towards the small positive voltages, reaching a minimum of around 0.25 dB/mm at +1V. Then, the loss increases again towards higher positive voltages, suggesting strong dependence of the attenuation loss on the applied voltage. The lowest attenuation region (between 0V to +3V) corresponds to the depletion of charges, whereas the higher losses at negative and positive voltage regions refer to surface inversion and accumulation of charges, respectively. On the contrary, the attenuation loss for the gold-doped HR-Si with sputtered oxide remains nearly constant (~0.2dB/mm) across the entire voltage range from -6V to +6V. This flat response indicates that the loss is largely independent of the applied voltage, suggesting suppression of charges at the oxide-silicon interface i.e. the absence of accumulation and inversion at the oxide-silicon interface.

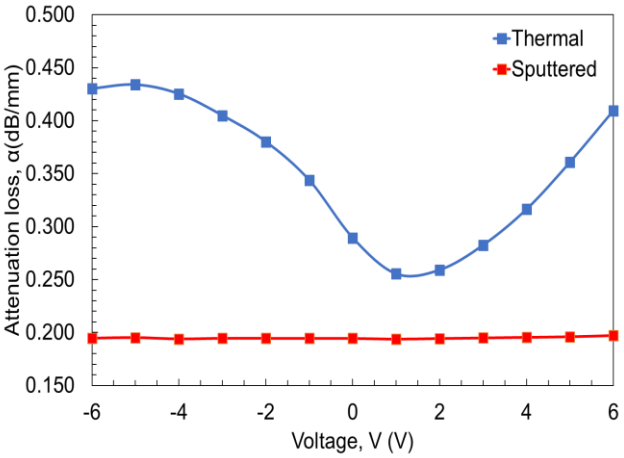


Figure 3 Effects of oxidation process on attenuation losses of gold-doped HR-Si

The effects of gold-etching on the CPW attenuation loss are illustrated in Figure 4 for the substrates with sputtered oxide. In both cases, the dependence on the applied voltage is seen towards more positive voltages, recording the highest loss at +6 V (accumulation region). However, this dependency is considered negligibly small i.e. less than 2% difference between highest loss and lowest loss for the measured range of voltages for each etched and non-etched substrate. It is also particularly interesting to note that the losses measured for etched substrates are higher than the non-etched substrates (almost by 5%), even

though the removal of the conductive gold surface layer has given superior resistivity value compared to the non-etched substrates. The presence of gold (in the case of non-etched substrates) on the silicon surface layer acts as additional traps at the oxide-silicon interface, suppressing the charge conduction, hence reducing the overall CPW attenuation loss. Apart from etching, the effects of light illumination were also included in the figure. Increase in losses are observed in both etched and non-etched cases, originated from the generation of additional carriers due to photon absorptions, more prominently in the accumulation region (positive region, in this case).

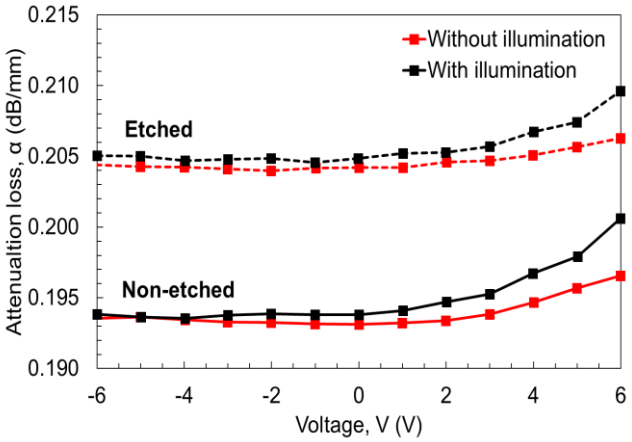


Figure 4 Effects of gold surface-etching and light illumination on attenuation losses of gold-doped HR-Si

Based on the results shown in Figures 3 and 4, it can be concluded that non-etched gold-doped HR-Si with sputtered oxide produce maximum suppression of parasitic surface conduction, indicated by the lowest loss and its weak dependency on the applied voltage. This particular substrate was then compared with its oxide-free counterpart. Figure 5 presents this comparison, alongside the losses measured on the 360-ohm.cm Fz-Si and Fz HR-Si substrates with resistivity ~ 10 kOhm.cm. For all substrates, the attenuation loss increases progressively with frequency, reflecting the inherent frequency-dependent losses as previously discussed. The losses on gold-doped HR-Si are significantly lower than Fz-Si and comparable to Fz HR-Si. The observation is attributed to the bulk resistivity values of the substrates. Fz-Si is of much lower resistivity compared to the other two substrates, and the Fz HR-Si resistivity is in the comparable range with the gold-doped HR-Si (kOhm.cm). However, the key observation of this graph is that the losses of the gold-doped HR-Si with oxide is comparable to the oxide-free gold-doped HR-Si, suggesting that the presence of the oxide layer does not significantly impact the attenuation loss on gold-doped HR-Si hence, promoting suppression of charges at the oxide-silicon interface.

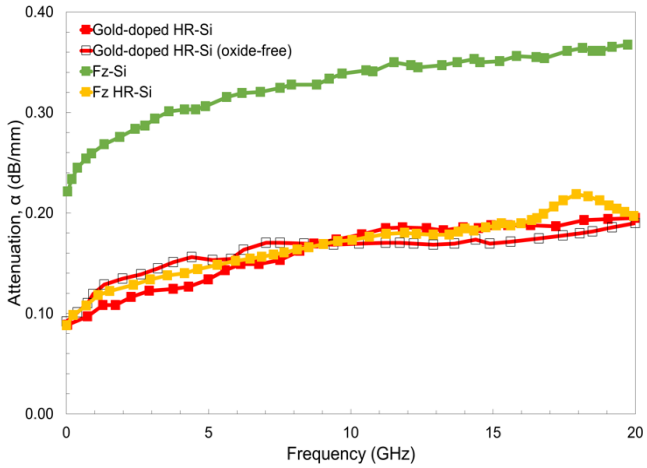


Figure 5 Substrate comparison on CPW attenuation losses

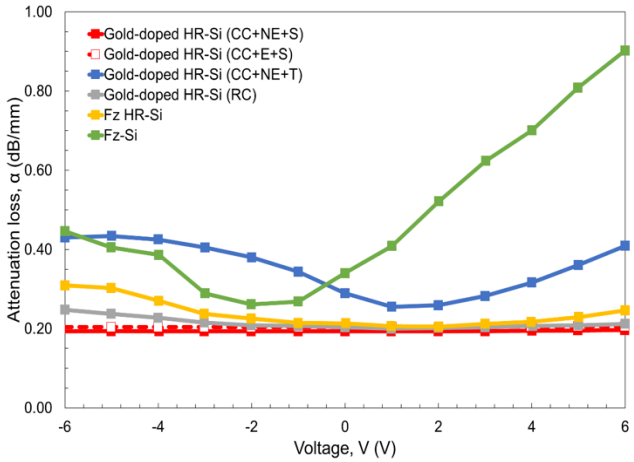


Figure 6 Bias-dependent losses on all substrates, including the controlled Fz-Si and Fz HR-Si. CC: Combined cooling (Controlled + rapid cooling); RC: Rapid cooling only; NE: Non-etched; E: Etched; T: Thermal oxide; S: Sputtered oxide

Figure 6 shows the comparison in bias-dependent CPW attenuation losses across all gold-doped HR-Si substrates discussed in this work so far, as well as the controlled Fz-Si and Fz HR-Si substrates. Additionally, the CPW attenuation loss of devices fabricated on non-etched gold-doped HR-Si developed through rapid-cooling with sputtered oxide is also analyzed to observe the effects of substrate annealing conditions on the losses and consequently, on the potential suppression of charges. The data clearly indicate that gold-doped HR-Si substrates with sputtered oxide (both non-etched and etched) exhibit the lowest losses compared to other substrates, with the least dependency on bias voltages. All other substrates illustrate higher losses with more significant bias voltage dependency.

4.0 DISCUSSION

To quantitatively measure the bias-dependency level of the substrates, a ratio of $\alpha_{max}/\alpha_{min}$ is used [18]. A ratio of 1 denotes bias-independent losses whilst any values higher than that portrays dependency of the CPW losses on the DC bias. Table 2 summarizes the results obtained for all substrates in this work. From the table, it is clear that the non-etched gold-doped HR-Si substrate with sputtered oxide exhibits the lowest loss and the least dependency on bias voltages with values of 0.193 dB/mm and 1.01, respectively. Its etched counterpart also promotes bias-independent nature with ratio 1.01 however, with a slightly higher loss of 0.204 dB/mm. In both cases, the presence of light increases the dependency to 1.04 and 1.02, respectively. Regardless, these ratios are still considerably low and almost close to 1. Strong dependency is shown in all other substrates, with the highest ratio shown by Fz-Si ($\alpha_{max}/\alpha_{min}$ = 3.45). This provides several indications: (1) Silicon substrates exhibit parasitic surface conduction, as illustrated by bias-dependent losses in Fz-Si, that hinder their potential in RF applications; (2) Bias-independent losses of CPWs on gold-doped HR-Si is not attributed to substrate resistivity since Float-zone HR-Si develops strong dependency of 1.51 despite being highly resistive; (3) the gold-doped HR-Si is sensitive to high temperature environment, as illustrated by the ratio of 1.68 obtained for gold-doped HR-Si with thermal oxide and (4) single-stage annealing does not provide sufficient suppression at the interface, shown by a dependency ratio of 1.24 for gold-doped HR-Si developed through rapid cooling procedure.

Table 2 $\alpha_{max}/\alpha_{min}$ ratio for CPWs on all gold-doped HR-Si and controlled substrates.

Substrate	Annealing	Au-etching	Oxide	Light?	*a_{meas} (dB/mm)	a_{max}/a_{min}
Au HR-Si	C+RC	YES	Sp	No	0.204	1.01
Au HR-Si	C+RC	NO	Sp	No	0.193	1.01
Au HR-Si	C+RC	YES	Sp	Yes	0.205	1.02
Au HR-Si	C+RC	NO	Sp	Yes	0.194	1.04
Au HR-Si	C+RC	NO	Th	No	0.289	1.68
Au HR-Si	RC	NO	Sp	No	0.203	1.24
Fz HR-Si	-	-	Sp	No	0.207	1.51
Fz-Si	-	-	Th	No	0.340	3.45

5.0 CONCLUSION

This study is aimed to investigate the effects of process variations on the development of gold-doped HR-Si substrates and their impacts on the DC and RF device performances working in the GHz-range. The findings demonstrate that double-stage annealing consists of controlled cooling and rapid-cooling procedures have effectively increased the bulk resistivity of the substrates, as compared to its single-stage counterparts. Additionally, high-temperature environment is found to be unsuitable for gold-doped HR-Si, reflected by the bias-dependent CPW losses, supporting the findings reported in [35]. Moreover, the removal of gold surface layer on the gold-doped HR-Si, which was found to be effective in increasing the resistivity of the substrate, is found to be unnecessary from the RF perspective as it actually provide higher losses. These results suggest that charge-trapping mechanism in gold-doped HR-Si is affected by a number of processes variations and can be optimized further to enhance its potential as advanced RF substrates. However, its implementation in large-scale manufacturing still poses several challenges especially in terms of its temperature sensitivity and potential risk of contaminations. Future research could focus on extending these findings to optimization of the charge-trapping mechanism in gold-doped HR-Si through its activation annealing procedures.

Acknowledgement

This work is supported by Ministry of Higher Education Malaysia for Fundamental Research Grant Scheme with Project Code: FRGS/1/2020/TK0/USM/02/6. A special thanks to C. H. (Kees) de Groot and Southampton Nanofabrication Centre, University of Southampton, United Kingdom for the fabrication facilities, technical support and helpful discussions.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

References

[1] International Roadmap for Devices and Systems (IRDS™) 2023 Edition -IEEE IRDS™. (n.d.). Retrieved from https://irds.ieee.org/editions/2023.

[2] Ali, K. B., Neve, C. R., Shim, Y., Rais-Zadeh, M., & Raskin, J. -p. 2014. Non-linear Characteristics of Passive Elements on Trap-rich High-resistivity SI Substrates. *2014 IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems*. In Press. https://doi.org/10.1109/sirf.2014.6828521.

[3] Allibert, F, Andia, L, Morandini, Y, Veytizou, C, Rack, M, Nyssens, L, *et al*. 2020. Engineering SOI Substrates for RF to mm-wave Front-ends. *Microwave Journal*. 72–82.

[4] Checchin, M., Frolov, D., Lunin, A., Grassellino, A., & Romanenko, A. 2022. Measurement of the Low-Temperature Loss Tangent of High-Resistivity Silicon using a High- Q Superconducting Resonator. *Physical Review Applied*. 18(3). https://doi.org/10.1103/physrevapplied.18.034013.

[5] Lu, H., Hou, B., Yang, L., Zhang, M., Deng, L., Wu, M., *et al*. 2022. High RF Performance GAN-on-SI HEMTs with

Passivation Implanted Termination. *IEEE Electron Device Letters*. 43(2): 188–191. https://doi.org/10.1109/led.2021.3135703.

[6] Ma, C., Yang, X., Shen, J., Liu, D., Cai, Z., Chen, Z., *et al*. 2022. Low RF Loss and Low Dislocation Density of GaN grown on High-resistivity Si Substrates. *Applied Physics Express*. 15(3): 031003. https://doi.org/10.35848/1882-0786/ac5260.

[7] Wu, N. Y., Gamble, S., Armstrong, B. M., Fusco, V. F., & Stewart, J. A. C. 1999. SiO/sub 2/ Interface Layer Effects on Microwave Loss of High-resistivity CPW Line. *IEEE Microwave and Guided Wave Letters*. 9(1): 10–12. https://doi.org/10.1109/75.752108.

[8] Lederer, D., & Raskin, J.-P. 2005. Effective Resistivity of Fully-processed SOI Substrates. *Solid-State Electronics*. 49(3): 491–496. https://doi.org/10.1016/j.sse.2004.12.003.

[9] Schollhorn, C., Zhao, N. W., Morschbach, M., & Kasper, E. 2003. Attenuation Mechanisms of Aluminum Millimeter-Wave Coplanar Waveguides on Silicon. *IEEE Transactions on Electron Devices*. 50(3): 740–746. https://doi.org/10.1109/ted.2003.810466.

[10] Jansman, A. B. M., Van Beek, J. T. M., Van Delden, M. H. W. M., Kemmeren, A. L. A. M., Dekker, A. D., & Widdershoven, F. P. 2004. Elimination of Accumulation Charge Effects for High-resistive Silicon Substrates. *ESSDERC '03. 33rd Conference on European Solid-State Device Research, 2003*. https://doi.org/10.1109/essderc.2003.1256799.

[11] Perrosé, M., Alba, P. A., Reboh, S., Lugo, J., Plantier, C., Cardinael, P., *et al*. 2024. Local Interface RF Passivation Layer Based on Helium Ion-Implantation in High-Resistivity Silicon Substrates. *2024 IEEE/MTT-S International Microwave Symposium - IMS 2024*. https://doi.org/10.1109/ims40175.2024.10600220.

[12] Popov, V. P., Tarkov, S. M., Tikhonenko, F. V., Antonov, V. A., Tyschenko, I. E., Simakin, S. G., & Rudenko, K. V. 2021. Thermally Robust High-Resistance Layers on Low-Resistance Silicon Synthesized by Molecular CO+ Ion Implantation. *Physica Status Solidi (A)*. 218(23). https://doi.org/10.1002/pssa.202100109.

[13] Philippe, J., Robillard, J.-F., Gloria, D., & Dubois, E. 2024. Improvement of Linearity in Trap-rich Substrates for Radio Frequency Applications: Which of Donor and Acceptor Trap is the Best? *Journal of Applied Physics*. 136(1). https://doi.org/10.1063/5.0205853.

[14] Ding, L., Raskin, J.-P., Lumbeeck, G., Schryvers, D., & Idrissi, H. 2020. TEM Investigation of the Role of the Polycrystalline-Silicon Film/Substrate Interface in High Quality Radio Frequency Silicon Substrates. *Materials Characterization*. 161: 110174. https://doi.org/10.1016/j.matchar.2020.110174.

[15] Yang, Y., Gao, L., & Gong, S. 2022. Surface-Acoustic-Wave Devices based on Lithium Niobate and Amorphous Silicon Thin Films on a Silicon Substrate. *IEEE Transactions on Microwave Theory and Techniques*. 70(11): 5185–5194. https://doi.org/10.1109/tmtt.2022.3194554.

[16] Rack, Martin, Belaroussi, Y., Ali, K. B., Scheen, G., Esfeh, B. K., & Raskin, J.-P. 2018. Small- and Large-Signal Performance up to 175°C of Low-Cost Porous Silicon Substrate for RF Applications. *IEEE Transactions on Electron Devices*. 65(5): 1887–1895. https://doi.org/10.1109/ted.2018.2818466.

[17] Scheen, G., Tuyaerts, R., Rack, M., Nyssens, L., Rasson, J., Nabet, M., & Raskin, J.-P. 2020. Post-process Porous Silicon for 5G Applications. *Solid-State Electronics*. 168: 107719. https://doi.org/10.1016/j.sse.2019.107719.

[18] Evseev, S. B., Nanver, L. K., Rejaei, B., & Milosavljević, S. 2014. Amorphous Silicon Carbide Nitride Layer as an Alternative to a Disordered Silicon Surface to Suppress RF/microwave Losses. *Microelectronic Engineering*. 125: 2–7. https://doi.org/10.1016/j.mee.2014.04.003.

[19] Bose, A., Biswas, D., Hishiki, S., Ouchi, S., Kitahara, K., Kawamura, K., & Wakejima, A. 2020. Elimination of the Low Resistivity of SI Substrates in GAN HEMTs by Introducing a SIC Intermediate and a Thick Nitride Layer. *IEEE Electron Device Letters*. 41(10): 1480–1483. https://doi.org/10.1109/led.2020.3019482.

[20] Wei, L., Yang, X., Shen, J., Liu, D., Cai, Z., Ma, C., *et al*. 2020. Al Diffusion at AlN/Si Interface and Its Suppression through Substrate Nitridation. *Applied Physics Letters*. 116(23). https://doi.org/10.1063/5.0006496.

[21] Lin, P., Liu, J., Lin, H., Chuang, Z., Hsu, W., Chen, Y., *et al*. 2023. Suppression of p-type Parasitic Channel Formation at the Interface between the Aluminum Nitride Nucleation Layer and the High-resistivity Silicon Substrate. *Surfaces and Interfaces*. 36: 102590. https://doi.org/10.1016/j.surfin.2022.102590.

[22] Moulin, M., Rack, M., Fache, T., Chalupa, Z., Plantier, C., Morand, Y., *et al*. 2022. High-resistivity Silicon-based Substrate using Buried PN Junctions Towards RFSOI Applications. *Solid-State Electronics*. 194: 108301. https://doi.org/10.1016/j.sse.2022.108301

[23] Mallik, K., Falster, R. J., & Wilshaw, P. R. 2003. Semi-insulating Silicon using Deep Level Impurity Doping: Problems and Potential. *Semiconductor Science and Technology*. 18(6): 517–524. https://doi.org/10.1088/0268-1242/18/6/321.

[24] Jordan, D. M., Haslam, R. H., Mallik, K., Falster, R. J., & Wilshaw, P. R. 2010. The Development of Semi-Insulating Silicon Substrates for Microwave Devices. *Journal of the Electrochemical Society*. 157(5): H540. https://doi.org/10.1149/1.3353822.

[25] Collins, C. B., Carlson, R. O., & Gallagher, C. J. 1957. Properties of Gold-Doped silicon. *Physical Review*. 105(4): 1168–1173. https://doi.org/10.1103/physrev.105.1168.

[26] Bemski, G. 1958. Recombination Properties of Gold in Silicon. *Physical Review*. 111(6): 1515–1518. https://doi.org/10.1103/physrev.111.1515.

[27] Yu, X.-Y., Li, C.-H., & Zhao, J.-H. 2017. Study on Optical and Electrical Properties of Gold-doped Silicon Fabricated by Femtosecond Laser. *Optical and Quantum Electronics*. 49(7). https://doi.org/10.1007/s11082-017-1084-6.

[28] Yu, N. C., Chu, K. I., & Li, H. J. 2023. Recombination Center Levels in Gold and Platinum Doped n-type Silicon for High-speed Thyristor. In *Proceedings of the 2023 2nd Asia Power and Electrical Technology Conference* (APET), IEEE. https://doi.org/10.1109/APET59977.2023.10488974.

[29] Utamuradova, S. B., Daliev, S. Kh., Khaitbaev, A., Khamdamov, J., Yuldoshev, U. M., & Paluanova, A. D. 2024. Influence of Gold on Structural Defects of Silicon. *East European Journal of Physics*. 2: 327–335. https://doi.org/10.26565/2312-4334-2024-2-38.

[30] Abuelgasim, A., Mallik, K., Ashburn, P., Jordan, D. M., Wilshaw, P. R., Falster, R. J., & De Groot, C. H. 2011. Reduced Microwave Attenuation in Coplanar Waveguides using Deep Level Impurity Compensated Czochralski-silicon Substrates. *Semiconductor Science and Technology*. 26(7): 072001. https://doi.org/10.1088/0268-1242/26/7/072001.

[31] Abuelgasim, A., Hashim, N. Z. I., Chong, H. M. C., Ashburn, P., & De Groot, C. H. 2014. Low loss 67-GHz Coplanar Waveguides and Spiral Inductors on 100 kOhm.cm Gold-doped High Resistivity CZ-Silicon. *2014 IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems*. https://doi.org/10.1109/sirf.2014.6828514.

[32] Hashim, N. Z. I., Abuelgasim, A., & De Groot, C. H. 2014. Suppression of Parasitic Surface Conduction in Au-compensated High Resistivity Silicon for 40-GHz RF-MMIC Application. *Asia-Pacific Microwave Conference*. 55–57.

[33] Hashim, N. Z. I., & De Groot, C. H. 2018. Gold-compensated High Resistivity Silicon as Low-loss Microwave Substrate. *2018 Australian Microwave Symposium (AMS)*. https://doi.org/10.1109/ausms.2018.8346970.

[34] Nabet, M., Rack, M., Hashim, N. Z. I., De Groot, C. H., & Raskin, J.-P. 2020. Behavior of Gold-doped Silicon Substrate under Small- and large-RF Signal. *Solid-State Electronics*. 168: 107718. https://doi.org/10.1016/j.sse.2019.107718.

[35] Courte, Q., Rack, M., Nabet, M., Cardinael, P., & Raskin, J. -p. 2022. High-Temperature Characterization of Multiple Silicon-Based Substrate for RF-IC Applications. *IEEE Journal of the Electron Devices Society*. 10: 620–626. https://doi.org/10.1109/jeds.2022.3188893.

[36] Bullis, W. M. 1966. Properties of Gold in Silicon. *Solid-State Electronics*. 9(2): 143–168. https://doi.org/10.1016/0038-1101(66)90085-2.
[37] Gösele, U., Morehead, F., Frank, W., & Seeger, A. 1981. Diffusion of Gold in Silicon: A New Model. *Applied Physics Letters*. 38(3): 157–159. https://doi.org/10.1063/1.92285.
[38] Gösele, U., & Tan, T. Y. 1982. Oxygen Diffusion and Thermal Donor Formation in Silicon. *Applied Physics a Solids and Surface*. 28(2): 79–92. https://doi.org/10.1007/bf00617135.
[39] Sarkar, D. 2005. *Physical and Chemical Methods in Soil Analysis*. New Age International.
[40] Leal-Romero, R., Zuniga-Juarez, J. E., Zaldivar-Huerta, I. E., Del Carmen Maya-Sanchez, M., Aceves-Mijares, M., & Reynoso-Hernandez, J. A. 2008. Fabrication and Characterization of Coplanar Waveguides on Silicon using a Combination of SIO and SRO. *IEEE Transactions on Components and Packaging Technologies*. 31(3): 678–682. https://doi.org/10.1109/tcapt.2008.922005.