Jurnal Teknologi

Full Paper

A SINGLE-SWITCH HIGH STEP-UP DC-DC CONVERTER WITH COUPLED INDUCTOR

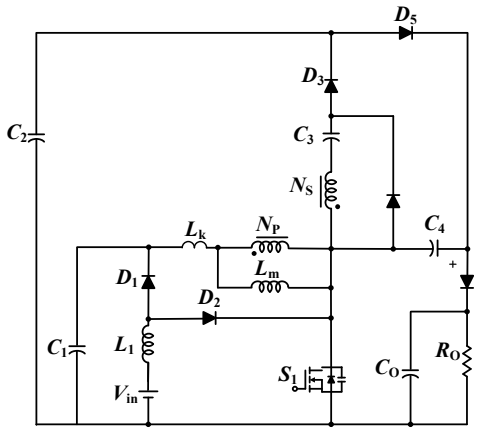
Thai Anh Au Tran, Kim-Anh Nguyen*, Xuan Khanh Ho, Duong Thach Pham

Faculty of Electrical Engineering, The University of Danang - University of Science and Technology, 54 Nguyen Luong Bang, Lien Chieu Ward, Danang 550000, Vietnam

Article history
Received
2 May 2025
Received in revised form
4 October 2025
Accepted
2 November 2025
Published Online
27 February 2026

*Corresponding author
nkanh@dut.udn.vn

Graphical abstract



Abstract

This paper presents a high step-up DC–DC converter employing a coupled inductor and a single switch. Conventional boost converters suffer from high switch voltage stress and efficiency loss due to leakage energy. A passive clamp circuit is introduced to recycle leakage energy and suppress voltage stress on the main switch, enhancing efficiency and reliability. The proposed topology is analysed in terms of operating modes, voltage gain, and voltage stress, and validated by both simulation and a 36 V/400 V, 300 W prototype. It achieves a voltage gain of 11.1 at a duty cycle of 0.42 and turns ratio of 2 under CCM, with efficiencies of 96.9% in simulation and 95.5% experimentally. Compared with existing designs, it attains higher voltage gain with fewer components and lower complexity. The converter is well suited for low-voltage renewable sources (12/24/48 V) and as a front-end stage for compact inverters in off-grid power supplies, UPS, microgrids, and mobile platforms.

Keywords: DC-DC converter, coupled inductor, high step-up, single switch, voltage gain, renewable energy

1.0 INTRODUCTION

As global energy demand continues to rise alongside environmental concerns, the shift towards renewable energy sources has become imperative for a cleaner and more sustainable future. Advances in clean energy technologies play a crucial role in effectively addressing these challenges. Increasing focus is being placed on renewable energy systems, including solar power, fuel cells, wind, and wave energy, to fulfill energy needs while mitigating environmental pollution [1, 2]. These technologies present viable solutions to

meet growing energy demands and sustainability objectives. Consequently, significant research and development efforts are being devoted to improving renewable energy systems to ensure a more efficient and environmentally friendly energy landscape [3, 4]. Among these renewable sources, photovoltaic (PV) and fuel cell (FC) technologies stand out as key contributors to providing clean, sustainable electricity [5]. Nevertheless, the voltage level is usually low [6].

To address the issue of low voltage, a conventional boost converter is applied [7]. According to theoretical analysis, the voltage level can increase indefinitely as the duty cycle approaches one. However, in practice, parasitic resistances cause significant voltage losses, leading to a reduction in conversion efficiency. In order to attain high voltage conversion while maintaining a low duty cycle, a double boost DC–DC converter structure is proposed to enhance conversion performance [8]. Although effective in high voltage conversion, this structure suffers from low efficiency due to proportional VS on the switch. The flyback converter can address the aforementioned issue by achieving high voltage using a coupled inductor (CI). However, another problem arises, energy leakage increases voltage spikes on the switch, affecting its lifespan [9].

CI have become essential in enhancing the performance of converters, offering significant advantages for practical use. A three-winding CI converter provides high VG with low switch stress, making it suitable for high-step applications, although it introduces design complexity due to the multiple windings, increasing the difficulty of implementation [10]. This paper presents a CI–based DC–DC converter that reduces VS on the switch, enhancing efficiency. However, this adds complexity to controlling the CI, making implementation more challenging [11]. Another design achieves high voltage conversion and reduces VS on semiconductors, yet managing the increased component count can raise system costs [12]. A CI structure with a variable coupling coefficient optimizes the efficiency at light loads, but requires advanced control strategies, increasing the design time and cost [13]. Switched-capacitor and switched-inductor techniques boost voltage in DC–DC converters. Switched-capacitor circuits reduce component size, while switched–inductor circuits provide higher voltage conversion [14, 15, 16]. However, these converters may suffer from higher switching losses and electromagnetic interference due to frequent operation of multiple components. Voltage lift is a method in DC–DC converters that boosts the output voltage by adding extra capacitive stages or windings, increasing VG without needing a higher duty cycle [17, 18, 19, 20]. However, high step–up converters using this technique and CI add complexity, additional components, switching losses, and stability issues. The voltage multiplier technique is used in DC–DC converters to increase the output voltage by multiplying the input voltage through multiple stages of capacitors and inductors [21, 22]. However, these converters suffer from increased complexity, potential voltage ripple, and reduced efficiency due to non-ideal components like capacitors and diodes.

In some applications, the VG may still be insufficient. Quadratic boost converters achieve high VG through the use of CI, providing benefits such as low VS, energy recovery, and reduced voltage spikes on the MOSFET during switching [23, 24, 25]. Building on these advantages, a new topology is proposed, integrating a boost stage with a CI into the quadratic boost converter for high VG. The input inductor ensures continuous current with low ripple, improving efficiency, while a passive clamp reduces switch voltage spikes, lowering conduction losses. This design not only enhances the performance of quadratic converters but also improves efficiency and reduces complexity, making it more suitable for applications such as renewable energy systems. The proposed high step-up DC–DC converter is well suited for small-scale photovoltaic (PV) systems with a few modules, fuel cells with outputs typically below 50 Vdc, and low-voltage energy storage systems (12/24/48 Vdc) [26, 27]. It can also serve as the front–end stage of low–power commercial inverters, boosting the low–voltage source to a standard DC-link level (300–400 Vdc) that feeds a DC–AC stage for 230 Vac output [28]. This makes it suitable for residential off–grid inverters, UPS and telecom backup, microgrids, data centers, specialized high-voltage loads, and mobile or electric platforms [29]. Such applications are already supported by commercial products from vendors such as Victron, Morningstar, Samlex, Mean Well, and Cotek. Therefore, the proposed topology offers both academic interest and strong practical potential for distributed energy systems and compact backup-power solutions.

2.0 METHODOLOGY

2.1 Operating Principles

As shown in Figure 1, the proposed converter (PC) employs a single MOSFET (S_1), six diodes (D_1–D_5 and D_o), five capacitors (C_1– C_4 and C_O), an input inductor (L_1) for current smoothing, and a coupled inductor (CI), to achieve an extremely high voltage gain.

To achieve an extremely high voltage conversion ratio, this work employs the CI by combining the effective turn-ratio boost with a multi-stage voltage-boosting network. This network integrates the three boosting stages into a single topology:

- First stage (boost converter): Formed by V_{in}, L_1, S_1, D_1, D_2, and the output capacitor C_1. It not only generates a higher voltage V_{C1} but also filters the input current.
- Second stage (intermediate voltage multiplier): Composed of input capacitor C_1, L_m, the two windings of the coupled inductor, capacitor C_3, and S_1, with output at C_2. In this stage, the turns ratio of the coupled inductor effectively boosts

the voltage, producing a high voltage across C_2. At this stage, capacitor C_2 also transfers energy to C_4 through D_5 (at the same voltage level).

- Third stage (output voltage multiplier): Capacitor C_1, L_m, and capacitor C_4 jointly deliver energy to the load.

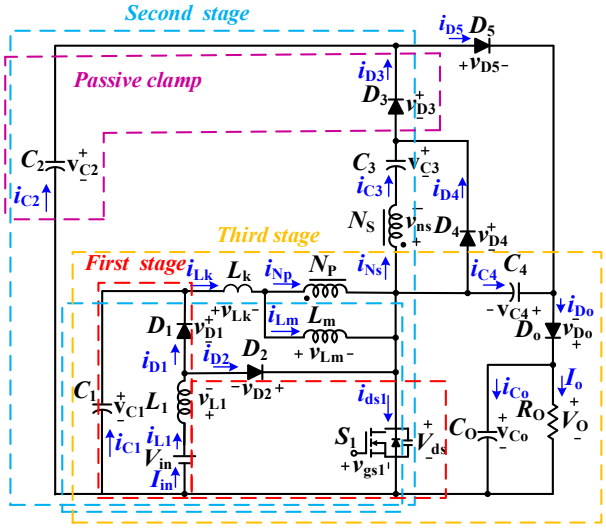


Figure 1 The proposed high step-up DC-DC converter

In addition to contributing to the voltage boosting process, D_3 and C_2 also form a passive clamping circuit that enables the recycling of the leakage inductance energy L_k. This mechanism suppresses voltage spikes across switch S_1, allowing the use of a device with a lower $R_{ds(on)}$, thereby improving the overall efficiency of the converter. This dual function also reduces the number of required components, resulting in a more compact and cost-effective design.

To simplify the analysis, the circuit is assumed to operate under the following conditions:

- All diodes and the switch are ideally;
- The capacitors C_1~C_4 and C_0 are sufficiently sized to maintain a constant voltage throughout one switching period;
- The CI is modeled with magnetizing inductance L_m and leakage inductance L_k on the primary side, with a winding ratio of $N_p{:}N_s = 1{:}n$.

The five operational states of the proposed converter are analyzed in detail with reference to the switching timing waveforms as illustrated in Figure 2. These operational states are depicted in Figures 3(a), 3(b), 3(c), 3(d), and 3(e), respectively.

State I $(t_0 - t_1)$, illustrated in Figure 3(a), can be described as follows: With v_{gs} high, S_1 is ON, D_1 and D_3 are OFF, and D_2, D_4, and D_5 conduct. Because $i_{Lk} > i_{Lm}$, the net current i_{Np} is positive, and the CI is coupled with both i_{Lk} and i_{Lm} increasing. During this phase, V_{in} energizes L_1 (the first stage–boost converter), while C_1 discharges into L_k, L_m, and C_3 through the CI (the second stage–intermediate voltage multiplier)). Meanwhile, C_4 is charged by C_2, and C_0 powers the load. This state stops when C_4 is fully charged and i_{D5} reaches zero at t_1.

State II $(t_1 - t_2)$, presented in Figure 3(b): With v_{gs} high, D_2 and D_4 conduct, while other diodes are OFF. V_{in} energizes L_1, C_1 discharges into L_k, L_m, and C_3, while C_0 powers the load. This state stops when v_{gs} goes low at t_2.

State III $(t_2 - t_3)$, shown in Figure 3(c): WIth v_{gs} low, D_2, D_3, and D_5 are OFF, while the others conduct. Since $i_{Lk} > i_{Lm}$, i_{Lm} increases, and i_{Lk} decreases, causing $i_{D4} = (i_{Lk} - i_{Lm})/n$ decreasing. V_{in} and L_1 charge C_1 and, along with L_m, L_k, and C_4, supply energy to C_o and the load. This state stops when i_{D4} reaches zero at t_3.

State IV $(t_3 - t_4)$, depicted in Figure 3(d): With v_{gs} low, D_2, D_4, and D_5 are OFF, while others conduct. Since $i_{Lk} < i_{Lm}$, i_{Np} is negative, causing current to flow through D_3 to C_2. V_{in} and L_1 charge C_1 (the first stage–boost converter). C_1 and L_m along with C_3, charge C_2 (the second stage–intermediate voltage multiplier). Meanwhile, V_{in}, L_1, L_m, and C_4 supply energy to C_0 and the load (the third stage–output voltage multiplier). The passive clamp formed by D_3 and C_2 recycles the leakage energy stored in L_k, redirecting it to charge C_2 (which subsequently supplies C_4 and the load). This energy recovery suppresses voltage spikes, improves efficiency, and reduces device stress. This state stops when C_4 fully discharges and i_{D0} is zero at t_4.

State V $(t_4 - t_5)$, presented in Figure 3(e): With v_{gs} low, D_2, D_4, D_5, and D_0 are OFF, while $D_1$and D_3 conduct. V_{in} and L_1 charge C_1 and supply energy to the CI. They also work with C_3 and L_k to charge C_2 through D_3. Meanwhile, C_0 powers the load. This state stops when v_{gs} goes high at t_5.

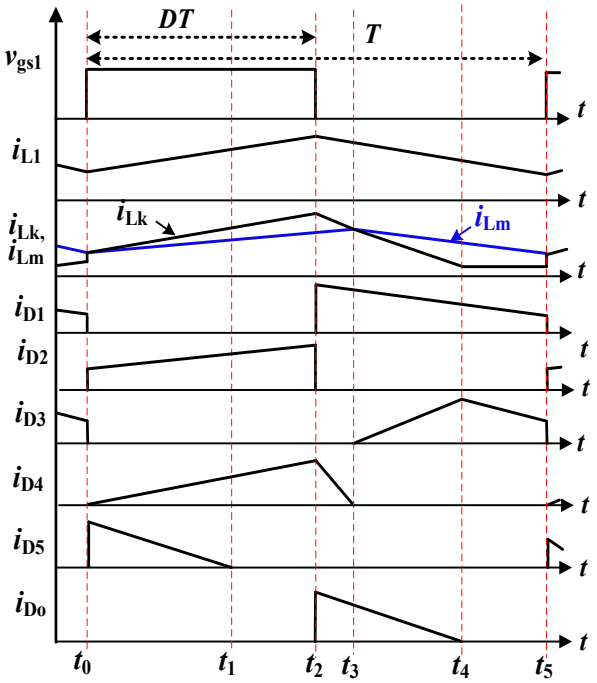
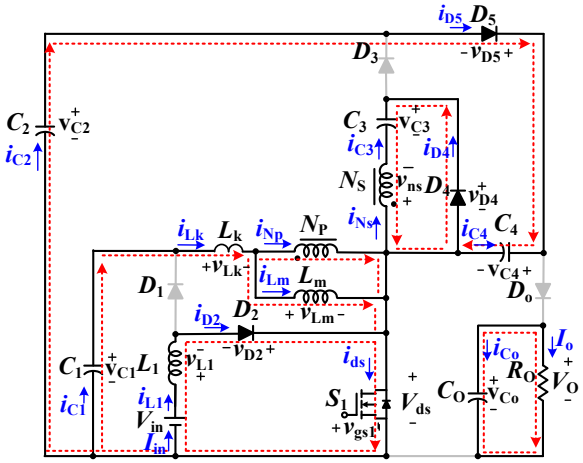
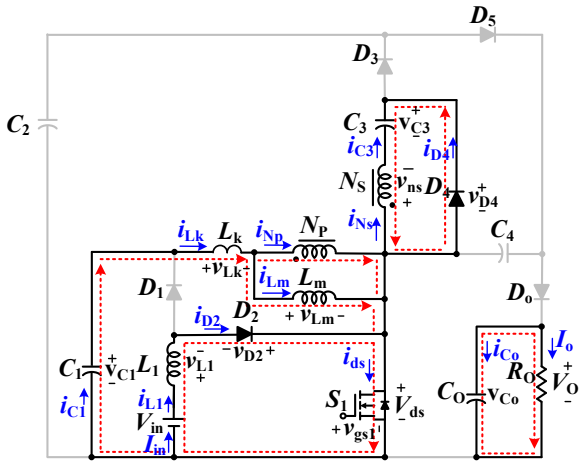
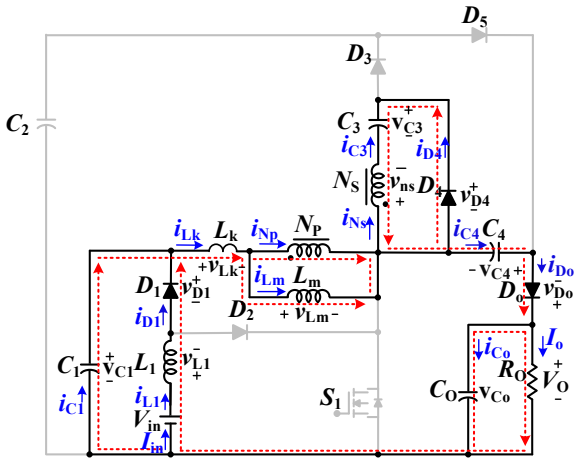
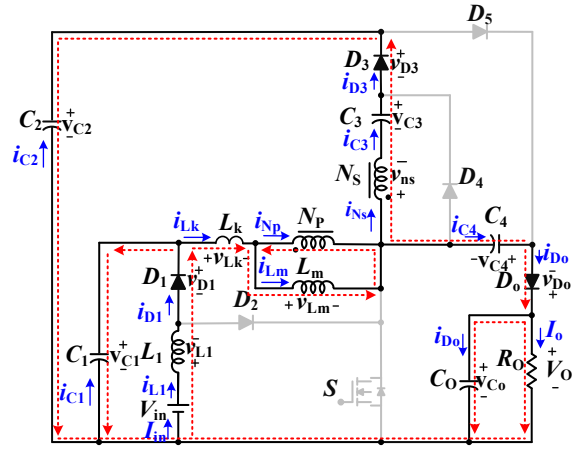


Figure 2 The waveforms of the proposed converter









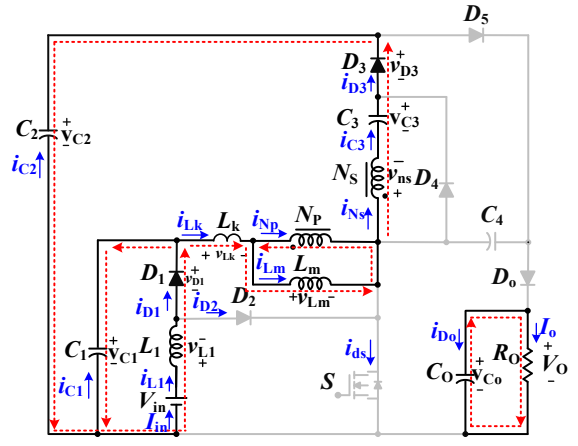


Figure 3 The operating states of proposed circuit: (a) State I, (b) State II, (c) State III, (d) State IV, and (e) State V

2.2 Analysis of the Proposed Converter in Steady-State Operation

The analysis is based on the mentioned states. To simplify the calculation process, we ignore the losses of the CI.

2.2.1 Voltage Gain Analysis

When Kirchhoff's II Law is applied, the following equations are obtained:

$$v_{L1} = V_{in}. \quad (1)$$

$$v_{Lm} = V_{C1}. \quad (2)$$

$$V_{C3} = v_{ns} = nv_{Lm} = nV_{C1}. \quad (3)$$

$$V_{C4} = V_{C2}. \quad (4)$$

The formulars can be obtained base on DT~T period:

$$v_{L1} = V_{in} - V_{C1}. \quad (5)$$

$$V_o = V_{in} - v_{L1} - v_{Lm} + V_{C4}. \quad (6)$$

$$V_{in} - v_{L1} - v_{Lm} - v_{ns} + V_{C3} - V_{C2} = 0. \quad (7)$$

Replacing $v_{ns} = nv_{Lm}$, we get

$$V_{in} - v_{L1} - (1+n)v_{Lm} + V_{C3} - V_{C2} = 0. \quad (8)$$

Substituting v_{L1} from (5) into (8),

$$V_{in} - (V_{in} - V_{C1}) - (1+n)v_{Lm} + V_{C3} - V_{C2} = 0. \quad (9)$$

which simplifies to

$$V_{C1} - (1+n)v_{Lm} + V_{C3} - V_{C2} = 0. \quad (10)$$

Therefore, the magnetizing-inductor voltage is

$$v_{Lm} = \frac{V_{C1}+V_{C3}-V_{C2}}{1+n}. \quad (11)$$

Applying the volt-second balance to the input inductor L_1:

$$\int_0^{DT} V_{in}\, dt + \int_{DT}^{T} (V_{in} - V_{C1})\, dt = 0. \quad (12)$$

Applying the same principle to the magnetizing inductor L_m:

$$\int_0^{DT} V_{C1}\, dt + \int_{DT}^{T} \frac{V_{C1}+V_{C3}-V_{C2}}{1+n} dt = 0. \quad (13)$$

Solving (12) and (13) gives the voltages across C_1 and C_2:

$$V_{C1} = \frac{1}{1-D} V_{in}. \quad (14)$$

$$V_{C2} = \frac{1+nD}{1-D} V_{C1} + V_{C3}. \quad (15)$$

From (3) and (14), the voltage across C_3 is:

$$V_{C3} = \frac{n}{1-D} V_{in}. \quad (16)$$

Finally, substituting (14) and (16) into (15) and (4) yields:

$$V_{C4} = V_{C2} = \frac{1+n}{(1-D)^2} V_{in}. \quad (17)$$

From (6) and (5), the output voltage can be expressed as

$$V_o = V_{in} - (V_{in} - V_{C1}) - v_{Lm} + V_{C4}. \quad (18)$$

which simplifies to

$$V_o = V_{C1} - v_{Lm} + V_{C4}. \quad (19)$$

Using (11) for v_{Lm}, together with (14) for V_{C1} and (17) for V_{C4}, we obtain

$$V_o = \frac{1}{1-D} V_{in} - \frac{V_{C1}+V_{C3}-V_{C2}}{1+n} + \frac{1+n}{(1-D)^2} V_{in}. \quad (20)$$

Substituting (14) for V_{C1}, (16) for V_{C3}, and (17) for V_{C2}, and simplifying gives

$$V_o = \frac{2+n}{(1-D)^2} V_{in}. \quad (21)$$

Therefore, the VG of the PC is

$$M = \frac{V_o}{V_{in}} = \frac{2+n}{(1-D)^2}. \quad (22)$$

2.2.2 Voltage Stress Analysis

The VS on the switch as:

$$V_{ds} = V_{Co} - V_{C4} = \frac{1}{(1-D)^2} V_{in}. \quad (23)$$

VS of $D_{1\sim5}$ and D_o is achieved as:

$$\begin{cases} V_{D1} = \frac{V_{in}}{1-D} \\ V_{D2} = \frac{DV_{in}}{(1-D)^2} \\ V_{D3} = \frac{(1+n)V_{in}}{(1-D)^2} \end{cases} \text{ and } \begin{cases} V_{D4} = \frac{nV_{in}}{(1-D)^2} \\ V_{D5} = \frac{V_{in}}{(1-D)^2} \\ V_{Do} = \frac{V_{in}}{(1-D)^2} \end{cases} \quad (24)$$

2.2.3 Converter Design Considerations

Based on the aforementioned equations and from the schematic representation in Figure 1, according Kirchhoff's current Law (KCL), the equation is derived as follows:

$$\frac{1}{T}\int_0^T i_{Do}\, dt = \frac{1}{T}\int_0^T (i_{C0} + I_O)\, dt = I_O. \quad (25)$$

$$\frac{1}{T}\int_0^T i_{D3}\, dt = \frac{1}{T}\int_0^T i_{Do}\, dt = I_O. \quad (26)$$

During DT ~ T, according to the KCL, the equation is written as:

$$\frac{1}{T}\int_{DT}^T i_{Lm} dt = \frac{1}{T}\int_{DT}^T (1+n)\, i_{D3} dt + \frac{1}{T}\int_{DT}^T i_{Do}\, dt. \quad (27)$$

From Equations (25), (26), and (27), i_{Lm_ave} is deduced as:

$$i_{Lm\_ave} = \frac{(2+n)I_O}{1-D} \quad (28)$$

The variation in current across L_m:

$$\Delta i_{Lm} = \int_0^{DT} i_{Lm}\, dt = \int_0^{DT} \frac{V_{Lm}}{L_m} dt = \frac{V_{Lm}}{L_m} DT. \quad (29)$$

Replace Equations (2), (14) into Equation (29):

$$\Delta i_{Lm} = \frac{V_{in} DT}{(1-D)L_m} \quad (30)$$

At boundary condition mode (BCM):

$$\frac{\Delta i_{Lm}}{2} = i_{Lm\_ave}. \quad (31)$$

To ensure continuous conduction mode (CCM), the ripple current of L_m must be small enough so that half of it remains below the average current. This condition is expressed as:

$$\frac{\Delta i_{Lm}}{2} < i_{Lm\_ave}. \quad (32)$$

Based on Equations (28), (30), and (32), the value of L_m is calculated using the formula:

$$L_m = \frac{V_{in} DT}{2(2+n)I_o} = \frac{V_{in} V_o DT}{2(2+n)P_o}. \quad (33)$$

In fact, with 40% of the selected load, the inductor is designed according to the following equation:

$$L_m = \frac{V_{in} V_o DT}{2(2+n)0.4P_o} \quad (34)$$

The change in inductor L_1 current during the time interval 0 ~ DT is given by:

$$\Delta i_{L1} = \frac{1}{T}\int_0^{DT} i_{L1}\, \delta\tau = \frac{V_{L1}}{L_1} DT. \quad (35)$$

The average current on inductor L_1:

$$i_{L1\_ave} = \frac{\Delta i_{L1}}{2}. \quad (36)$$

The design of inductor L_1 is based on Equations (35) and (36), with a 40% load:

$$L_{\mathrm{L1\_design}} = \frac{V_{\mathrm{in}}}{2I_{\mathrm{in}}0.4}DT = \frac{V_{\mathrm{in}}^2}{0.8P_0}DT \quad (37)$$

The capacitor design is based on factors such as the voltage ripple, switching frequency, and energy charging time, ensuring enough capacitance to maintain voltage stability during the conversion process.

$$C_0 = \frac{(1-D)V_{\mathrm{O}}}{f_{\mathrm{s}}R_0\Delta V_0}. \quad (38)$$

$$C_1 = \frac{(1-D)I_{\mathrm{in}}}{f_{\mathrm{s}}\Delta V_{\mathrm{C1}}} = \frac{(1-D)P_0}{f_{\mathrm{s}}V_{\mathrm{in}}\Delta V_{\mathrm{C1}}}. \quad (39)$$

$$C_{2,3,4} = \frac{DI_{\mathrm{C2,3,4}}}{f_{\mathrm{s}}\Delta V_{\mathrm{C2,3,4}}} = \frac{D^2V_{\mathrm{in}}}{nf_{\mathrm{s}}^2(1-D)\Delta V_{\mathrm{C2,3,4}}}. \quad (40)$$

3.0 RESULTS AND DISCUSSION

3.1 Simulation Results

The simulations, executed utilizing the SIMPLIS software, are predicated on the calculation formulas delineated in Section 2, with the simulation parameters detailed in Table 1.

Figure 4 illustrates the relationship between voltage gain and duty cycle with *n* from 1.5 to 3. The voltage factor M represents the target voltage gain when Vin = 36 V and Vo = 400 V at *n* = 2. Under these conditions, the duty cycle falls within the range of 0.4 to 0.6, allowing the converter to achieve the required VG while maintaining optimal efficiency.

Table 1 Simulation Parameters for The Proposed Topology

Parameter	Value
V_{in}	36 V
V_{O}	400 V
D	0.42
N_{p}: N_{s}	1: 2
f_{s}	50 KHz
R_0	533 Ω
P_0	300 W
L_{m}	125 µH
L_1	44 µH
C_0	550 µF
$C_{1,2,3,4}$	47 µF

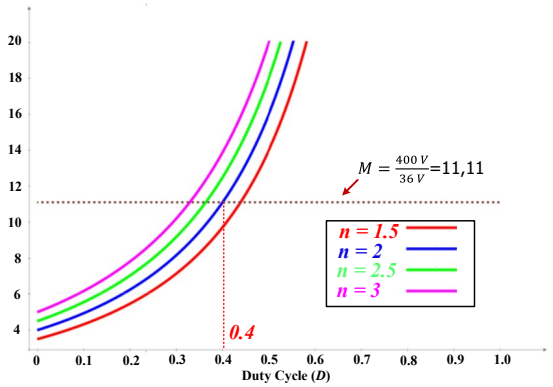


Figure 4 Voltage gain $M = \frac{V_{\mathrm{o}}}{V_{\mathrm{in}}}$ versus duty cycle D for turns ratios n=1.5, 2, 2.5, 3.

Figure 5 shows the simulation model of the proposed converter topology developed using Simplis/Simmetrix software. This simulation setup is used to validate the theoretical analysis and to observe the performance under various operating conditions.

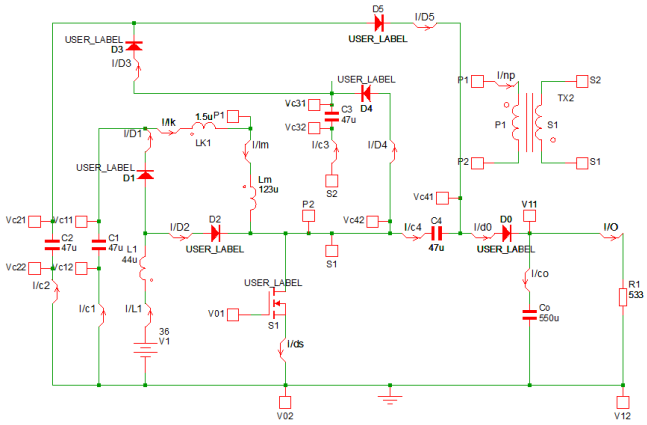


Figure 5 Simulation of the proposed converter topology

The simulated waveforms of the proposed converter are shown in Figure 6 over a 500 µs window.

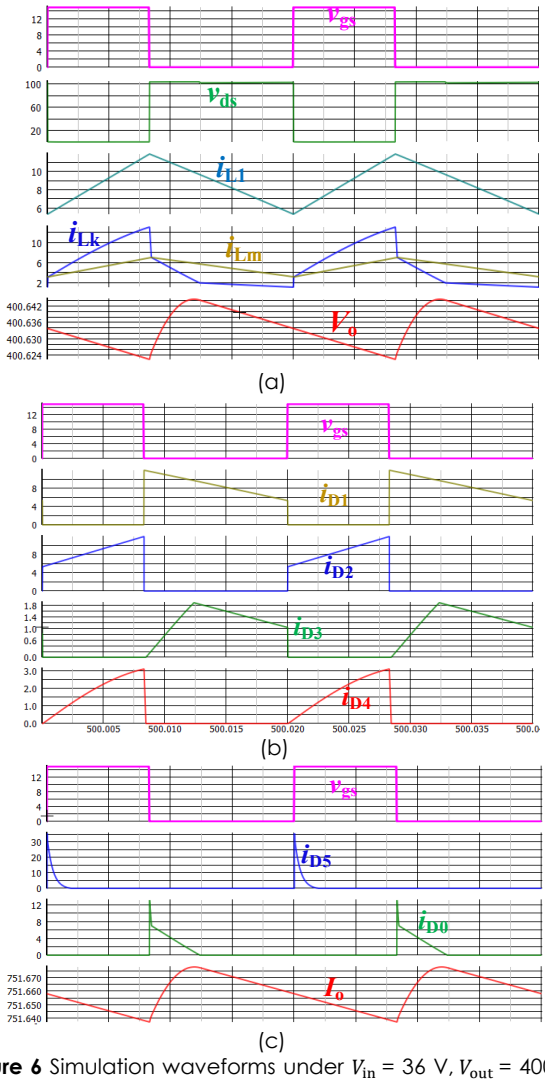


Figure 6 Simulation waveforms under V_{in} = 36 V, V_{out} = 400 V, and P_{o} = 300 W; (a) v_{gs}, v_{ds}, i_{L1}, i_{Lk}, i_{Lm}, and V_{O}; (b) v_{gs} and $i_{\mathrm{D1\sim D4}}$; (c) v_{gs}, i_{D5}, i_{D0}, and I_0

The plots include the gate signal v_{GS}, v_{DS}, input current i_{L1}, leakage and magnetizing inductor currents i_{LK} and i_{Lm}, diode currents i_{D1}–i_{D5}, and output voltage V_O. The gate signal v_{GS} (magenta) toggles between 0 V and 12 V with a ~20 µs period (50 kHz switching frequency) and a duty cycle close to 50%, ensuring consistent control of the power switch. The VS (yellow) peaks when the switch is off and drops during conduction, indicating that the switch operates under a relatively low VS, which supports reliability and efficiency.

The input inductor current i_{L1} (blue) exhibits a triangular waveform that never reaches zero, confirming operation in CCM, where the inductor current is continuously flowing throughout the switching cycle. This mode minimizes peak currents, reduces switching losses, and improves efficiency—key advantages in high-gain designs. The leakage i_{LK} (green) and magnetizing i_{Lm} (cyan) currents of the CI also remain above zero, reinforcing that all magnetic components operate in CCM. i_{LK} reaches up to ~1.5 A with sharp transitions during energy transfer, while i_{Lm} maintains a smoother profile, peaking at ~0.5 A. Their waveforms illustrate efficient energy handling and transfer through a magnetic coupling mechanism. The diode currents i_{D1}–i_{D5} show pulsed behavior with peak values between 0.5 A and 1.5 A. i_{D1} and i_{D2} alternate complementarily, and i_{D3} and i_{D4} conduct during distinct intervals, reflecting a well-timed, multi-phase boosting process.

The output voltage V_O (red) remains stable at approximately 400 V with minimal ripple (less than 1 V), demonstrating effective voltage regulation and good filtering performance. In summary, these results confirm that the converter operates stably in Continuous Conduction Mode, providing efficient energy transfer, reduced stress on components, and excellent voltage regulation–qualities that make it ideal for high step–up applications such as PV systems, fuel cells, or battery–powered equipment.

3.2 Experimental Results

To verify the theoretical analysis, a hardware prototype with the specifications listed in Table 1 was implemented in Figure 7, and the result waveforms are shown in Figure 8.

Figures 8(a)–8(f) provide time-domain confirmation of the steady-state voltages and currents reported in the previous table. Figure 8(a) shows the measured voltage across the MOSFET V_{ds}, where the peak level is effectively limited to around the expected theoretical stress rather than rising to the full output voltage. This demonstrates the proper operation of the passive clamp network, which recycles the leakage energy of the coupled inductor and prevents excessive overshoot on the switch. Only minor high–frequency spikes appear at each turn-off transition, attributable to residual stray inductance and probe coupling; their short duration confirms that the clamp circuit effectively suppresses the main surge and allows the use of a lower-rated, lower-$R_{DS(on)}$ device.

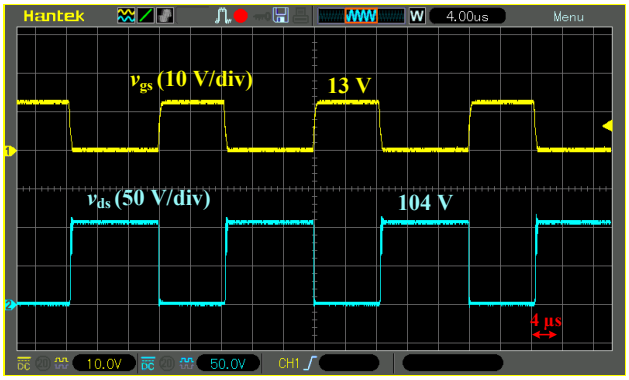
Figure 8(b) displays the voltage across diode D_1, which peaks near 61 V with only a small overshoot at turn–off; the slight excess above the ideal steady–state value is linked to the diode's forward drop and transient switching characteristics. Figure 8(b) also shows the waveform of D_2, peaking at about 43 V and exhibiting a bit more pronounced ringing, again due to reverse-recovery and stray–inductance effects.

Figure 8(c) illustrates the stresses on the high-voltage diodes D_3 and D_4 , reaching apprpximately 304 V and 200 V respectively; both waveforms have a flat plateau between switching intervals, confirming the correct charge–transfer function of these branches. The traces for D_5 and the output diode D_o, shown in Figure 8(d), peak at approximately 104 V and closely overlap in both timing and amplitude, demonstrating symmetrical operation of the output rectification stage.

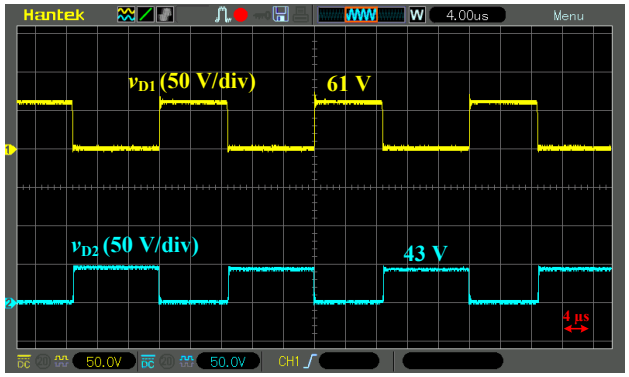
In addition to the voltage waveforms, Figure 8(e) also includes the input current and the leakage current of the coupled inductor. The input current follows the expected average level and ripple pattern corresponding to the designed duty cycle and power transfer. The leakage–current waveform displays the characteristic spike–like pulses during switching transitions, confirming the recycling of leakage energy by the clamp network and illustrating why the measured V_{ds} remains well below the uncontrolled spike levels that would appear in an unclamped topology. The output voltage trace in the same figure remains tightly regulated at approximetely 400 V, indicating that the converter maintains a stable operation under the tested load.

Overall, the oscilloscope captures in Figures 8(a)–8(f) visually substantiates the analytical predictions and highlight the clamp circuit's key role in protecting the main switch and improving efficiency. The small deviations between measured and theoretical steady–state values are explained by practical non–idealities such as diode recovery, parasitic inductance, PCB layout, and probe effects.

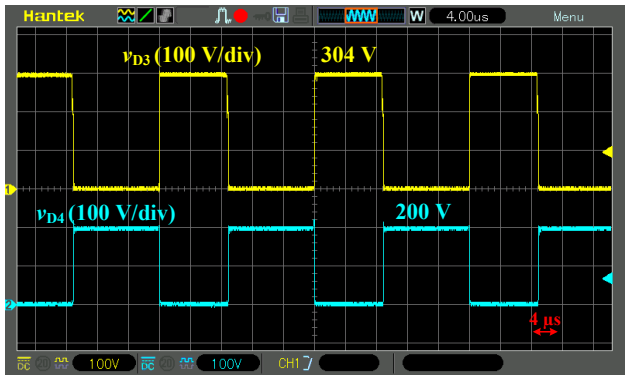
Figure 7 The hardware prototype and experimental setup



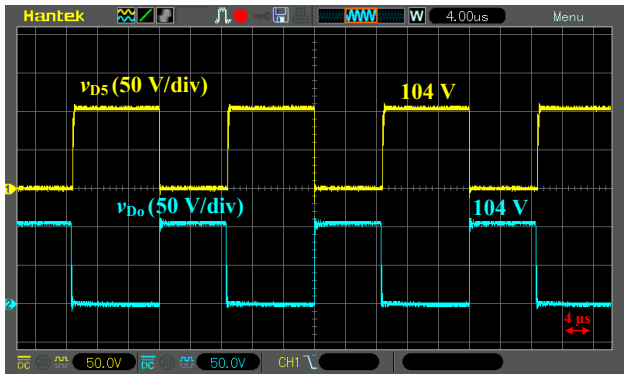
(a) V_{gs} and V_{ds}



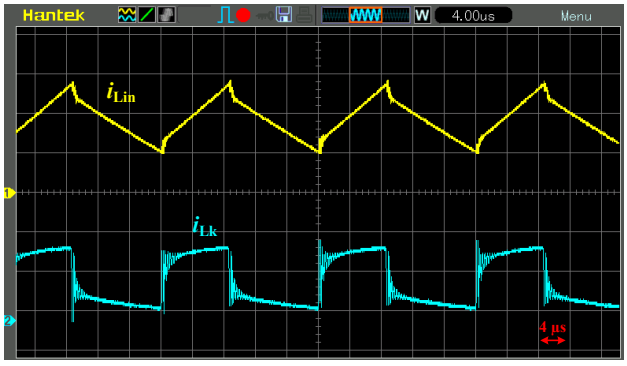
(b) V_{D1} and V_{D2}



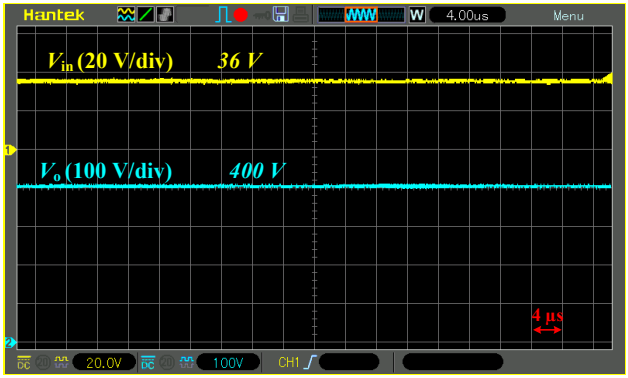
(c) V_{D3} and V_{D4}



(d) V_{D5} and V_{DO}



(e) i_{Lin} and i_{Lk}



(f) V_{in} and V_O

Figure 8 The experimental waveforms

3.3 Power Loss Analysis

Utilize SIMetrix-SIMPLIS to evaluate power loss at P_o = 300 W with a purely resistive load of 533 Ω. Given on Figure 9, the efficiency losses mainly originate from the switch and the diodes. The switch incurs a loss of 1.75 W contributing 18% of the total losses, while the diodes account for 7.97 W (82%), leading to a total power loss of 9.72 W This results in an overall system efficiency of approximately 96.9% at an output power of 300 W. The switch and diode losses remain the key factors affecting system efficiency.

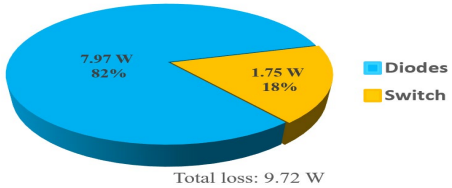


Figure 9 Power-loss distribution of the proposed converter at P_o = 300 W

3.4 Comparison with Other Topologies

A comprehensive comparison between the PC and several recently published high step–up converters [21–25] is summarized in Table 2 and further illustrated in Figures 10(a)–10(b). The following comparison highlights (i) component count, (ii) voltage gain (VG),

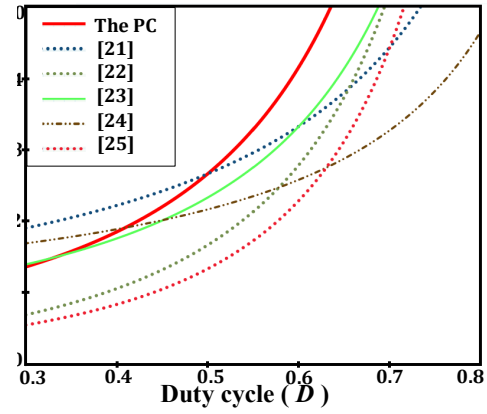
(iii) switch voltage stress (VS), and (iv) full–load efficiency:

- Component count (Table 2): The PC uses only one switch, six diodes, five capacitors, and one coupled inductor (13 components in total). This is less than the more complex designs in [21] and [22], and comparable to those in [23–25]. The reduced number of components not only simplifies the gate–drive and control circuitry but also lowers the overall implementation cost of the converter.
- Voltage gain (Table 2, Figure 10(a)): For n=2, the PC provides a quadratic gain, offering a higher gain at moderate duty cycles than those in [22], [24], and [25]. Although [21] also achieves a high gainl, it requires two switches and more passive components.
  Moreover, the PC's gain expression is simpler and more predictable than that of [23], facilitating analysis and design.
- Switch voltage stress (Table 2, Figure 10(b)): The PC maintains a low. This stress is slightly higher than that in [21], but significantly lower than the variable and often higher than the stress found in [22] and [23]. Compared to [24] and [25], the PC also provides lower or comparable stress, allowing the use of low–voltage MOSFETs with a small $R_{DS(on)}$, which improves both efficiency and reliability.
- Full-load efficiency (Table 2): As reported in Table 2, the PC achieves a full–load efficiency of 95.5%, which is higher than that of [22–25] (93–94.5%), and slightly below the highest value of [21] (97%) which comes at the cost of more components and two switches. This demonstrates that the PC delivers good efficiency with a simpler structure.

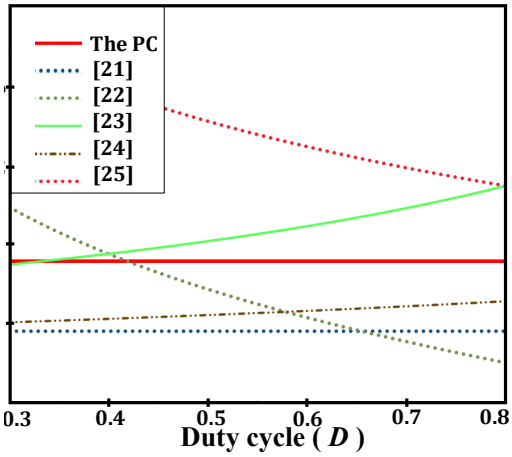
In summary, by combining a compact component count, high and easily predictable quadratic voltage gain, low and stable switch stress, and competitive full-load efficiency, the proposed converter achieves a well-balanced trade–off between performance, simplicity, and practicality. These advantages make it an attractive candidate for high step-up DC-DC applications.

Table 2 Comparison Between The Proposed Converter and Other Step-Up Dc-Dc Converters

Ref.	Number of components				Voltage gains in CCM	VS of switch ($/V_o$)	Eff.
	S	D	C	I/CI			
[21]	2	8	6	0/3	$\frac{3n+2}{1-D}$	$\frac{1}{3n+2}$	97%
[22]	1	5	4	2/2	$\frac{n(D-D^2)+nD+1}{(1-D)^2}$	$\frac{1}{n(D-D^2)+nD+1}$	94%
[23]	2	4	4	1/1	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{1-D}{1+D+2n(1-D)}$	94.5%
[24]	1	8	8	1/1	$\frac{n(2-D)-D+4}{1-D}$	$\frac{1}{n(2-D)-D+4}$	94%
[25]	1	6	4	2/1	$\frac{1+nD}{(1-D)^2}$	$\frac{1}{1+nD}$	93%
PC	1	6	5	1/1	$\frac{2+n}{(1-D)^2}$	$\frac{1}{2+n}$	95.5%



(a)



(b)

Figure 10 Comparison with relevant topologies: (a) VG and (b) VS.

4.0 CONCLUSION

This paper presents a high step-up DC-DC converter with a single switch and a coupled inductor, achieving high voltage gain through a multi–stage voltage–boosting network combined with a coupled inductor's turns ratio, while maintaining a relatively low switch voltage stress. The proposed topology has been thoroughly analyzed and validated through operating principles, steady–state analysis, simulation results, power loss analysis, comparative evaluation, and hardware implementation at 36 V input, 400 V output, and 300 W power. The converter achieves 96.9% efficiency in simulation and 95.5% efficiency in experimental validation, confirming its high performance in terms of voltage gain and component count compared to existing designs. Despite the high voltage gain, the hard–switching operation slightly limits efficiency, and practical implementation requires careful attention to dynamic response, stability, and high–frequency parasitic effects.

The proposed converter fits well with low–voltage renewable energy applications (PV, fuel cells), energy storage systems (12/24/48 V), and as a front–end stage for compact inverters in residential off–grid,

backup, and mobile power applications. Thus, it offers both academic value and strong practical potential for high-voltage DC-DC conversion.

Future work will focus on soft-switching techniques, optimized component design, and extended experimental validation. The topology also has potential for bidirectional conversion, renewable energy integration, and electric vehicle applications, providing a compact and versatile platform for high-voltage DC-DC conversion.

Acknowledgement

This research received no external funding.

Conflicts of Interest

The authors declare no conflict of interest.

References

[1] Sayad, E., T. Wilberforce, K. Elsaid, M. Rabaia, M. Abdelkareem, K. Chae, and A. Olabi. 2021. A Critical Review on Environmental Impacts of Renewable Energy Systems and Mitigation Strategies: Wind, Hydro, Biomass and Geothermal. *Science of the Total Environment*. 766: 144505. https://doi.org/10.1016/j.scitotenv.2020.144505.

[2] Hamed, T., and A. Alshare. 2022. Environmental Impact of Solar and Wind Energy—A Review. *Science of the Total Environment*. 754: 141989. https://doi.org/10.1016/j.scitotenv.2020.144505.

[3] Şen, Z. 2019. Innovative Methodologies in Renewable Energy: A Review. *International Journal of Energy Research*. 43(11): 5621–5658. https://doi.org/10.1002/er.4619.

[4] Al-Thani, H., M. Koç, R. J. Isaifan, and Y. Bicer. 2022. "A Review of the Integrated Renewable Energy Systems for Sustainable Urban Mobility. *Sustainability*. 14(17): 10517. https://doi.org/10.3390/su141710517.

[5] Rahman, M. M., and N. M. Bauid. 2022. The Renewable Energy Sources for Electricity Generation: Short Review. *Maejo International Journal of Energy and Environmental Communication*. 4(1): 29–33. https://doi.org/10.54279/mijeec.v4i1.247736.

[6] He, X., S. Hashimoto, W. Jiang, J. Liu, and T. Kawaguchi. 2023. Design and Implementation of a Low-Voltage Photovoltaic System Integrated with Battery Energy Storage. *Energies*. 16(7): 3057. https://doi.org/10.3390/en16073057.

[7] Alla, R., K. Rajani, and R. T. Yadlapalli. 2024. Performance Analysis of DC–DC Boost Converter with High Gain. In *Proceedings of the Second IEEE International Conference on Measurement, Instrumentation, Control and Automation (ICMICA)*. 1–6. Kurukshetra, India. https://doi.org/10.1109/ICMICA61068.2024.10732039.

[8] Rahimi, T., M. R. Islam, H. Gholizadeh, S. Mahdizadeh, and E. Afjei. 2021. Design and Implementation of a High Step-Up DC–DC Converter Based on the Conventional Boost and Buck–Boost Converters with High Value of Efficiency Suitable for Renewable Application. *Sustainability*. 13: 10699. https://doi.org/10.3390/su131910699.

[9] Gökçegöz, F., E. Akboy, and A. H. Obdan. 2021. Analysis and Design of a Flyback Converter for Universal Input and Wide Load Ranges. *Electrica*. 21(2): 235–241. https://doi.org/10.5152/electrica.2021.20092.

[10] Moradpour, R., and A. Tavakoli. 2020. A DC–DC Boost Converter with High Voltage Gain Integrating Three-Winding Coupled Inductor with Low Input Current Ripple. *International Transactions on Electrical Energy Systems*. 30(6): e12383. https://doi.org/10.1002/2050-7038.12383.

[11] Khalilzadeh, M., and K. Abbaszadeh. 2015. Non-Isolated High Step-Up DC–DC Converter Based on Coupled Inductor with Reduced Voltage Stress. *IET Power Electronics*. 8 (11): 2184–2194. https://doi.org/10.1049/iet-pel.2014.0899.

[12] Pourfarzad, H., M. Saremi, and T. Jalilzadeh. 2020. "An Extended High-Voltage-Gain DC–DC Converter with Reduced Voltage Stress on Switches/Diodes. *Electrical Engineering*. 102(6): 2435–2452. https://doi.org/10.1007/s00202-020-01040-4.

[13] Pajnić, M., P. Pejović, and O. Aleksić. 2018. Design and Analysis of a Novel Coupled Inductor Structure with Variable Coupling Coefficient. *IET Power Electronics*. 11 (6): 1042–1050. https://doi.org/10.1049/iet-pel.2017.0566.

[14] Zhang, H., and J. Wang. 2024. High Boost DC–DC Converter Based on Switched Inductor, Switched Capacitor, and Voltage Multiplier Cells. *Journal of Electrical Engineering*. 12 (2): 124–135. https://doi.org/10.1007/s40998-024-00702-4.

[15] Sadeghpour, D., and J. Bauman. 2022. High-Efficiency Coupled-Inductor Switched-Capacitor Boost Converter with Improved Input Current Ripple. *IEEE Transactions on Industrial Electronics*. 69(8): 7940–7951. https://doi.org/10.1109/TIE.2021.3106397.

[16] He, Y., L. Chen, and X. Sun. 2024. An Integrated Switched Capacitor Coupled Inductor Buck–Boost DC–DC Converter. *IEICE Electronics Express*. 21 (11): 20240211. https://doi.org/10.1587/elex.21.20240211.

[17] Rajabi, A., F. Mohammadzadeh Shahir, and E. Babaei. 2021. Designing a Novel Voltage-Lift Technique Based Non-Isolated Boost DC–DC Converter with High Voltage Gain. *International Transactions on Electrical Energy Systems*. 31(12): e13213. https://doi.org/10.1002/2050-7038.13213.

[18] Shayeghi, H., R. Mohajery, M. Hosseinpour, F. Sedaghati, and N. Bizon. 2023. A Transformer-Less High Voltage Gain DC–DC Converter Based on Cuk Converter and Voltage-Lift Technique. *Journal of Electrical Engineering & Technology*. 18(5): 1991–2001. https://doi.org/10.5370/JEET.2023.18.5.1991.

[19] Vesali, M. 2023. A New Three-Winding Coupled Inductors High Step-Up DC–DC Converter with Low Input Current Ripple. *IET Power Electronics*. 16(12): 2022–2033. https://doi.org/10.1049/pel2.12522.

[20] Alilou, S. M., M. Maalandish, A. Samadian, P. Abolhassani, S. H. Hosseini, and M. H. Khooban. 2023. A New High Step-Up DC–DC Converter Using Voltage Lift Techniques Suitable for Renewable Applications. *CSEE Journal of Power and Energy Systems*. 9(1): 56–68. https://doi.org/10.17775/CSEEJPES.2022.02910.

[21] Semiromizadeh, J., H. Izadi, and E. Adib. 2022. High Step-Up Interleaved DC–DC Converter for Photovoltaic Systems. *IET Power Electronics* 15: 33–42. https://doi.org/10.1049/pel2.12210.

[22] Andrade, A. M. S. S., L. Schuch, and M. L. da Silva Martins. 2019. Analysis and Design of High-Efficiency Hybrid High Step-Up DC–DC Converter for Distributed PV Generation Systems. *IEEE Transactions on Industrial Electronics*. 66(5): 3860–3868. https://doi.org/10.1109/TIE.2018.2840496.

[23] Guepfrih, M. F., G. Waltrich, and T. B. Lazzarin. 2019. Quadratic-Boost-Double-Flyback Converter. *IET Power Electronics*. 12(16): 3166–3177. https://doi.org/10.1049/iet-pel.2019.0340.

[24] Hasanpour, S., Y. P. Siwakoti, A. Mostaan, and F. Blaabjerg. 2020. New Semi-Quadratic High Step-Up DC/DC Converter for Renewable Energy Applications. *IEEE Transactions on Power Electronics*. 1–11. https://doi.org/10.1109/TPEL.2020.2999402.

[25] Modaberi, S. A., B. Allahverdinejad, and M. R. Banaei. 2021. A Quadratic High Step-Up DC–DC Boost Converter Based on Coupled Inductor with Single Switch and Continuous Input Current. In *Proceedings of the 12th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*. 1–6. Tabriz, Iran. https://doi.org/10.1109/PEDSTC52094.2021.9405958.

[26] Rahimi, R., S. Habibi, M. Ferdowsi, and P. Shamsi. 2022. An Interleaved High Step-Up DC–DC Converter with Coupled

Inductor and Built-In Transformer for Renewable Energy Applications. In *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 1–6. Detroit, MI. https://doi.org/10.1109/ECCE50734.2022.9948130.

[27] Rahimi, R., S. Habibi, M. Ferdowsi, and P. Shamsi. 2021. An Interleaved Quadratic High Step-Up DC–DC Converter with Coupled Inductor. *IEEE Open Journal of Power Electronics.* 2: 647–658. https://doi.org/10.1109/OJPEL.2021.3133911.

[28] Hasanpour, S., Y. P. Siwakoti, A. Mostaan, and F. Blaabjerg. 2021. "New Semi-Quadratic High Step-Up DC/DC Converter for Renewable Energy Applications. *IEEE Transactions on Power Electronics.* 36(1): 433–446. https://doi.org/10.1109/TPEL.2020.2999402.

[29] Tarzamni, H., H. S. Gohari, M. Sabahi, and J. Kyyrä. 2024. Nonisolated High Step-Up DC–DC Converters: Comparative Review and Metrics Applicability. *IEEE Transactions on Power Electronics.* 39(1): 582–625. https://doi.org/10.1109/TPEL.2023.3264172.