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Performance Analysis of Memristor Models for RRAM Cell Array Design using SILVACO EDA

Nor Zaidi Haron*, Norsuhaidah Arshad, Fauziyah Salehuddin

Centre for Telecommunication Research and Innovation, Faculty of Electronic and Computer Engineering, Universiti Teknikal Malaysia Melaka Hang Tuah Jaya, 76100, Durian Tunggal, Melaka, Malaysia

*Corresponding author: zaidi@utem.edu.my

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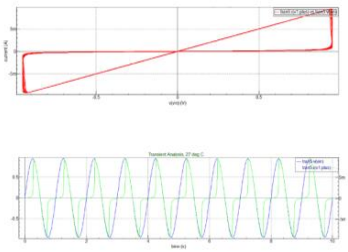
Graphical abstract



Abstract

Resistive Random Access Memory (RRAM) is gaining attention as one of the prominent contenders to replace the conventional memory technologies such as SRAM, DRAM and Flash. This emerging memory uses scaled CMOS devices (22 nm or less) to form the peripheral circuits such as decoder and sense amplifier; while a non-CMOS device known as memristor is used to form the cell array. Although potentially becoming the main future memory, RRAM is anticipated to be impacted by the high manufacturing defect density that in turn might lead to quality and reliability problems. This paper presents the initial work towards producing a high quality and reliable RRAM devices. A design and simulation of three memristor SPICE models published in prominent literatures were performed using Silvaco EDA simulation tool. The aim is to identify the optimal model to be used in our RRAM design, which is based on 22 nm CMOS technology. Performance analysis shows that the model proposed by D. Biolek is suitable to be used in our RRAM design.

Keywords: Memristor; RRAM; SPICE modeling; quality; reliability

1.0 INTRODUCTION

Resistive Random Access Memory (RRAM) is gaining attention as one of the prominent contenders to replace the conventional memory technologies (such as SRAM, DRAM and Flash). This emerging memory uses scaled CMOS devices (22 nm or less) to form the peripheral circuits such as decoder and sense amplifier; while a non-CMOS device known as memristor is used to form the cell array. Memristors are non-linear two terminal devices that can memorize the resistive state. The combination of novel devices and advanced circuit architecture enables RRAM to offer benefits such as ultrascale storage capacity, low power consumption and fast data access [1-3].

Although potentially to be the main future memory, there are many challenges need to be addressed including design, fabrication, performance-cost, quality and reliability issues [2]. In terms of quality and reliability, RRAM is anticipated to be impacted by high manufacturing defects and faults [3-5]. Testing for quality and reliability improvement requires engineers to study the behavior of the product they manufactured. In the perspective of memory test, understanding the faulty behavior of RRAM in the presence of defects will enable the development of appropriate fault models and efficient test schemes; thus, improve the outgoing product. Yet, these quality improvement activities could be done efficiently with the availability of appropriate electrical models, something that is lacking at the moment. Moreover, existing test schemes may not detect the faulty behaviors of RRAM cells as the components are based on non-CMOS devices.

This paper presents the initial work towards producing a high quality and reliable RRAM devices. A design and simulation of three memristor SPICE models published in prominent literatures was performed using Silvaco Electronic Design Automation (EDA) simulation tool. The aim is to identify the optimal memristor model to be used in our RRAM design, which is based on 22 nm CMOS technology. Performance analysis shows that the memristor model proposed by Biolek *et al*. in 2013 is suitable to be used in our RRAM design [6].

The paper is organized as follows. Section 1 presents the background used to understand the work presented including the memory model concept, functional and electrical RRAM model, and RRAM operation. Section 2 reviews the three considered memristor models used in our experiment. Section 3 provides the simulation results and performance analysis. Finally, Section 4 concludes the paper.

1.1 Memory Models

In order to evaluate a memory system in a simple manner and short time duration, a top-down hierarchical modeling is commonly utilized [7]. This approach eases the description and evaluation of

memory systems using simulation tools. The top-down hierarchical approach is carried out by dividing the models into several abstraction levels as shown in Figure 1. The behavioral model is the highest abstraction level and the layout model is the lowest abstraction level. As the abstraction levels shift from the highest to the lowest, the model provides lesser information about the memory functionality and more about the memory physical structure. Simulation time increases as the abstraction levels shift from the highest toward the lowest. Functional and electrical models are the most common models used in modeling a memory.

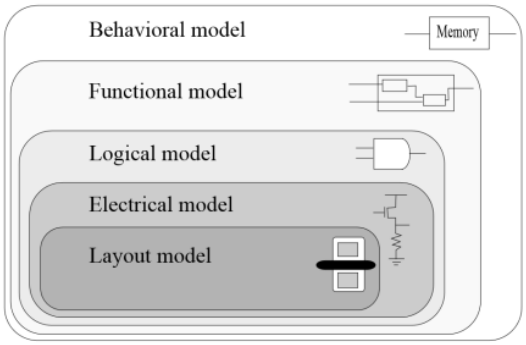


Figure 1 Abstraction levels of memory modeling [7]

1.2 Functional RRAM Model

Functional model comprises a collection of functional blocks that interrelate with each other to accomplish a specific function. Figure 2 illustrates a functional model of RRAM that consists of four main blocks including of the memory cell array, row/column decoder, a sense amplifier, a pulse generator and a read/write (R/W) selector [8].

The memory cells, which are the main unit, are structured in an array of horizontal rows and vertical columns. Each memory cell is capable of storing one bit of binary information. It also shares a common connection with other cells in the same row and other common connection with other cells in the same column. The decoder enables access to a particular memory cell according to address coming from outside of the memory array. The sense amplifier senses the read current of the accessed memory cell. The current will be converted into a voltage and be amplified prior to sending the output data to the data register. The pulse generator generates read/write pattern signals. The read/write (R/W) selector switches the memristor to ground for writing operation and reference resistance for reading operation.

1.3 Electrical RRAM Model

The electrical model describes the electrical components that construct the memory. At this level, the functional blocks and logic gates of the memory are described using electrical components such as resistors, transistor and capacitors. For RRAM, except the memory cell array, the other units are built using standard CMOS transistors and resistors [9].

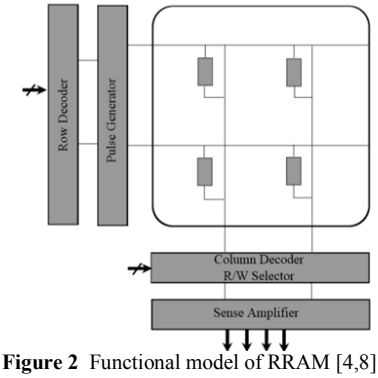


Figure 2 Functional model of RRAM [4,8]

The RRAM cell array gets special attention and will be described in detailed as it is formed using a novel non-CMOS device known as memristor [10]. Memristor consists of two metal electrodes, *Pt* separated by a thin film of titanium oxide. As shown in Figure 3(a), the thin film with Lnm long is divided into two regions: doped (TiO2-x) region with length *w* and undoped region (TiO2) with length (*L*-*w*) [11].

When applying a positive voltage through the memristor, the oxygen vacancies drift toward the undoped region reducing the memristance. When the memristor is fully doped, the lowest possible memristance, $M=R_{on}$ is achieved. On the other hand, the oxygen vacancies drift toward the doped region when a negative voltage is applied through the device. In this situation, the memristance increases. When the undoped region dominates the device the highest possible memristance, $M=R_{off}$ is achieved. When the power supply is removed, the oxygen vacancies stop and remain fixed [12].

Strukov *et al.* [11] modeled memristor as two resistors connected in series as shown in Figure 3(b). The voltage-current relation of the memristor is given as:

$$v = iM(x) = i[R_{on}w/L + R_{off}(1-w/L)] \quad (1)$$

where M is the total memristance, *x* is the normalized length of the doped region to the total length of the memristor$x=w/L$. At time t, the amount of charge that passes through the memristor determines *w*. Given μ_v is the average oxygen vacancy mobility, the time derivative of *w* is described as:

$$dw/dt = \mu_v R_{on} i(t)/L \quad (2)$$

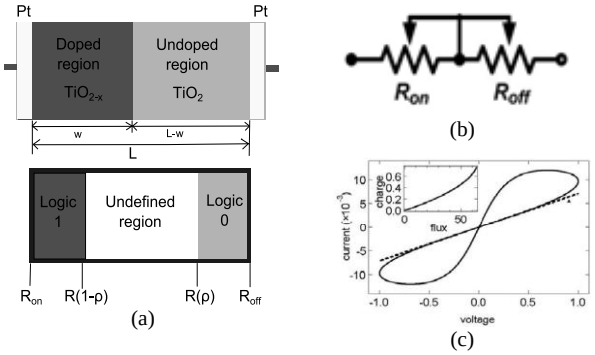


Figure 3 Memristor: (a) model (b) electrical equivalent circuit (c) I-V curve [9]

One of the main properties of memristors is the existence of a pinched current-voltage (I-V) hysteresis effect as shown in Figure 3(c). This I-V hysteresis effect is persistent and controllable making memristors suitable for non-volatile memory cells. To ensure that RRAM operates binary data correctly, logic 1 is defined when $R_{on} \leq M(t) \leq R(1-p)$, logic 0 when $R(1-p) \leq M(t) \leq R_{off}$ and safety margin when $R(1-p) \leq M(t) \leq R(p)$ where $0 \leq p \leq 1$; see Figure 3(a).

1.4 RRAM Operations

Write operations are performed by applying the appropriate voltage polarity as shown in Figure 4 [13]. The write duration must capable to set the memristance from $M=R_{off}$ to $M=R_{on}$ and vice-versa. Therefore, applying a voltage through a memristor causes the memristance to change its state from $M=R_{off}$ to $M=R_{on}$ and vice-versa. A positive voltage is applied through the memristor for a specific time to write logic 1. Meanwhile, to write a logic 0, the negative voltage is applied across the memristor for a fixed duration.

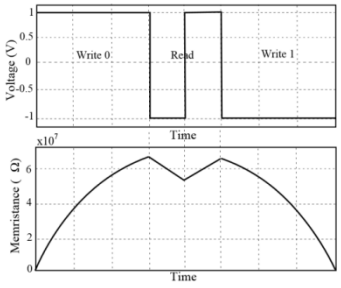


Figure 4 Variation of memristance due to voltage over time [13]

Because of this mechanism, two phases of read operation are required to ensure that the memristor retains its memristance after the read operation. As shown in Figure 4, a negative pulse followed immediately with positive pulse with the same magnitude and duration creates a zero net change in memristance.

2.0 CONSIDERED MEMRISTOR MODELS

This section describes the concept and design of the considered memristor models. Three SPICE memristor models proposed by Joglekar *et al.* [14], Prodromakis *et al*. [15] and Biolek *et al*. [6] were used in the work. The description of these memristor models begins with the mathematical derivation that expresses their electrical behavior followed by the SPICE code.

2.1 Joglekar's Memristor Model

Joglekar *et al.* [14] argued that the memristor model proposed by Strukov *et al*.[10] has some errors when w approaches the boundaries, $w \sim 0$ or $w \sim L$. This "boundary effect" is due to the influence of a non-uniform electric field that significantly suppresses the drift of the dopants. Hence, Joglekar *et al.* introduced a window function expressed as follows [14]:

$$f(x) = 1 - (2x-1)^{2p} \tag{3}$$

where p is a positive exponent parameter and x is the normalized length of the doped region to the total length of the memristor $x=w/L$. This window function confirms zero drift at the boundaries. Introducing this window function alters the time derivative of the doped region of Equation (2) and in turn the state variable becoming:

$$dx/dt = \mu_v R_{on} i(t) f(x) / L^2 \tag{4}$$

Figure 5 gives the SPICE code for the Joglekar's memristor model. More detailed explanation of the code can be referred to Joglekar's paper [14].

```
* Ron, Roff - Resistance in ON / OFF States
* Rinit - Resistance at T=0
* D - Width of the thin film
* uv - Migration coefficient
* p - Parameter of the WINDOW-function
* for modeling nonlinear boundary conditions
* x - W/D Ratio, W is the actual width
* of the doped area (from 0 to D)
.SUBCKT memristor_joglekar plus minus PARAMS:
+ Ron=100 Roff=16K Rinit=11K D=10N uv=10F p=10
**********************************************
* DIFFERENTIAL EQUATION MODELING *
**********************************************
Gx 0 x value={ I(Emem)*uv*Ron/D**2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
* RESISTIVE PORT OF THE MEMRISTOR *
*******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
**********************************************
*Flux computation*
**********************************************
Eflux flux 0 value={SDT(V(plus,minus))}
**********************************************
*Charge computation*
**********************************************
Echarge charge 0 value={SDT(I(Emem))}
**********************************************
* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
**********************************************
*window function, according to Joglekar
.func f(x,p)={1-(2*x-1)**(2*p)}
.ENDS memristor
```

Figure 5 SPICE code of the memristor model proposed by Joglekar *et al.* [14]

2.2 Prodromarkis's Memristor Model

Like Joglekar *et al.,* Prodromakis *et al*. [15] claimed that the memristor model proposed by Strukov *et al*. suffers from a severe drawback. When the memristor is completely doped, $w=L$; the memristance is lower than the lowest possible memristance, $M<R_{on}$. A similar condition happens when the memristor is completely undoped, $w=0$; the memristance exceeds the highest possible memristance, $M>R_{off}$. Prodromakis *et al*. also argued that their model solves the "terminal-state problem" that occur in Joglekar's model. Based on these arguments, Prodromakis *et al*. proposed window function as follows [15]:

$$f(x) = 1 - [(x-0.5)^2 + 0.75]^p \tag{5}$$

where p is a control parameter that is used to integrate scalability and flexibility in window function $f(x)$. Prodromakis provides a comprehensive explanation of window function in his literature [16].

The SPICE code for Prodromakis' memristor model is given in Figure 6. Except for the second last instruction that describes the window function, the other SPICE instructions are the same with those used by Joglekar *et al.*

```
* Ron, Roff - Resistance in ON / OFF States
* Rinit - Resistance at T=0
* D - Width of the thin film
* uv - Migration coefficient
* p - Parameter of the WINDOW-function
* for modeling nonlinear boundary conditions
* x - W/D Ratio, W is the actual width
* of the doped area (from 0 to D)
*
.SUBCKT memristor_prodromakis plus minus PARAMS:
+ Ron=100 Roff=16K Rinit=11K D=10N uv=10F p=10 j=1
**********************************************
* DIFFERENTIAL EQUATION MODELING *
**********************************************
Gx 0 x value={I(Emem)*uv*Ron/D**2*f(V(x),p)}
Cx x 0 1 IC={(Roff-Rinit)/(Roff-Ron)}
Raux x 0 1T
*******************************
* RESISTIVE PORT OF THE MEMRISTOR *
*******************************
Emem plus aux value={-I(Emem)*V(x)*(Roff-Ron)}
Roff aux minus {Roff}
**********************************************
*Flux computation*
**********************************************
Eflux flux 0 value={SDT(V(plus,minus))}
**********************************************
*Charge computation*
**********************************************
Echarge charge 0 value={SDT(I(Emem))}
**********************************************
* WINDOW FUNCTIONS
* FOR NONLINEAR DRIFT MODELING *
**********************************************
*window function, according to prodromakis
.func f(x,p)=1-((((x-0.5)**2)+0.75)**p)
.ENDS memristor
```

Figure 6 SPICE code of the memristor model proposed by Prodromakis *et al.* [15]

2.3 Biolek's Memristor Model

Similarly, Biolek *et al.* oppose the memristor model proposed by Strukov. By considering the boundary value of memristance Biolek's model is described by [6]:

$$R(q(t)) = R_{off} + \frac{R_{on} - R_{off}}{ae^{-4kq(t)} + 1}, \text{a} = \frac{R_{ini} - R_{off}}{R_{off} - R_{ini}} \quad (6)$$

where k is a constant and R_{on} and R_{off} are limiting values of memristance. Equation (6) represents the memristance as a function of the native state variable q. The SPICE code of the Biolek's model is given in Figure 7.

```
.subckt memristorR1 plus minus Ron=100 Roff=10k Rini=5k
.paramuv=10f D=10n k='uv*Ron/D**2'
 a='(Rini-Ron)/(Roff-Rini)'
 *model of memristive port
 Roff plus aux 'Roff'
 Eres aux minus
 vol='(Ron-Roff)/(1+a*exp(-4*k*V(q)))*I(Eres)'
 *end of the model of memristive port
 *integrator model
 Gx 0 Q cur='i(Eres)'
 Cinit Q 0 1
 Raux Q 0 100meg
 *end of the integrator model
 .ends memristorR1
```

Figure 7 SPICE code of the memristor model proposed by Biolek *et al.* [6]

3.0 EXPERIMENTAL RESULTS AND DISCUSSION

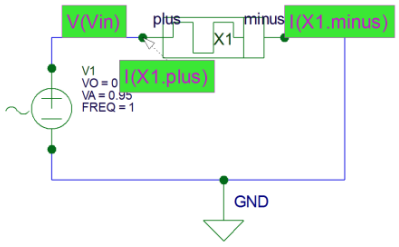
The functionality of the proposed models was evaluated using SILVACO EDA simulation tools. All of the SPICE models are used to create the symbols in the Gateway. Three performance characteristics were carried out: current versus voltage (I-V), current versus time (I-T) and voltage versus time (V-T) under sinewave voltage source, and I-T and V-T under squarewave voltage source.

3.1 Joglekar's Memristor Model

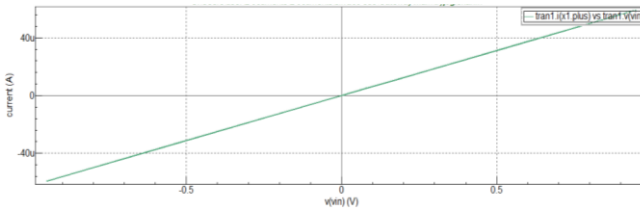
Figure 8(a) illustrates the simulation circuit set up for the Joglekar's memristor model in the SILVACO EDA simulation tools. The created memristor symbol was connected to the voltage source with a sinewaveform supplied with Vdd=0.95 V at 1 Hz frequency. A squarewave voltage source was also used in the simulation. Note that the Vdd value was chosen so that the model can work with the 22 nm CMOS technology, which is used to form the decoder and sense amplifier circuitries.

Figure 8(b), (c) and (d) shows the simulation results for Joglekar's model for each of the three performance characteristics, respectively. The I-V curve shows that the model cannot exhibits the pinched hysteresis effect. For the I-T and V-T waveforms supplied with sinewave, it is observed that the voltage and current go at the same rate; this result contradicts to the theoretical concept of memristors whereby the voltage lags current by some sinewave phase [11].

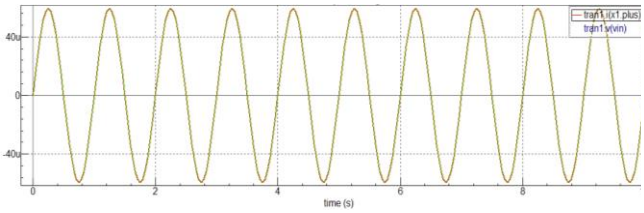
From this simulation, we deduce that this model is not suitable to be used in our RRAM. This is due to the fact that the optimum model must exhibit almost ideal behavior as close as the theoretical model so that it gives an accurate faulty behavior when defect is injected into it. Accurate faulty behavior will then define the efficient test algorithms for high quality testing.



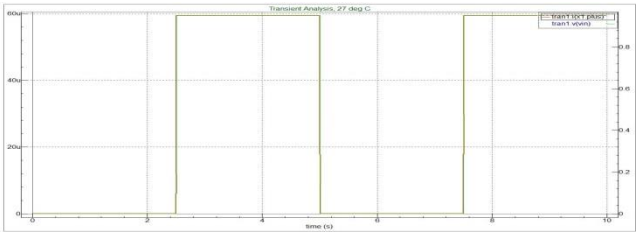
(a)



(b)



(c)

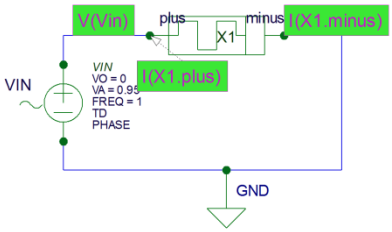


(d)

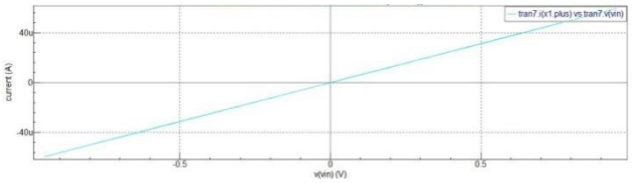
Figure 8 (a) Simulation circuit for the Joglekar'smemristor model (b) simulation results for I-V curve, (c) simulation results for I-T and V-T under sinewave voltage source, (d) simulation results for I-T and V-T under squarewavevolltage source

3.2 Prodromakis' Memristor Model

The same simulation setup was used to simulate the Prodromakis' model as shown in Figure 9(a). Figure 9(b), (c) and (d) shows the simulation results for the Prodomakis' model for each of the three performance characteristics, respectively. All three results are almost the same with the results produced by the Joglekar's model. Both current and voltage shows the results are in the same phase.



(a)



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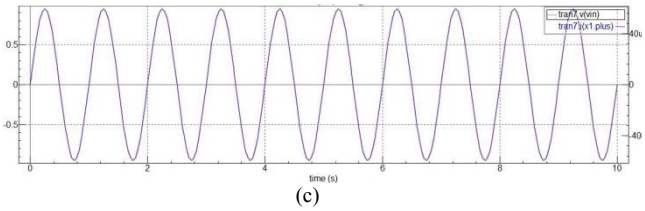
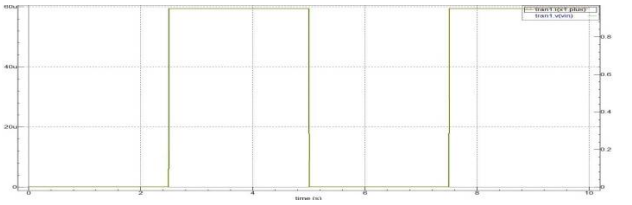


(c)

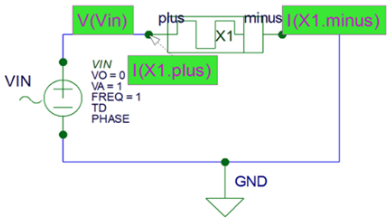


(d)

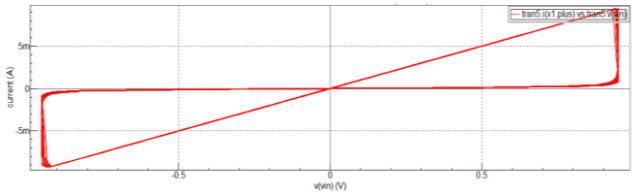
Figure 9 (a) Simulation circuit for the Prodoromakis' memristor model (b) simulation results for I-V curve, (c) simulation results for I-T and V-T under sinewave voltage source, (d) simulation results for I-T and V-T under squarewave voltage source

3.3 Biolek's Memristor Model

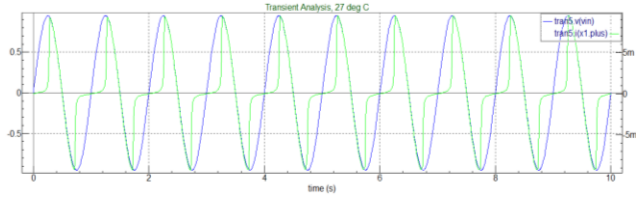
The simulation set up that was used to simulate the Biolek's model is shown in Figure 10(a). Figure 10(b), (c) and (d) shows the simulation results for Biolek's model for each of the three performance characteristics, respectively. All of the three results show the best simulation results in terms of current, voltage and time relationship characteristics for 0.95 V operation. The simulation provides exact results as revealed by Biolek.



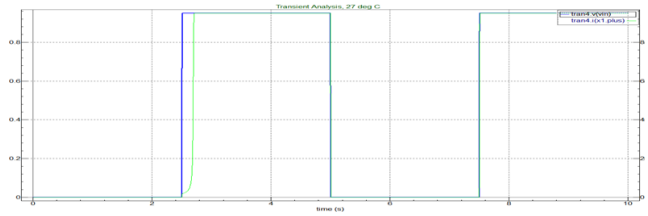
(a)



(b)



(c)



(d)

Figure 10 (a) Simulation circuit for the Biolek'smemristor model (b) simulation results for I-V curve, (c) simulation results for I-T and V-T under sinewave voltage source, (d) simulation results for I-T and V-T under squarewave voltage source

■4.0 CONCLUSION

This paper presented a preliminary study of designing the electrical model of RRAM. At this stage, the optimal memristor model needs to be carefully chosen as it will be used as the RRAM cells where the defect injection and simulation will be carried out. The electrical behavior of the memristor-based RRAM cells will determine the correct fault analysis and test development. To achieve this aim, three existing memristor models have been studied, simulated and analyzed. Of the three models, Biolek's model shows the best simulation results in terms of the current, voltage and time relationship characteristics for 0.95 V operation. The Joglekar's and Prodromakis' models provide similar results, yet they are not suitable for our complete RRAM design. Future

work is to integrate the Biolek's memristor model into our RRAM design followed by fault analysis and test development.

Acknowledgement

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