Jurnal Teknologi, 45(D) Dis. 2006: 153-165

SIMULATION OF ULTRA SHALLOW JUNCTION FORMATION FOR NANO DEVICES APPLICATIONS BY DOPANT DIFFUSION FROM SPIN ON GLASSES

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Abstract. For realizing deep submicron MOSFETs, ultra shallow junctions with low sheet resistance and high doping concentrations are required to suppress short channel effects and to increase the performance. In this paper, ultra shallow junctions were simulated using ATHENA software package from Silvaco TCAD Tools to model the diffusion from spin on dopant (SOD) into silicon. High performance 40 nm P^+N shallow junction fabricated by rapid thermal diffusion of B150 into silicon have been obtained. The junction showed very good characteristics with leakage currents as low as 0.5 nA/cm^2. Shallow junctions less than 20 nm have also been obtained but the quality was not very good due to very high surface leakage current. Junction formation by diffusion of polysilicon layer on Si substrates then SOD layer deposition on top of it produced shallower junctions with low sheet resistance.

Key words: Ultra shallow junction, MOSFET, ULSI, diffusion, spin on dopant, ATHENA, ATLAS

Abstrak. Bagi merealisasikan MOSFET submikron, simpangan cetek ultra berkerintangan rendah diperlukan bagi menghalang kesan saluran pendek dan bagi meningkatkan peranti. Dalam kajian ini, pembentukan simpangan cetek ultra disimulasikan menggunakan perisian ATHENA dan Silvaco Inc. bagi memodelkan resapan dari SOD ke dalam silikon. Simpangan ultra P^+N berkualiti tinggi dengan kedalaman 40 nm telah dibentuk menggunakan ciri-ciri yang baik dengan arus bocor serendah 0.5 na/cm^2. Simpangan cetek kurang daripada turut diperoleh tetapi kualiti simpangan-simpangan cetek ini kurang baik disebabkan oleh arus bocor permukaan yang tinggi. Pembentukan simpangan dari resapan lapisan polisilikon di atas silikon diikuti oleh SOD di atasnya menghasilkan simpangan yang lebih cetek yang berkerintangan rendah.

Kata kunci: Simpangan cetek ultra, resapan, SOD, ATHENA, MOSFET

1.0 INTRODUCTION

The continued growth in portable devices results in the emphasis on lower power and faster semiconductor devices. The grand challenges to the

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Semiconductor Industry are described in International Technology Roadmap for Semiconductor (ITRS) [1-3]. One of these challenges is the requirement for the continuing reduction of junction depth of shallow junctions [1-4]. Shallow junction formation is one of the most important issues in MOSFER scaling. As ultra-large-scale integrated (ULSI) technology moves below the technology node, tight control of the depth of ultra shallow junctions become critical [5]. Shallow junctions must also have low sheet resistance [5, 6]. Producing highly doped and fully activated shallow with low sheet reistance will be needed.

Shown in Figure 1 is a plot of the ITRS projections for the sheet resistance of the ptype source/drain junctions in 1999, 2001 and 2003 editions. We can see that initially instantaneous reduction of both junction depth and sheet resistance was considered possible. In subsequent editions, the requirements on the sheet resistance have been lenient. The sudden drop in the sheet resistance predicted by ITRS 2003 is motivated by a change in the device structure [5].

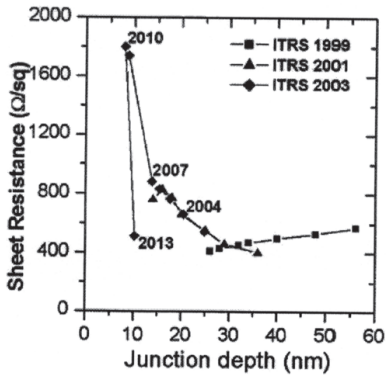

Figure 1 Plot of the sheet resistance vs. junction depth predictions made in 1999, 2001 and 2003 editions of ITRS [5]

In the past, it was possible to increase the active concentration and at the same time decrease the sheet resistance and the junction depth. It is becoming progressively more difficult to continue increasing the active concentration in the junctions using current junction formation techniques. As a result, subsequent versions of the ITRS laid-back the requirements on the sheet resistance allowing it to increase as the junction depth is reduced [5].

The ITRS calling for shallow junction forces the exploration of alternate doping technologies. It is expected that an alternative method is developed to form the ultra shallow junction with the lower sheet resistance. Diffusion from spin-on dopant (SOD) is one of the candidates to form such ultra shallow junction

with lower sheet resistance. The diffuision using SOD which is based on the diffusion technique using liquid sources has ben applied since the seventies but recently, SOD has become more popular in IC processing [6].

2.0 SIMULATION PROCESS

We have used the SSUPREM-4 embedded in the ATHENA software package in order to simulate the diffusion from SOD into silicon. The initial wafer structure used in our model was 8 Ωcm^{-2} and <100> oriented silicon wafer. Diodes were realized usingdifferent active windows for electrical characterization of PN junctions. We have used conventional furnace and rapid thermal diffusion to diffuse SOD layer into silicon to form PN junctions.

Boron was used on n-Si to form P^+N junction and phosphorus was used on p-Si wafer to form N^+P junction. There is no SOD diffusion model acailable in the ATHENA software. However, due to the similar diffusion behaviour of impurities from SOD and doped oxide into silicon, the diffusion of impurities from SOD has been simulated using the doped oxide model.

Figure 2 and 3 show the structure of P^+N shallow junction using furnace diffusion and rapid thermal diffusion. The boron concentration was chosen to be $7.0x10^{21}$ions/cm^3. The diffused time for furnace annealing was 30 minutes and 20 seconds for rapid thermal annealing. Figure 4 shows N^+P junction structure at temperature for 30 minutes inconventional furnace diffusion. The phosphorus concentration was chosen to be 8.0×10^{21}.ions/cm^3.

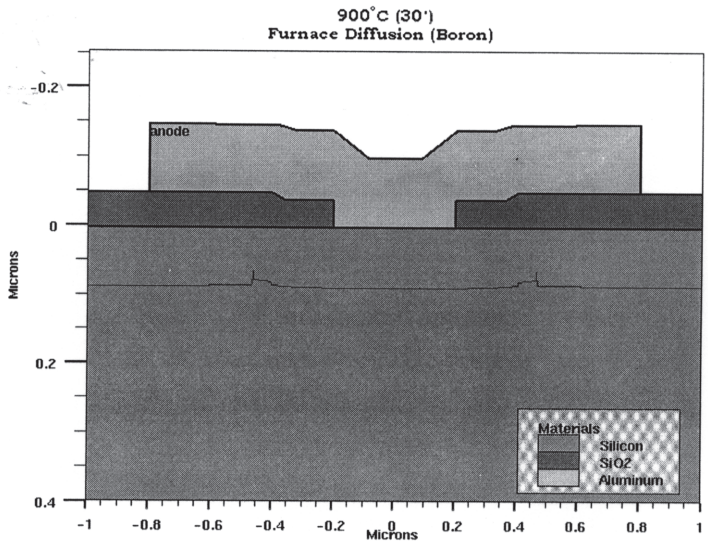

Figure 2 Structure of P^+N junction at 900°C for 30 minutes using furnace diffusion

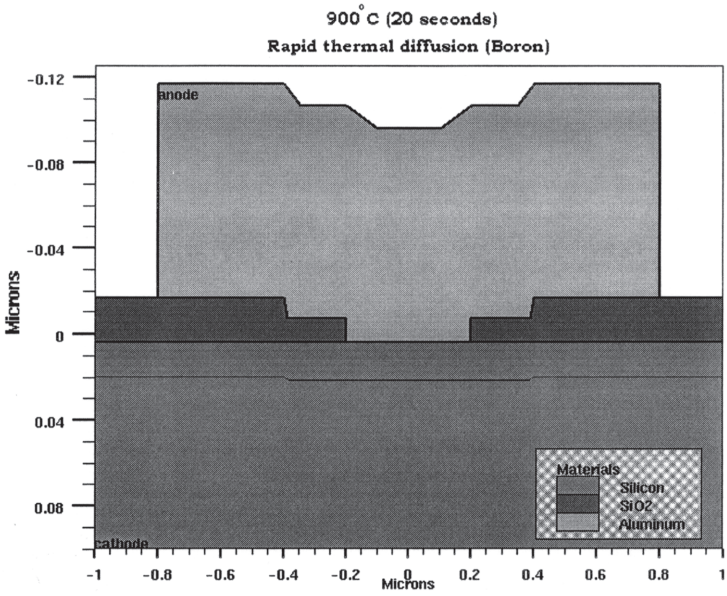

Figure 3 N^+P junction structure of rapid thermal diffusion at 900°C for 20 seconds

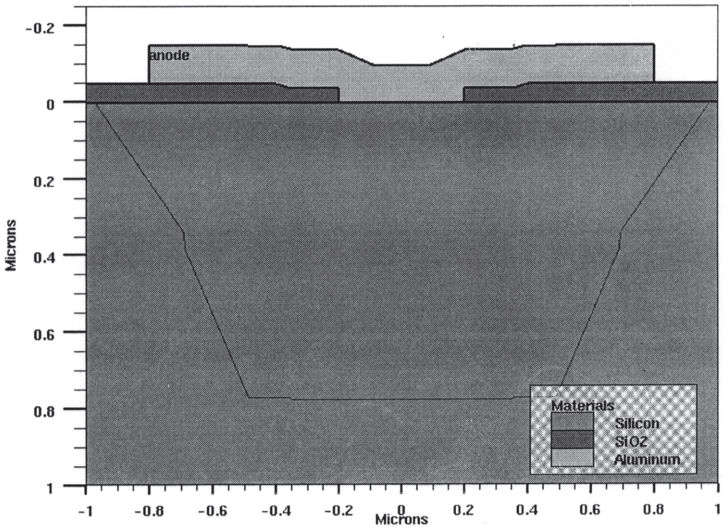

Figure 4 PN junction structure

As stated earlier, diffusion from SOD into silicon was able to create ultra shallow junction. However, the sheet resistance became increasingly high. In order to overcome this problem, junction formation for the diode structure by diffusion from polysilicon layer then doped by diffusion from spin on dopant

also investigated. This structure has advantages of low sheet resistance. Figure 5 illustrates the structurre of P^+N shallow junction with polysilicon layer on top.

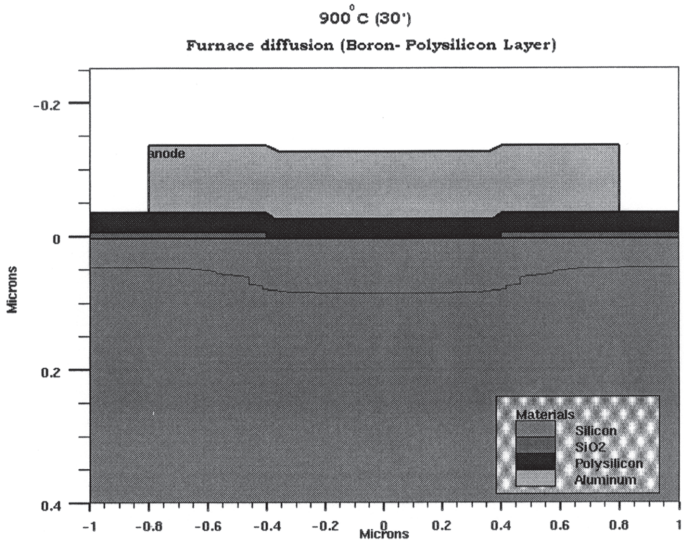

Figure 5 PN junction that has polysilicon layer on top

Diffusion of boron and phosphorus into dilicon through polysilicon was carried out in almost the same way as P^+N shallow junction formation for boron and phosphorus diffusion into silicon. The only difference was that there was a polydilicon layer depodited on mono silicon before SOD deposition to serve as capping layer for dopant diffusion from SOD source.

3.0 RESULTS AND DISCUSSION

3.1 Boron Diffusion

Conventional furnace diffusion

Figure 6, 7 and 8 show the SRP profiles abtained for boron diffusion at 900°C and in nitrogen ambient. The shallowest junction was obtained for boron diffused for 30 minutes in nitrogen. The results are presented in Table 1. Table 1 shows the comparison between the junction depths extracted from SRP profiles and the sheet resistance values from experimental work done by N.N Toan [6] and the simulated values at every condition.

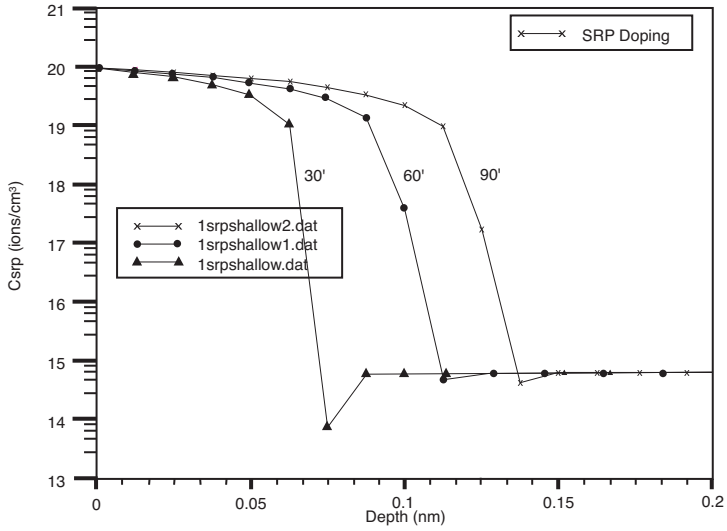

Figure 6 SRP profiles of boron using furnace diffusion at 900°C

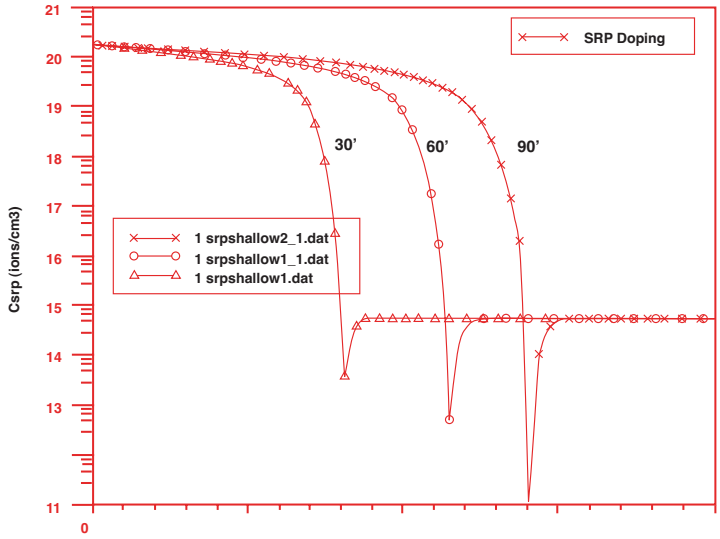

Figure 7 SRP profiles of boron using furnace diffusion at 1 000°C

After changing many values of boron diffusivity in SOD layer and silicon substrate [6], the best fitted profiles were abtained for diffusion at 900°C and 1°C. There was only slightly defferent between profile measurements and simulation results. At 1000°C, the simulated profiles were always deeper than the measured profiles. In this simulation process, the boron diffusivity in SOD

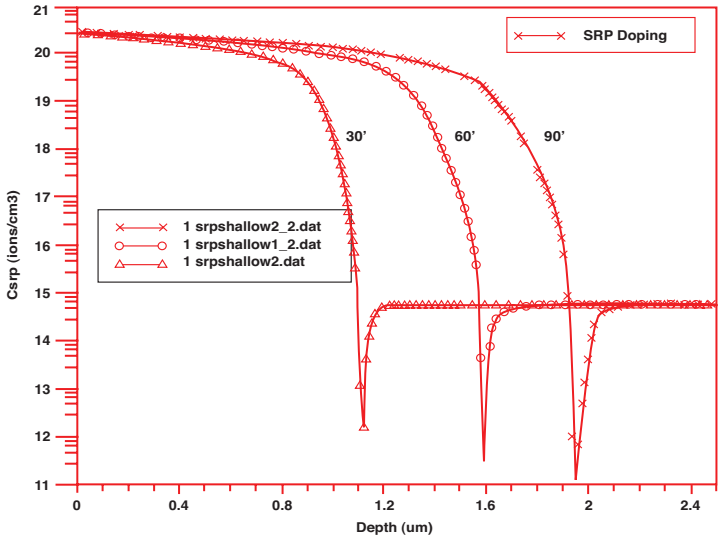

Figure 8 SRP profiles of boron using furnace diffusion at 1 100°C

Table 1 Sheet resistances and junction depths vs. temperatures and times

	900°C				1000°C				1100°C			
t (minit)	Rs(Ω/cm²)		Xj(μm)		Rs(Ω/cm²)		Xj(μm)		Rs(W/cm²)		Xj(μm)	
30	4pp	Sim	SRP	Sim	4pp	Sim	SRP	Sim	4pp	Sim	SRP	Sim
	359.5	346.9	0.08	0.08	46.3	43.9	0.25	0.35	11.9	8.15	1.2	1.16
60	200.3	235.3	0.14	0.12	38.7	30.5	0.34	0.50	8.5	5.8	1.48	1.64
90	150.7	188.5	0.16	0.15	34.1	24.7	0.41	0.61	5.0	4.6	1.80	2.01

had the pre-factor (DIX.0) value of 1.00cm²/s and the activation energy (DIX.E) 3.00eV. The boron diffusivity in SOD layer was much higher than the default diffusivity of boron in oxide [6].

From the shown table and graphs, diffusion at high temperature can increase the junction depth. When temperature was increased, the impurity atoms have more energy and will increase the diffusion speed thus the impurity atoms will diffuse deeper into silicon [7]. The abjective to frorm junction less than 50 mm in depth has not been achieved. In order to solve this problem, boron diffusion using rapid thermal diffusion was simulated.

Rapid thermal diffusion

The simulation was carried out using the same diffusivity values of boron in SOD layer as stated above, D1X.0=1.00 cm_2/s and DIX.E=3eV. All other parameters used the default values. The sheet resistance values were extracted and compared with the measured values as listed in Table 2. The diffusivity of boron in silicon which was found in the previous part was applied here but it resulted in very high sheet resistance values. Therefore, we have used default value of boron diffusivity in silicon. According to simulated profiles, shallow junctions of approximately 18 nm, 25 nm, 41 nm, and 71 nm were obtained for samples diffused at RTD temperatures respectively. The sheet resistances were found about the same as the measured value done by N. N. Toan [6]. Figure 9 show the simulated net doping profiles of boron at different temperatures for 20 seconds in nitrogen ambient.

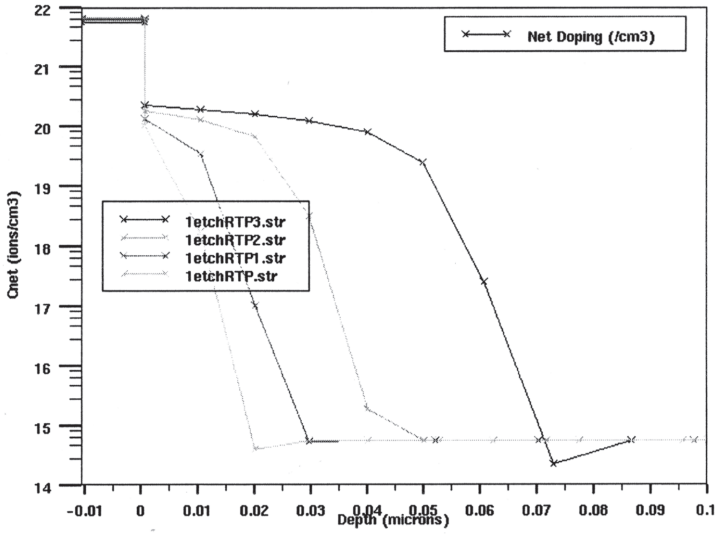

Figure 9 Net doping profiles of boron by rapid thermal diffusion

Leakage current density (J_R) is a very important parameter presenting the quality of diode. In Figure 3.3, the differences between diode characteristics for these samples are clearly illustrated. As seen in Table 2, diodes fabricated at 1000°C and 1050°C with junctions depth of 41nm and 71nm respectively show low leakage current densities which are $0.5nA/cm^2$ and $0.3nA/cm^2$. On the other hand, the leakage current increased for diodes fabricated at lower temperatures. From this table, we can see that the deeper the junction depth,

Table 2 Diode parameters fabricated from B150 RTD

T(°C)	900°C	950°C	1000°C	1050°C
Rs(Ω /cm^2)	>>	3900	500	250
Simulated RS(Ω /cm^2)	6080.5	2134.6	654.5	237.2
Xj (nm)	13	28	56	105
Simulated Xj (nm)	18	25	41	71
Diod area (nm^2)	J_R(2.5V) (nA/cm^2)	J_R(2.5V) (nA/cm^2)	J_R(2.5V) (nA/cm^2)	J_R(2.5V) (nA/cm^2)
100 × 100	2.240	1.273	0.581	0.356
200 × 200	2.214	1.197	0.558	0.349
400 × 400	2.197	1.135	0.553	0.327
800 × 800	2.178	1.083	0.546	0.298

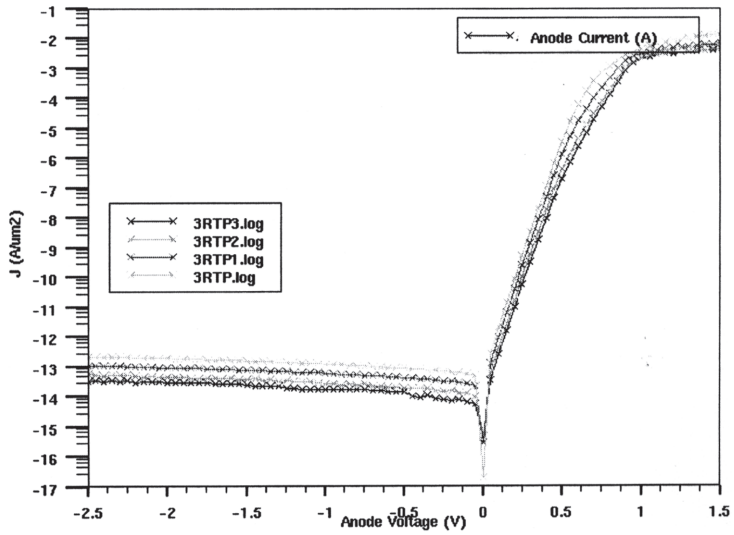

Figure 10 I-V characteristics of PN junction

the lower its current density. The leakage current density is also decreased when the diode area is increased. This is because of the different contributions of the bulk and the peripheral between different areas [6].

The current density shown in the Table 2 was calculated simply by taking the ratio of the total leakage current over the diode area. Actually, the total leakage current I_R can be presented with bulk leakage current density I_B which contributed from the diode bulk area and peripheral leakage current density I_P as shown in the following Equation (1) below and in Figure 11 [6].

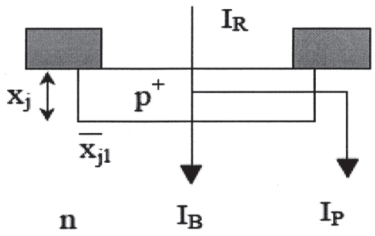

Figure 11 Leakage current model [6]

$$I_R = (I_p L) + (I_B A) \text{ or} \tag{1}$$

$$J_R = I_R/A = (I_p . L/A) + I_B \tag{2}$$

Where L is the diode periphery and A is the diode area.

From the equation, the obtained bulk leakage current densities I_B are about 2nA/cm^2 and less for all samples. The peripheral leakage current densities I_P are decreased when the diode junctions are going deeper at higher diffusion temperatures. This result can be explained by the fact that the lateral junction depth x_{j1} is often about 2/3 of the vertical junction depth x_j [6].

When the junction become too shallow, then the shallower lateral junction will create a higher peripheral leakage current. At the same time, the silicon oxide and silicon interface will also become important and it may increase the peripheral leakage current. The metal/Si interface could increase the leakage current if the depletion layer was too close to this region in the case of very shallow junctions.

In summary, high performance shallow junction have been obtained using RTD of B150 diffusion source into Si. All the junctions which were deeper than 20nm had bulk leakage current densities of about 1nA/cm^2.

3.2 Phosphorus diffusion

Phosphorus diffusion into silicon by using conventional furnace was presented since the quality of the diodes realized by RTD was not reality good. The leakage current density was high for this diffusion. In this simulation, the diffusivity values used were the default values. Diffusivity values of phosphorus in SOD were lower than boron diffusivity values in SOD. In fact, the pre-factor and activation energy for boron diffusivity in silicon are also higher. It will affect diffusion profiles such as junction depth and sheet resistance.

The results of sheet resistance values and junction depths of phosphorus diffusion at various temperatures and times are listed in Table 3. There was difference between simulated profiles and measured profiles for phosphorus diffusion. Figure 12 shows the junction structure of phosphorus by furnace diffusion

Table 3 Sheet resistances and junction depths VS1 temperatures and times

t(mins)	Rs(Ω/cm^2)		Xj(μm)		Rs(Ω/cm^2)		Xj(μm)		Rs(Ω/cm^2)		Xj(μm)	
	4pp	Sim	SRP	Sim	4pp	Sim	SRP	Sim	4pp	Sim	SRP	Sim
15	242.7	202.0	0.60	0.61	13.78	10.25	0.76	0.92	8.38	8.19	1.06	1.45
30	70.55	90.66	0.78	0.67	10.63	7.24	1.12	1.08	4.93	9.10	1.28	1.72
60	23.45	35.94	1.17	0.75	8.39	7.56	1.55	1.23	5.30	9.82	2.04	2.12
120	15.58	14.51	1.55	0.85	8.99	8.21	2.10	1.42	5.21	9.64	2.85	2.71
240	11.97	7.58	2.08	1.00	9.17	9.10	2.44	1.65	3.98	7.93	3.48	3.57

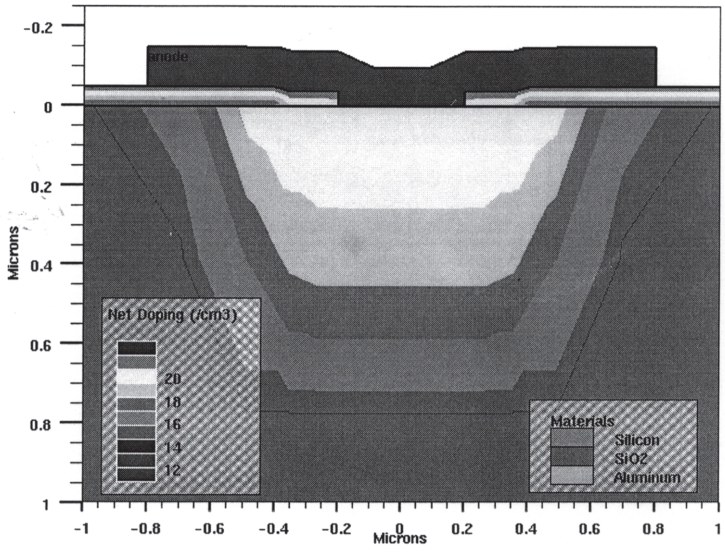

Figure 12 Junction formation of N^+P at 900°C for 30 minutes by furnace diffusion

3.3 Boron diffusion into polysilicon/Si

A polysilicon layer was deposited on top of the Si substrate and then a SOD layer was deposited on top of this layer. At high temperature, dopant atoms

will diffuse into this layer and subsequently into the Si substrate to create a PN junction. This structure has advantages of low series resistance and the diode metal contact is brought far away from the semiconductor PN junction. As a result, the quality of diodes can be improved significantly.

Diffusion of boron into polysilicon on Si structures was investigated using conventional furnace annealing at different temperatures from 800°C-1000°C. Table 4 shows sheet resistance and junction depth of poly-buffered diodes prepared by simulation. As seen in Table 4, there were slightly different between measured sheet resistances and simulated sheet resistances. The reason was there is no suitable model for diffusion in polysilicon in ATHENA software package. In other hand, default model was used. However, the simulation results showed that the resistance for polysilicon layer was lower. The junction depth obtained was also shallower if using polysilicon layer.

Table 4 Sheet resistance and junction depth of poly-buffered diodes

T(°C)	850°C	900°C	950°C	1000°C
Measured Rs(Ω /cm2) (poly/Si)	200	44	31	18
Simulated Rs(Ω /cm2) (poly/Si)	190	67	31	17
Simulasi Xj (nm) (Without polysilicon)	0.041	0.085	0.179	0.352
Simulasi Xj (nm) (Polysilicon layer)	0.035	0.078	0.171	0.341

4.0 CONCLUSIONS

PN junctions with depth less than 50nm were successfully simulated using rapid thermal diffusion. However, these shallow junctions have high sheet resistance characteristics. Leakage current density was also higher when the junction was shallower and the active region of the diode was smaller. For future ULSI technology, shallow junctions with low resistance characteristics are needed. From our simulation, diffusion from polysilicon layer was solved the resistance problem. Junction formation by diffusion from polysilicon layer doped by diffusion from SOD produced shallower junctions with low resistance.

ACKNOWLEDGEMENTS

We would like to thank the staffs of Faculty of Engineering, Universiti Kebangsaan Malaysia and School of Microelectronic Engineering, Universiti Malaysia Perlis (UNIMAP).

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