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A 0.3 mW 2.4 GHZ LOW POWER LOW NOISE AMPLIFIER USING FORWARD BODY BIAS TECHNIQUE FOR WIRELESS SENSOR

Anishaziela Azizan, Sohiful Anuar Zainol Murad*

School of Microlectronic Engineering, Universiti Malaysia Perlis, 01000 Kangar, Perlis, Malaysia

*Corresponding author
sohiful@unimap.edu.my

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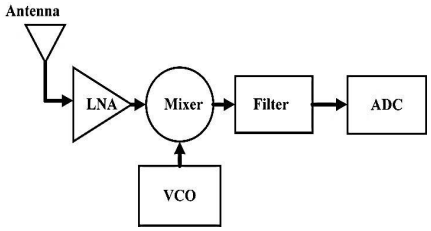
Graphical abstract



Abstract

This paper presents a 0.3 mW 2.4 GHz low-power low-noise amplifier (LNA) using a forward-body bias technique for a wireless sensor network. The proposed LNA is implemented using CMOS 0.13-µm Silterra technology. The forward-body bias technique with a cascode configuration has been adopted in order to obtain low power consumption. A low supply voltage of 0.5 V is used to optimize the trade-offs between the LNA performances. The post-layout simulation results indicate that a power consumption of 0.3 mW is achieved. The simulated input return loss (S11) is less than -17.71 dB while the output return loss (S22) is below -14.83 dB. Moreover, the gain (S21) of 9.86 dB, the noise figure (NF) of 5.11 dB and the input-referred third-order intercept point (IIP3) of -7.5 dBm at 2.4 GHz is obtained with the calculated figure of merit (FOM) of 4.64 (1/mW).

Keywords: Low-noise amplifier, forward-body bias, power consumption, trade-offs, gain, noise figure, figure of merit

Abstrak

Kertas kerja ini membentangkan penguat rendah hingar (LNA) berkuasa rendah 0.3 mW dengan frekuensi 2.4 GHz menggunakan teknik jasad pincang ke depan untuk rangkaian penderia tanpa dawai. LNA yang dicadangkan telah dilaksanakan dengan menggunakan teknologi Silterra 0.13-µm CMOS. Teknik jasad pincang ke depan dengan tatarajah kaskod telah diterima pakai bagi mendapatkan penggunaan kuasa yang rendah. Satu voltan bekalan rendah 0.5 V digunakan untuk mengoptimumkan keseimbangan antara prestasi-prestasi LNA. Keputusan simulasi pasca bentangan menunjukkan bahawa penggunaan kuasa 0.3 mW dicapai. Simulasi kehilangan masukan balik (S11) adalah kurang daripada -17.71 dB manakala kehilangan keluaran balik (S22) adalah di bawah -14.83 dB. Tambahan pula, gandaan (S21) adalah 9.86 dB, angka hingar (NF) adalah 5.11 dB dan tertib titik pintasan ketiga (IIP3) adalah -7.5 dBm pada 2.4 GHz diperolehi dengan merit angka yang dikira (FOM) ialah 4.64 (1/mW).

Kata kunci: Penguat rendah hingar, jasad pincang ke depan, penggunaan kuasa, keseimbangan, gandaan, angka hingar, angka merit

1.0 INTRODUCTION

There is a great demand on wireless sensor networks (WSNs) nowadays due to its functions in the market. A WSN consist of a group of low-cost, low-power, multifunction, small wireless nodes, which work together to collect and process data and communicate wirelessly. WSNs are used in such

applications as remote sensing, monitoring healthcare, security systems, home automation and traffic control [1]. In agriculture, WSNs are used in monitoring environmental parameters like temperature, carbon dioxide (CO2) concentrations, and humidity, intensity of radiation and wind pressure or speed. The basic specifications of a WSN are reliability, accuracy, flexibility, expense, difficulty of development and power consumption. However, due to their being battery powered, power consumption has become one of the most important specifications [2].

In intelligent farming, in order to improve the efficiency and growth in crop yields while improving cultivation by collecting different data, WSNs can be applied. Information and data on weather conditions, the soil environment, monitoring, soil humidity and pH levels can greatly help in improving crop yields while maintaining soil fertility [3]. This paper will focus on studying, analysing and implementing the technique in a block in a radio frequency (RF) front-end design which is a low-noise amplifier (LNA). The LNA is the first block in a receiver part of the RF front-end as shown in Figure 1 [4], [5]. The main objective of this LNA design is to consume less power while maintaining suitable output performances.

This paper consists of LNA theories, in Section 2, followed by the design procedures in Section 3. The LNA circuit design is presented in Section 4. Next, Section 5 presents the simulation results and the conclusions are presented in Section 6.

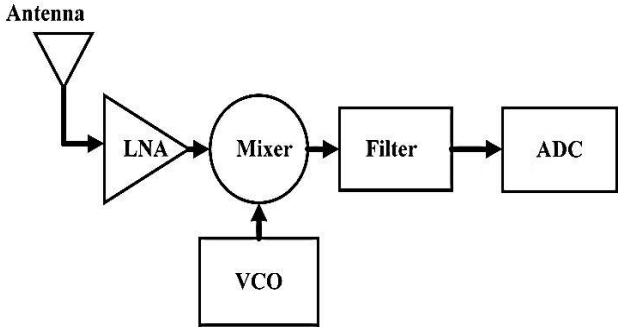


Figure 1 WSN receiver block diagram

2.0 LNA THEORIES

2.1 Gain

The RF amplifier power gain is defined as the difference between the output and the input signal or as a ratio of the output to the input power. The gain represents how well the load of the LNA received signal power compares to the input power. The unit of the power gain is dB.

2.2 Input and Output Matching

Input matching (S11) shows how well the input impedance is matched to the characteristic impedance, which is 50 Ω. Meanwhile, S22 depicts the output impedance matching. The lower that S11 and S22 are, the better the impedance matching that is achieves. This is because S11 and S22 comprise a ratio that describes the input and output signal reflection when the AC signal is treated as a wave. The unit of S11 and S22 is dB. A diagram of a s-parameters representation of a two-port network is shown in Figure 2.

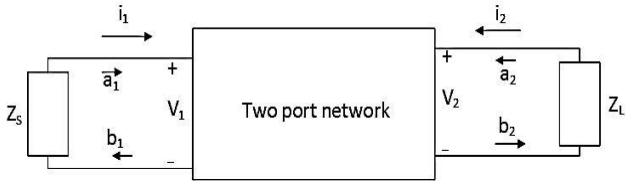


Figure 2 S-parameters representation of a two-port network.

$$S11=\frac{b1}{a1}\Big|_{a_2=0} \quad (1)$$

$$S22=\frac{b1}{a2}\Big|_{a_1=0} \quad (2)$$

2.3 Noise Figure

The noise figure can be defined as the ratio between the input signal-to-noise ratio (SNR*i*) and the output SNR. The value is always greater than 1.

$$NF=\frac{SNRi}{SNRo} \quad (3)$$

Normally, the noise figure is expressed in dB, as follows:

$$NFdB=10\log 10(NF) \quad (4)$$

2.4 1 dB Compression Point

The 1 dB compression point is used to interpret the highest gain in its linear region. It shows the performance of the LNA in terms of linearity. When the power gain is in the linear region, the value of the output power is directly proportional to the input power. When the gain begins to drop but the output power does not increase linearly with the increased input power, this means that power compression occurs. As the power gain drops by 1 dB, it is defined as the 1 dB compression point as shown in Figure 3.

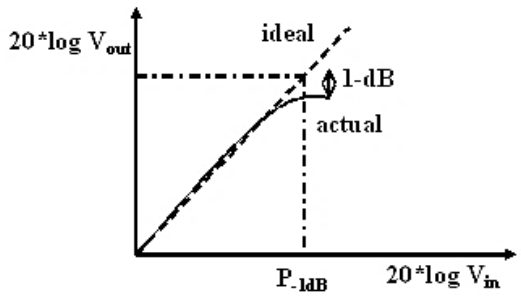


Figure 3 Plot of the 1 dB compression point

2.5 Power Consumption

The supply power consumption is the total power consumed from the power supply to maintain the proper operation of the LNA. The unit for this parameter is either mW or dBm. The power consumption can be calculated based on equation (5):

$$P_{DC} = I_D V_{DD} \tag{5}$$

The drain current I_D is given by:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6}$$

where μ_n is the electron mobility in Si = 1360 cm^2/Vs, Cox is the capacitance per unit gate area of the oxide layer = $\varepsilon_{ox} / t_{ox}$, t_{ox} is the thickness of the oxide layer and ε_{ox} is the dielectric or permittivity of the silicon dioxide.

2.6 Figure of Merit

Different figures of merit (FOMs) are commonly used in the literature in order to evaluate the performance of low-voltage and low-power LNAs. One figure of merit of the LNA is the ratio of the gain in dB to the dc power consumption in mW. The FOM in the table is expressed as below according to the definition in [6]:

$$\text{FOM} = \frac{\text{Gain}_{(abs)}}{(\text{NF} - 1)_{(abs)} \times P_{DC}} (1 / \text{mW}) \tag{7}$$

3.0 DESIGN PROCEDURES

It is very important to have the specifications of the design in order to get a successful LNA design. After setting the specifications by using the Composer Schematic Editor in Cadence, the schematic is designed. Next, the test bench is created so as to simulate the design schematic by using the Cadence Spectre analogue simulation environment.

3.1 Design Specifications

The performance budgeting of the WSN receiver is summarized in Table 1 [7]. In addition, the previous published works are also considered so as to ensure that the result obtained from this research is improved. There are several published LNAs focusing on low power consumption for wireless sensor network applications [6]-[20].

Table 1 Performance budgeting of the LNA

Parameters	Value
Gain (dB)	4-15
NF (dB)	2-10
S11, S22 (dB)	<-15
IIP3 (dBm)	-10 to 0

The range of gain specifications is between 4 and 15 dB targeted to be achieved from this circuit design. A higher gain is better, but the value should be considered also for the current consumed from the simulation, as the objective is to consume the least power. Meanwhile, the NF value must be as low as possible for a better performance due to the reduction of the losses. The input-referred third-order intercept point (IIP3) is set to be within the range of 0 to -10 dB. If the IIP3 is nearer to 0, this is a better performance on the part of the LNA circuit. Broadly, the performance of the LNA is determined by the S-parameters [15]. However, there will be trade-offs between gain, NF and IIP3.

4.0 LNA CIRCUIT DESIGN

Figure 4 shows the schematic design of the proposed LNA. The design is based on the forward body bias technique because the transistors can operate under a low supply voltage, which is one of the effective ways to consume less power [5],[12],[13]. Besides, this technique could be employed with simplicity so as to minimize the size and cost. The gain will decrease when the supply voltage is low. Therefore, the proposed circuit employs a cascode structure consisting of two NMOS transistors. The main elements of this LNA are transistors M1 and M2. Notice that the NMOS transistors have four ports, that is, a gate (G), a drain (D), a source (S) and a body (B). The source of M1 is connected to ground, ensuring that M1 is in a common-source configuration. The gate of M1 is the input port of the signals while the drain of M2 is the output port of the signals. For low power consumption, the body is connected to a positive voltage source which can reduce the threshold voltage (V_{th}) of the NMOS transistors.

In this design, the biasing voltage (VB) is set to 0.3 V, which is much less than 0.7 V, that is, the turn-on voltage of PN junctions. Therefore, the body-source junction of the NMOS transistor in this LNA has a

negligible leakage current. In the circuit shown in Figure 3, the R1 is the biasing resistance at the gate of transistor M1. The inductance L2 is connected to the drain of transistor M2, which can increase the gain. Meanwhile, an appropriate value for C2 is selected by considering gain and center frequency. C1 and C3 are the coupling capacitances.

The function of C1 and L1 is for the input-matching of 50 Ω, and the value is also tuned in order to ensure that the circuit operates at 2.4 GHz. The size of the transistor will determine how low the current is so as to get the lowest power consumption and also to increase the gain and efficiency.

The series LC circuits of C3 and L3 are a part of the output-matching in the design. Both values are tuned to get the desired output-matching at the centre frequency of 2.4 GHz. R2 is a part of the biasing resistor.

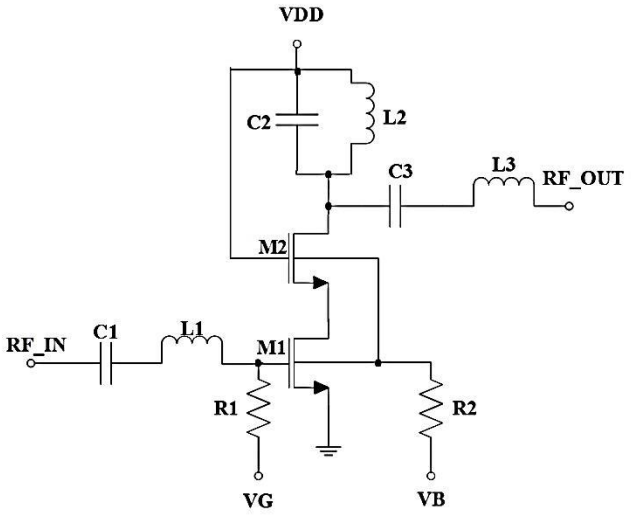


Figure 4 Schematic of the proposed LNA

5.0 SIMULATION RESULTS

Figure 5 depicts the simulation results for input-matching of the circuit. The simulation result shows that the value of input return loss (S11) for pre-layout is -14.27 dB at 2.4 GHz. However, the post-layout of S11 improved to -17.71 dB. This is caused by the parasitic effect such as the input capacitance and the parasitic between the inductor and substrate. Overall, the value of input matching is acceptable and within the expectation range.

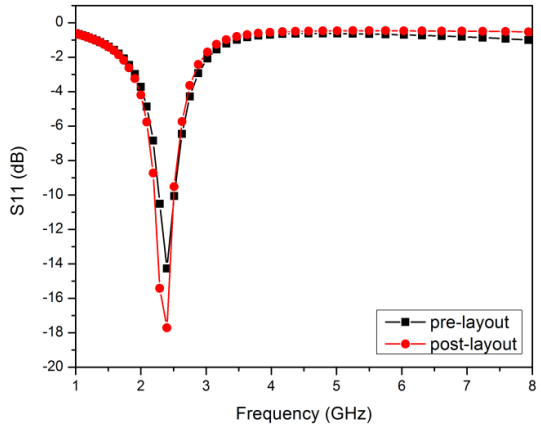


Figure 5 Input return loss (S11)

Figure 6 shows the output return loss (S22) of the proposed LNA. It can be seen that both the pre-layout and the post-layout are a match with each other. The simulated S22 is less than -12.00 dB. There are the differences between the pre-layout and post-layout are due to the parasitic nature of routing, capacitance, inductance and the output pad.

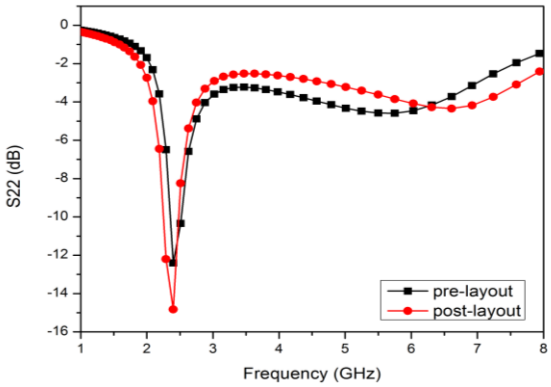


Figure 6 Output return loss (S22)

Figure 7 depicts the voltage gain (S21) of the proposed forward-body bias with cascode configurations of the LNA. According to the simulation results, S21 degrades to 9.86 dB from 12.03 dB. As explained previously for the input- and output-matching, S21 also suffers from parasitic effects. The parasitic resistance in the load inductors could degrade the voltage gain of the circuit.

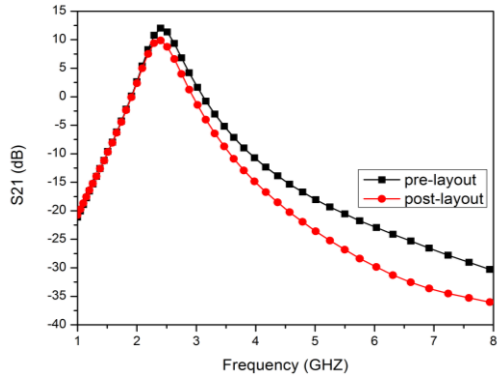


Figure 7 The gain of the proposed LNA

Figure 8 illustrates the pre-layout and post-layout simulation results for the noise figure (NF). As can be seen, there is a difference between the pre-layout and post-layout curves which can be explained by parasitic effects. The NFs of 4.95 dB and 5.11 dB are achieved for the pre-layout and post-layout at 2.4 GHz, respectively. The increase in the NF is due to the parasitic effects of the passive components on the input of the LNA. Moreover, the route from the input pad to the gate inductor and from the inductor to the input transistor can be modelled by a resistor, which could also contribute to the noise. Overall, the NF achieved from this LNA circuit is within the specifications.

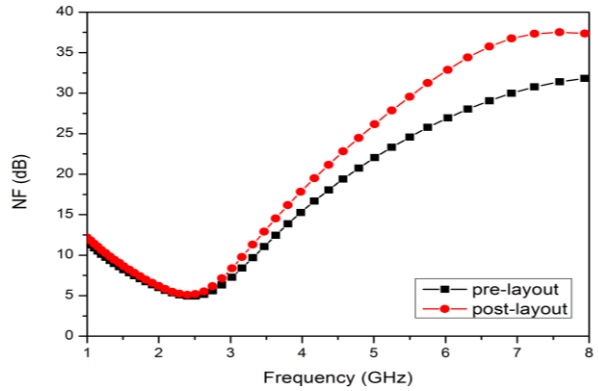


Figure 8 Noise performance of the proposed LNA

The linearity of the proposed LNA is measured by the input 1 dB compression point (IP_{1dB}). As shown in Figure 9, a simulated IP_{1dB} of -18 dB is achieved. Notice that the plot value is typically an acceptable specification and that it is a trade-off between power consumption and linearity requirements.

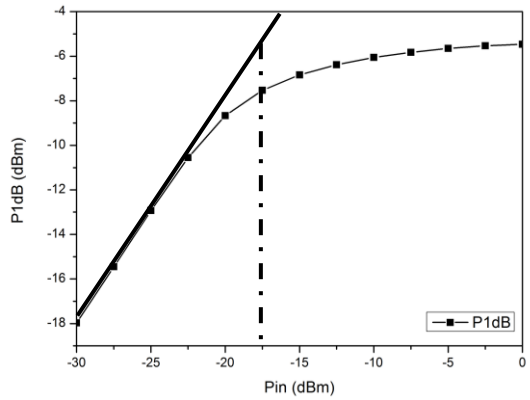


Figure 9 Simulated result of the input 1 dB compression point

A two-tone test for a third-order intercept point (IIP3) is performed on the LNA in order to measure the linearity requirement. The two-tone test is applied at frequencies of 2.4 GHz and 2.48 GHz with equal power. As shown in Figure 10, an IIP3 of -7 dBm is achieved. This value is achieved within the specifications and represents a trade-off between power consumption and linearity requirements. In other words, the design has been optimized to obtain the best IIP3 value with the goal of consuming the least power in the LNA.

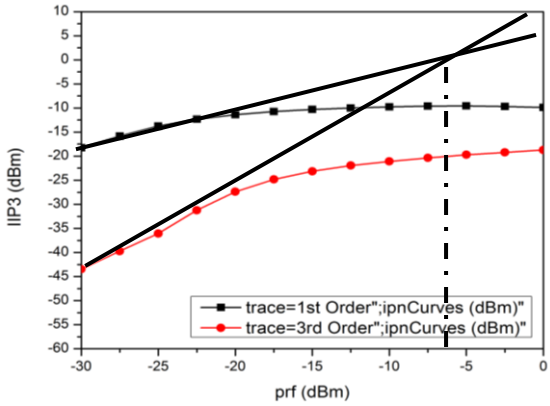


Figure 10 Simulated result of the IIP3

The plot of the stability factor is shown in Figure 11. The LNA is unconditionally stable, whereby the stability for pre-layout and post-layout is greater than 1.

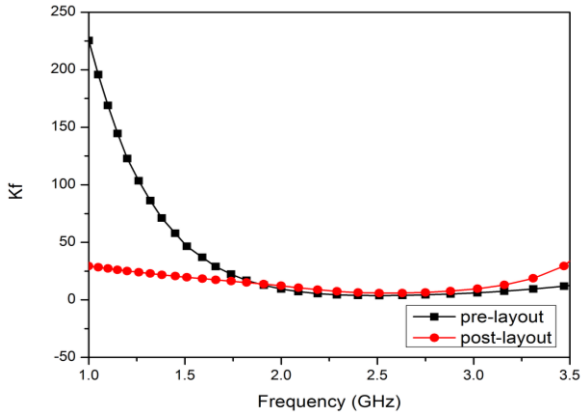


Figure 11 Stability of the proposed LNA

Table 2 summarizes the performance of the recently published LNAs for WSNs. Compared with other works; the proposed LNA exhibits the least power consumption and excellent linearity. The results show that the proposed LNA is suitable for WSN applications.

The layout of the proposed LNA is presented in Figure 12. The die area including the pads is 1.02 mm x 0.93 mm; this layout will be taped out in the future.

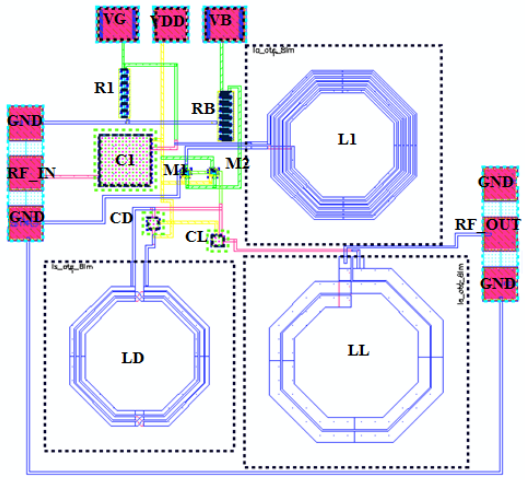


Figure 12 Layout of the proposed LNA (0.93 mm x 1.02 mm)

Table 2 Performances comparison of recently published LNAs for WSNs

References	[16]	[17]	[18]	[19]*	[20]*	This Work
CMOS Technology (µm)	0.12	0.18	0.18	0.2	0.18	0.13
Supply Voltage (V)	1.0	1.8	1.8	1.0	1.8	0.5
Frequency (GHz))	2.4	2.4	2.4	2.0	2.4	2.4
Gain (dB)	20	14.12	16.8	25.67	14.7	9.86
S11, S22 (dB)	N/A	-11, -18	-13, -15	-14.6, -13.3	-18, N/A	-18, -15
NF (dB)	3.9	1.59	3.6	4.0	4.8	5.11
P_{1dB} (dBm)	N/A	-8	-20	N/A	-15	-18
IIP3 (dBm)	N/A	1	-10	N/A	2	-7.5
Power (mW)	22.6	7.2	2.16	5.13	0.58	0.3
FOM (1/mW)	0.30	1.60	2.48	2.48	4.64	4.64
Chip Size (mm^2)	0.018	282	496	N/A	0.39	0.95

*Pre-layout simulation results.

6.0 CONCLUSION

A forward-body bias technique with a cascode configuration LNA for WSNs has been designed and simulated using CMOS 0.13-µm Silterra technology. All the circuit components, including the input- and output-matching, have been designed on-chip. The forward-body bias technique allows for the reduction of the threshold voltage and thus reduces the power consumption. The post-layout simulation results show that a power consumption of 0.3 mW is achieved for a 0.5 V power supply with other parameters are acceptable. Moreover, the FOM of the proposed LNA is among the highest as compared with previously-published works. Based on the performances of the LNA, the design is suitable for WSN applications.

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