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DIGITAL FRONT-END FOR WIDEBAND ANALOG FRONT-END IN A MULTI-STANDARD SOFTWARE DEFINED RADIO RECEIVER

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Abstract. Software defined radio (SDR) is a concept that has been gaining momentum in realizing a wireless multi-mode, multi-band, and multi-standard radio terminal, capable of operating according to a variety of different mobile communication standards. This paper investigates a number of architectural issues and trade-offs involved in the consideration of receiver analog front-end for a multi-standard SDR with a fundamental objective of expanding the digital signal processing (DSP) towards the antenna. The most suitable analog front-end architecture is considered to design digital front-end and the implementation is done in a SDR terminal. The simulation undertaken demonstrated that GSM and DECT standards specifications are met by a multiplier less digital quadrature downconversion and multirate filtering composed of a 5^{th} order comb filter, an inverse sinc filter and a generic FIR filter. A fixed point architectural design was defined and an efficient implementation in usage of FPGA hardware resource and the results are presented.

Keywords: Analog to digital conversion, FIR filters, sigma delta modulator, quadrature down-conversion, multirate filtering

Abstrak. Perisian tertakrif radio merupakan suatu konsep yang sedang memperoleh momentum bagi merealisasikan terminal radio wayarles berbilang mod, berbilang jalur dan berbilang piawai supaya dapat beroperasi mengikut pelbagai piawai komunikasi mudah alih yang berbeza. Kertas kerja ini menyelidik beberapa isu seni bina dalam mempertimbangkan hujung hadapan penerima beranalog bagi perisian tertakrif radio yang beroperasi untuk pelbagai piawai dengan objektif utama agar pemprosesan isyarat digit dikembangkan ke arah antena. Arkitektur hujung hadapan beranalog yang paling sesuai dipertimbangkan untuk mereka bentuk hujung hadapan berdigit dan implementasi dilakukan menggunakan terminal perisian tertakrif radio. Simulasi yang dilakukan menunjukkan spesifikasi piawai GSM dan DECT dicapai menerusi penukar rendahan kuadratur berdigit dan penapisan berbilang kadar yang diwakili oleh penapis bersisir tertib lima, penapis FIR sinc songsang dan penuras FIR umum. Suatu arkitektur reka bentuk titik tetap ditakrifkan dan implementasi yang efisien dalam mengurangkan penggunaan sumber perkakasan FPGA serta keputusannya dilaporkan.

Kata kunci: Penukaran analog ke digit, penapis FIR, pemodulat sigma delta, penukaran rendahan kuad, penapis berbilang kadar.

1.0 INTRODUCTION

SDR is an emerging technology, thought to realize flexible radio systems, multi-service, multi-standard, re-configurable and re-programmable by software [1]. A goal in SDR

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is to push the digitization point as close as possible to the antenna using wideband analog-to-digital converter (ADC) [1]. An ideal architecture of a software radio receiver with minimum analog components in analog front-end (AFE) is shown in Figure 1 [2]. The only analog components are the antenna, the bandpass filter, and the low noise amplifier (LNA). ADC is immediately done at radio frequency (RF) in order to digitally elaborate the signal on a completely re-programmable board. The flexibility of the SDR terminal to adapt to different types of signals by having different symbol rates is made possible by using re-configurable and re-programmable hardware such as Field Programmable Gate Array (FPGA). More radio functions, can be written in software and embedded in programmable logic.

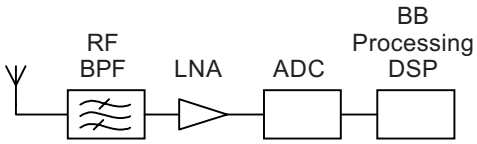


Figure 1 The ideal software radio receiver

However, at the moment, this ideal receiver is far from achievable since it is not reasonable to use a single RF stage for a multi-band system, due to the impossibility of building antennas and LNAs on a bandwidth ranging from hundreds of megahertz to units or tens of gigahertz. ADC performance is still not sufficient enough to perform digitization at RF. Particularly, the analog input bandwidth, sampling rate, dynamic range, and therefore, resolution, need considerable amounts of improvement if wideband front-end and sampling at RF are to become a reality. The ability to process signals corresponding to a wide range of frequency bands and channel bandwidths is a critical feature of multi-standard radios and impacts heavily on the design of both analog and digital segments of the receiver.

Digital front-end (DFE) is a term introduced in [2]. Digital front-end is a hardware platform digitally realizing front-end functionalities that were formerly realized by analog signal processing. The digital front-end functionalities are channelization and sample rate conversion. Channelization is a functionality comprising all necessary tasks to extract a single user channel for further processing at baseband thus involving, downconversion, filtering, and possibly dispreading. Sample rate conversion is a part of digital signal processing to process signals at different sample or symbol rate in order to cope with signals of different mobile standard.

The work presented in this paper discusses a short overview of different analog front-ends and suggests a suitable architecture for realizing digital front-end. The digital front-end is designed and implemented in an FPGA to meet the GSM and DECT standard specifications for multi-standard SDR receiver. Section 2.0 reviews receiver architectures, including heterodyne, direct conversion, low intermediate frequency

(IF), wideband IF double conversion, bandpass sampling, and wideband IF subsampling techniques. Section 3.0 explains the methodology and simulation results of the digital front-end approach using the suggested suitable analog front-end architecture, with respect to the fundamental idea of expanding DSP toward the antenna, and section 4.0 elaborates the design implementation in FPGA, including simulation results for each standard. Section 5.0 summarizes and concludes the work presented in this paper.

2.0 ANALOG FRONT-END ARCHITECTURE

Many issues are involved when attempting to consider a suitable architecture for analog front-end in SDR terminal. To understand some of the barriers in different types of receiver architectures, a review is given and analyzed. It is assumed that there are no distortions due to the channel. Thus, the received signal, $x_{Rx}(t)$, equals to the transmitted ones, $x_{Tx}(t)$.

$$\underline{x}_{Rx}(t) = \underline{x}_{Tx}(t) \tag{1}$$

$$= \mathrm{Re}\left\{\underline{x}_{Tx,BB}(t)e^{j2\pi fct}\right\} \tag{2}$$

$$= \frac{1}{2}\left(\underline{x}_{Tx,BB}(t)e^{j2\pi fct} + \underline{x}^{*}_{Tx,BB}(t)e^{-j2\pi fct}\right) \tag{3}$$

where $\underline{x}_{Tx,BB}(t)$ is the complex baseband signal to be transmitted, fc is the carrier frequency and $\underline{x}^{*}$ denotes the conjugate of $\underline{x}$. Equation (3) suggests that the received signal comprises of two components, one is centered at fc and the other is at $-fc$.

2.1 Superheterodyne Receiver

The superheterodyne receiver is a traditional receiver architecture, and the one most often used due to its high selectivity and sensitivity [3]. The heterodyne receiver is depicted in Figure 2 [4]. At first, the RF band is selected and the out-of band signals are attenuated using a passive band selection filter. The signal is amplified by means of a LNA and the image signal is filtered with a passive bandpass filter. First, the signal band is translated down to some IF which is usually much lower than the initially received frequency band using a local oscillator (LO) as in equations (4) and (5). This relaxes the requirements for the channel selection filter.

$$\underline{x}_{Rx,IF}(t) = \underline{x}_{Rx}(t)e^{-j2\pi f_{LO1}t} \tag{4}$$

$$= \frac{1}{2}\left(\underline{x}_{Tx,BB}(t)e^{j2\pi(fc-f_{LO1})t} + \underline{x}^{*}_{Tx,BB}(t)e^{-j2\pi(fc+f_{LO1})t}\right) \tag{5}$$

The result is a sum of band of interest centered at $f_{IF} = fc\text{-}f_{LO1}$ and a second signal component which lies $2fc$ apart from the frequency band of interest. As the first mixer downconverts frequency bands symmetrically located above and below LO frequency, to the same center frequency, an image-reject filter in front of the mixer is needed. In a dual IF topology, the resulting signal is subsequently downconverted again to baseband and the last down-conversion generates real/in-phase (I) and imaginary/quadrature (Q) components of the signal as in equations (6)-(9). The I and Q channels are necessary in typical phase and frequency modulated signals because the two sidebands of RF spectrum contain different information and result in irreversible corruption if they overlap each other without being separated into two phases.

$$Re\left\{\underline{x}_{\mathrm{Rx,BB}}(t)\right\} = Re\left\{\underline{x}_{\mathrm{Rx,IF}}(t)e^{-j2\pi f_{LO2}t}\right\} \tag{6}$$

$$= \underline{x}_{\mathrm{Rx,IF}}(t)\cos(2\pi f_{LO2}t) \tag{7}$$

$$Im\left\{\underline{x}_{\mathrm{Rx,BB}}(t)\right\} = Im\left\{\underline{x}_{\mathrm{Rx,IF}}(t)e^{-j2\pi f_{LO2}t}\right\} \tag{8}$$

$$= -\underline{x}_{\mathrm{Rx,IF}}(t)\sin(2\pi f_{LO2}t) \tag{9}$$

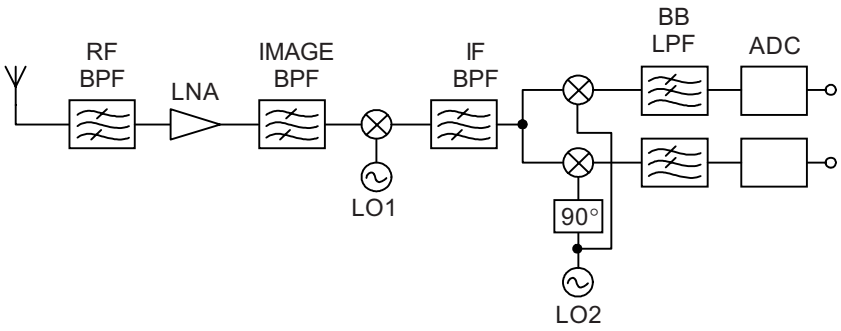


Figure 2 Superheterodyne architecture

The adaptability to many different receiver requirements is a major advantage of the heterodyne receiver. The effect of DC offsets of the first few stages is removed by bandpass filtering, and that of the last stage is suppressed by the total gain in the proceeding stages. In addition, I/Q mismatches occur at much lower frequencies and therefore, are easier to control and correct [5]. As for the LO leakage, since the first mixer LO frequency is out of the band of interest, it is suppressed by the front-end bandpass filter and its radiation from the antenna is less objectionable.

However, the need for a large number of external components and the complexity of the structure resulted in problems if a high level of integration is necessary. This is also the major drawback from the cost point of view. Furthermore, amplification at a

high IF frequency can cause high power consumption. Even though this architecture is widely used now, it is difficult to change system parameters such as bandwidth because RF and IF signals are processed by fixed narrowband analog components.

2.2 Direct Conversion Receiver

Direct conversion is an alternative wireless receiver architecture to well established superheterodyne, particularly for highly integrated, low power terminal [3]. In a direct conversion, also called zero-IF or homodyne conversion [6], the incoming RF signal is downconverted to baseband (zero IF) in one step by mixing with an oscillator output of the same frequency, where $f_{LO}=f$c. A direct conversion receiver is shown in Figure 3 [7]. The RF band is selected by an external passive filter and the signal is amplified by an LNA, as in the superheterodyne architecture. The signal is then mixed directly to DC by a RF mixer, hence, the rest of the passive filters and mixing stages are unnecessary. The resulting baseband signal is then filtered by analog baseband lowpass filters to select the desired channel before the ADC. The direct conversion can be real or complex. While the first is more expensive with respect to the mixer, it circumvents filters that would be necessary for the suppression of RF images in the second case [1]. The second case is represented in equations (10) to (13).

$$Re\{\underline{x}_{\mathrm{Rx,BB}}(t)\} = Re\{\underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO}t}\} \tag{10}$$

$$= \underline{x}_{\mathrm{Rx}}(t)\cos(2\pi f_{LO}t) \tag{11}$$

$$Im\{\underline{x}_{\mathrm{Rx,BB}}(t)\} = Im\{\underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO}t}\} \tag{12}$$

$$= -\underline{x}_{\mathrm{Rx}}(t)\sin(2\pi f_{LO}t) \tag{13}$$

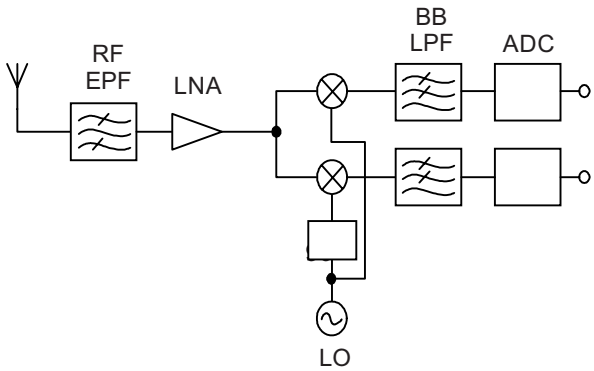


Figure 3 Direct conversion architecture

The main advantage of a direct conversion receiver is that it does not suffer the image problem as the incoming RF signal is downconverted directly to baseband

without any IF stage. Another advantage of the direct conversion architecture is its simplicity. Since it does not require any high frequency bandpass filter, which is usually implemented off-chip in a super-heterodyne receiver for appropriate selectivity, the direct conversion architecture requires less number of external components. However, there are a number of issues in the implementation of the direct conversion receiver. The major disadvantage is that severe DC offsets can be generated at the output of the mixer when the leakage from the LO is mixed with the LO signal itself. This could saturate the following stages and affect the signal detection process leading to I/Q mismatch and even-order distortion [6]. Besides, since the mixer output is a baseband signal, it can easily be corrupted by a large flicker noise of the mixer, especially when the incoming RF signal is weak. As a result, homodyne receivers are extremely difficult to implement.

2.3 Low-IF Receiver

The low IF receiver architecture combines the advantages of heterodyne receivers and direct conversion receivers. Figure 4 shows receiver architecture with low IF topology [8]. The RF front-end of the low-IF receiver [9] is similar to the direct conversion in Figure 3. The difference is that the RF signal is downconverted using quadrature RF downconversion to an IF of around a few hundred kilo-hertz up to several mega-hertz, depending on the channel spacing, instead of the DC frequency as in equations (14) to (17).

$$Re\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\} = Re\left\{\underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO}t}\right\} \tag{14}$$

$$= \underline{x}_{\mathrm{Rx}}(t)\cos(2\pi f_{LO}t) \tag{15}$$

$$Im\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\} = Im\left\{\underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO}t}\right\} \tag{16}$$

$$= \underline{x}_{\mathrm{Rx}}(t)\cos(2\pi f_{LO}t) \tag{17}$$

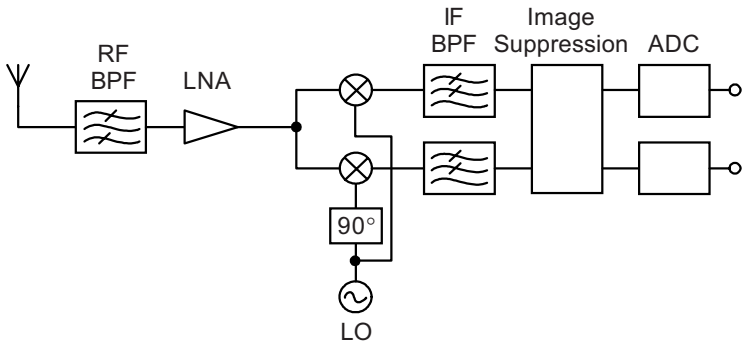


Figure 4 Low IF architecture

In contrast to direct conversion receiver, the channel select filter must be a bandpass filter. As a non zero IF is used, the image frequency problem cannot be avoided. A complex signal processing is then needed to suppress the image components. The most common techniques to remove the image in low-IF receivers are to use image rejection architectures or polyphase filters [10]. After ADC, the signal is digitally downconverted to baseband before digital filtering.

Since the wanted signal is not situated around DC, there is absolutely no DC problems such as DC offset, flicker noise, and LO self mixing in low IF receiver [11]. At the same time, high level integration can be achieved. However, the main disadvantage is that the image signal suppression required is larger. In direct conversion receiver, the mirror signal is the wanted signal itself, while in the low-IF case, it may be larger than the wanted signal. In addition, this receiver architecture has higher demand for I/Q balance or more complicated analog part. I/Q imbalances cause interference that cannot be removed in later stages and so directly decrease the image-reject capabilities of the front-end [9].

2.4 Wideband IF Double Conversion Receiver

An alternative architecture well suited for integration of the entire receiver is wide-band IF with double conversion [8]. In a wide-band IF double conversion receiver architecture as shown in Figure 5 [12], signal down-conversion is performed in multiple phases, as in the superheterodyne receiver, but the discrete image and IF filters are avoided. This receiver system takes all of the potential channels and frequency in a wide signal band, translates them from RF to an IF using a first stage mixer with a single frequency LO (equations (18) to (21)).

$$Re\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\} = Re\left\{\underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO1}t}\right\} \tag{18}$$

$$= \underline{x}_{\mathrm{Rx}}(t)\cos(2\pi f_{LO1}t) \tag{19}$$

$$Im\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\} = Im\left\{\underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO1}t}\right\} \tag{20}$$

$$= -\underline{x}_{\mathrm{Rx}}(t)\sin(2\pi f_{LO1}t) \tag{21}$$

Then, the high frequency components are filtered using a simple lowpass filter, allowing all channels to pass to the second stage of mixers. The second mixer stage, where $f_{\mathrm{LO2}}=f_{\mathrm{IF}}$, is tunable to perform the channel selection and furthermore, it is a quadrature type to accomplish the image rejection. Equations (22) and (23) represent downconversion in the second stage. All of the channels at IF are frequency translated directly to baseband and channel filtering is performed at the baseband.

$$Re\left\{\underline{x}_{\mathrm{Rx,BB}}(t)\right\} = Re\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\}\cos(2\pi f_{LO2}t) + Im\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\}\sin(2\pi f_{LO2}t) \tag{22}$$

$$Im\left\{\underline{x}_{\mathrm{Rx,BB}}(t)\right\} = Im\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\}\cos(2\pi f_{LO2}t) - \mathrm{Re}\left\{\underline{x}_{\mathrm{Rx,IF}}(t)\right\}\sin(2\pi f_{LO2}t) \tag{23}$$

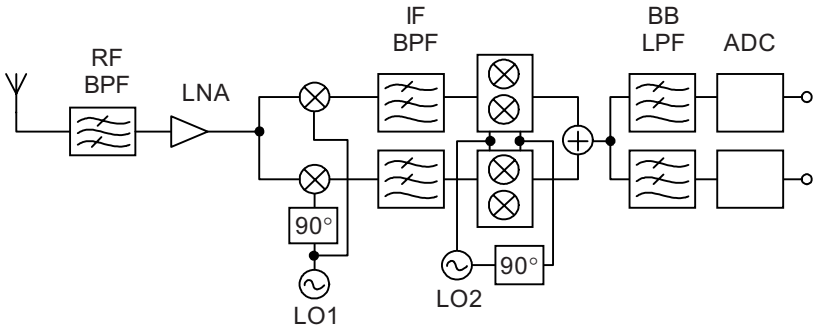


Figure 5 Wideband IF double conversion architecture

The most important advantage is the fact that neither of the LOs is at the RF frequency, reducing the risk of LO mixing, which degrades the overall receivers dynamic range. In addition, this architecture achieves image rejection without a passive phase shifting filter in the signal path. However, the additional mixers make it difficult to achieve a low power, low noise figure, and low distortion receiver. The image rejection mixer requires highly accurate phase and gain matching between the quadrature LOs and the signal path.

2.5 Bandpass Sampling Receiver

Bandpass sampling offers an attractive alternative solution. It is a special form of undersampling [13]. The ideal goal of an SDR approach is to move the ADC as close as possible to the antenna, minimizing the number of required front-end components. The minimal set would contain the antenna, amplifier for the necessary gain towards the ADC, bandlimiting filters, and the ADC (Figure 1). The sampled RF signal generated by the ADC, operating at a rate slightly higher than twice the highest frequency would be fed to the signal processors, in order to extract the channels among the available ones.

However, this approach requires a huge amount of computational power, particularly if the RF frequencies are of some gigahertz. Bandpass sampling, instead, intentionally aliases (undersamples) the signal, thus reducing the resulting processing rate and at the same time can still successfully recover the information bandwidth by adopting a sampling rate matched to its bandwidth. This process converts the information RF band down to a very low IF without any LO mixing and image filtering. First, the signal entering the antenna passes through a narrow bandpass filter centered on the carrier frequency and matched to the size of the information band. Next, the signal is processed by a LNA. The amplified signal is then sampled using ADC. After sampling, the analog information bandwidth is folded into the resulting sampled bandwidth. To make sure that spectrum overlap does not occur, the bandpass sampling frequency, fs, must satisfy:

$$\frac{2f_h}{k} \le f\mathrm{s} \le \frac{2f_l}{(k-1)} \tag{24}$$

where, f_h and f_l are high and low frequency of the bandpass bandwidth respectively, and k is restricted to integer values that satisfy:

$$2 \le k \le \frac{f_l}{(f_h - f_l)} \tag{25}$$

and $(f_\mathrm{h} - f_\mathrm{l}) = f_\mathrm{l}$. Using this equation, the sampling frequency of ADC can be selected.

The major advantages of bandpass sampling are the sampling frequency and processing rate are proportional to the information bandwidth, rather than the carrier frequency. A bandpass sampling ADC works like a mixer and also ADC. Therefore, there is no need for a mixer, thus, reduces design complexity. However, the input bandwidth of the ADC must include RF carrier and this requires a huge amount of computational power. Another drawback is the filter at RF must have a steep roll-off, because it must attenuate the energy outside the information bandwidth. The filter at RF must have a programmable center frequency and this basically represents the major disadvantage of the technique.

2.6 Wideband IF Subsampling Receiver

Wideband IF subsampling architecture performs transformation of analog RF signal to digital IF signal. The subsampling approach can be thought of as generating a signal replica at much lower IF frequency close to DC. The analog segment consists of superheterodyne section where the received signal undergoes two stages of down-conversion to a low intermediate frequency of IF2 as in equations (26) and (27). The first stage downconversion is similar to equations (4) and (5). The signal is subsequently sub-sampled and digitized at IF, extending the boundary of the digital domain one stage closer to the antenna.

$$\underline{x}_{\mathrm{Rx,IF2}}(t) = \underline{x}_{\mathrm{Rx}}(t)e^{-j2\pi f_{LO2}t} \tag{26}$$

$$= \frac{1}{2}(\underline{x}_{\mathrm{Tx,BB}}(t)e^{j2\pi(f_{IF1}-f_{LO1})t} + \underline{x}^{*}_{\mathrm{Tx,BB}}(t)e^{-j2\pi(f_{IF1}+f_{LO2})t} \tag{27}$$

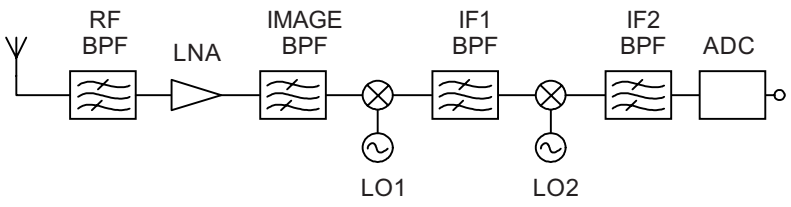


Figure 5 Wideband IF subsampling architecture

The digitization can be performed as Full Band or Partial Band Digitization (Figure 6) [1,14]. While in the case of Full Band Digitization, the whole bandwidth comprising all services to be supported is digitized. In Partial Band Digitization, just a part of the whole bandwidth (e.g. equivalent to the largest channel bandwidth of all services to be supported) is digitized. Since the whole bandwidth to be supported can easily extend to some 100 MHz, while the dynamic range mobile communications standards may be well above 100 dB, Full Band Digitization does not seem to be feasible, not even in the near future. Therefore, Partial Band Digitization is the most promising candidate for SDR terminals.

Wideband IF subsampling requires dual stage IF down-conversion of RF signal to a fixed IF. For a multi-standard terminal capable of processing standards like GSM and DECT, the entire frequency band present at the RF filter is about over 1000 MHz wide spanning from 890 to 1900 MHz. The RF filter rejects the image frequencies of the first mixer. The transition bandwidth of the RF filter can be made broad if *IF*1 is chosen to be sufficiently large, at least a couple of hundred MHz. On the other hand, with regard to subsequent sampling, *IF*1 should not be chosen too high. The bandpass and anti-alias filters at *IF*1 and *IF*2, respectively, are designed for Partial Band Digitization bandwidth, B_a, of each standard. Passband B_a of the analog front-end needs to be sufficiently large to accommodate the air-interface with the widest channel bandwidth (B_a = 1.6 MHz for GSM and B_a = 20 MHz for DECT). Since signal sampling is done at *IF*2, the required *IF*2 is determined by the Nyquist bandwidth to maintain

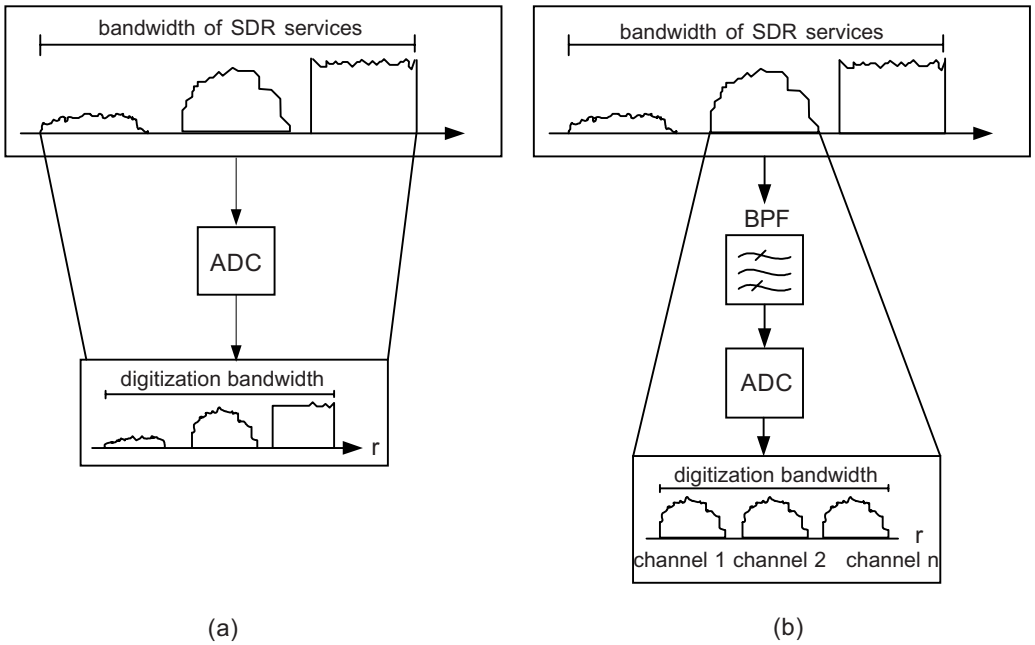


Figure 6 (a) Full band digitization (b) Partial band digitization

faultless sampling. The following relationship between the sampling frequency and the final intermediate frequency *IF*2 holds:

$$fs = \frac{4}{2D-1} IF2 \qquad D = 1,2,3.... \tag{28}$$

The *IF*2 signal subsampling is performed in the 2nd Nyquist zone, D=2, and applied to ensure suitable conditions for the digital signal processing in the baseband signal, giving fs=4*IF*2/3. Either of the images centered on fs/4 or 3fs/4 may be downconverted to baseband. However, for even values of D, an additional spectrum reversal is necessary for the down-conversion of the former image, while no such operation is needed for the latter image. As a result, it is more convenient to downconvert the image centered around 3fs/4 since quadrature digital down-conversion for this centre frequency can be achieved efficiently. This signal is later going to be processed digitally to shift and center it at DC. Digital quadrature down-conversion to baseband eliminates some of traditional drawbacks associated with I/Q mismatch [12].

A high fs relaxes the required steepness of the analog bandpass and anti aliasing filter frequency responses, but places additional demands on the ADC and the subsequent DSP. This important trade-off between the analog and digital domains needs to be carefully considered, particularly with respect to the expected radio channel conditions and the typical levels of interferers and blockers. The choice of *IF*1 is more or less independent of *IF*2 and can be optimized with respect to implementation of

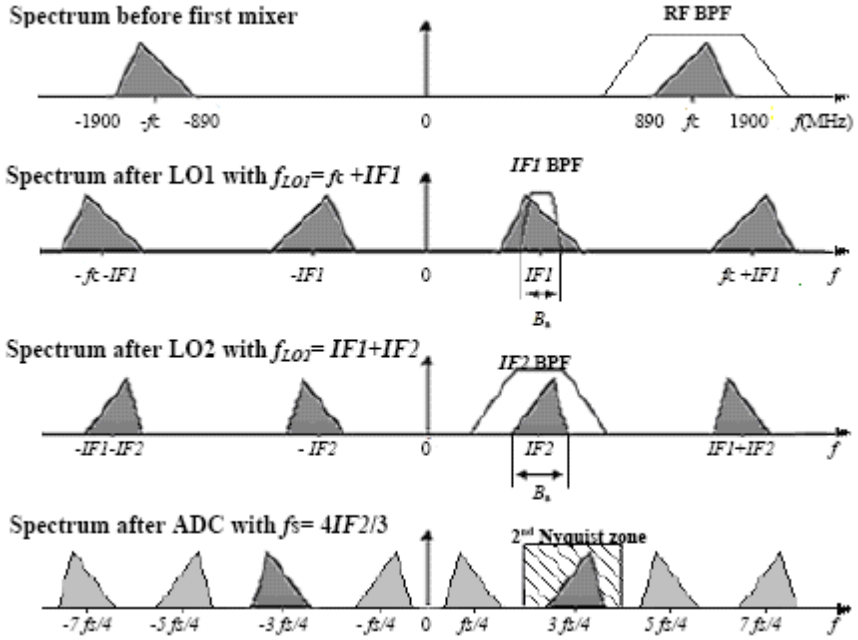


Figure 7 Spectral representation of signals in wideband IF subsampling architecture

the bandpass filter. In addition to alleviating the dynamic range problems of the ADC, this approach would allow a reduction in the sampling rate, fs, in accordance to the channel bandwidth of the target standard, hence achieving significant savings in power consumption. A drawback of this architecture is that two analog filters with demanding requirements, and two analog mixers contributing to intermodulation distortions are required. Furthermore, fs and $IF2$ are related according to the subsampling equation.

3.0 DIGITAL FRONT-END STRUCTURE AND DESIGN

The principal of digital front-end approach is shown in Figure 8. The digital front-end is designed based on the wideband fixed IF subsampling architecture (Figure 5) because it eliminates the intrinsic disadvantages of the other architectures, such as dynamic offset, RF leakage, and image rejection. This architecture also fulfills the SDR requirement by pushing the digitization point one step closer to the antenna, performing sampling at IF. In addition, the fixed frequency LO can be integrated much easier than a tunable LO oscillator used in other architectures.

3.1 Quadrature Downconversion

Signal processing is almost always simpler and thus more efficiently performed at baseband. Thus, the digitized IF signal needs to be down converted to baseband before further DSP. Downconversion to baseband is a process of channelization with one main advantage compared to analog downconversion, which is the perfect I-Q matching and thus, image rejection can be realized. As a result of sampling using equation (28), downconversion can be done efficiently and more conveniently for

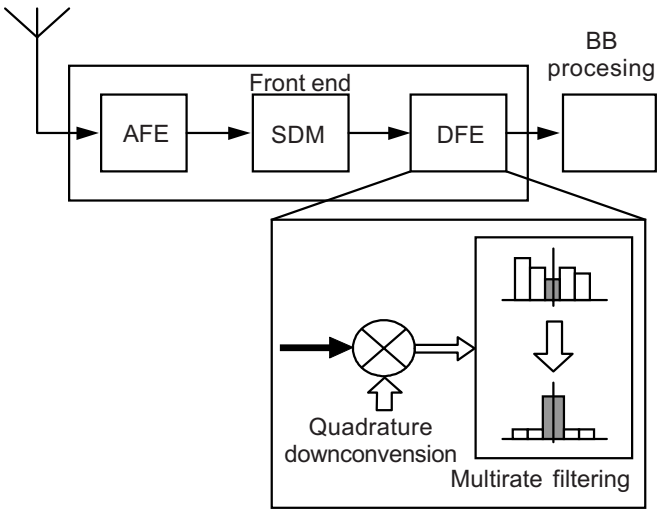


Figure 8 Digital front-end approach

signal centered around 3*f*s/4 to obtain in phase (I) and quadrature (Q) components by multiplying the sub-sampled IF signal with periodic bit sequences at *f*s, representing cosine and sine carriers.

3.2 Multirate Filtering

Multirate filtering was designed to reduce the number of computation needed to convert a wideband signal with high sampling rate to a single channel with reduced sampling rate. Instead of going instantly from the initial sampling rate to the final one, which can be very computationally expensive, the rate conversion is accomplished by dividing the process into several steps (block sets), with each step producing a different sampling rate from the initial one. The process is resumed until the intended sampling rate and channel bandwidth are achieved.

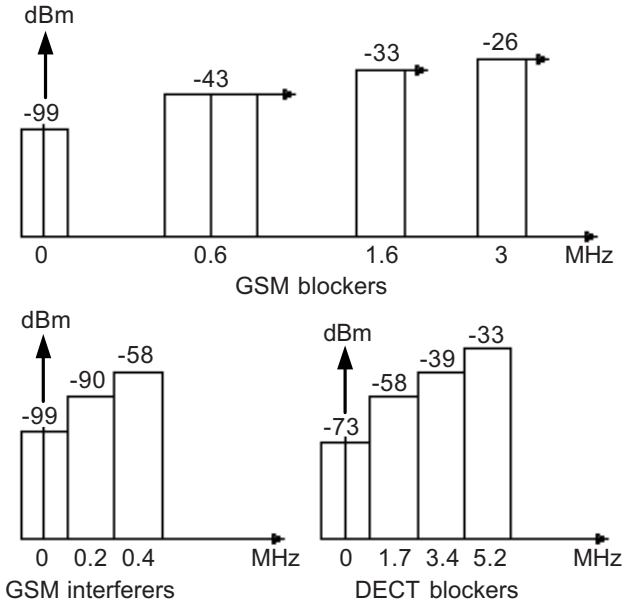


Figure 9 GSM and DECT blockers and interferers specifications

Table 1 GSM and DECT standard specifications

	CNR (dB)	IF2 (MHz)	OSR	Symbol rate	Channel bandwidth	Peak to peak channel ripple
GSM	9	13	64	270.833KSPS	100 kHz	0.1 dB
DECT	10.3	55.296	32	1.152MSPS	700 kHz	0.5 dB

Multirate filtering applies channelization functionality to select the channel of interest and sample rate conversion functionality is applied to reduce the OSR to match the symbol rate of the standard. Cascaded filters are designed to meet the carrier to noise ratio (CNR) requirement for the worst case blocking profile and adjacent channel interferers for GSM and DECT standards, as shown in Figure 9 [15].

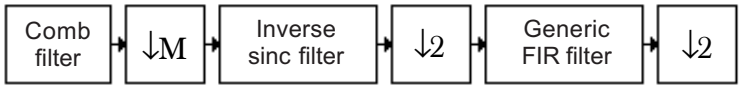


Figure 10 Multirate filters structure

Comb filter is a very interesting first stage filter since it needs no multiplier. The comb filter is known to be an efficient way to down sample the output signal to four times the Nyquist rate [23]. This work is based on multiple of the standards symbol rate, so the comb filter is designed to give output with four times the final symbol rate. Since a bandpass sigma delta modulator with order L=4 is considered, a cascade of N=5 (N=L+1) comb filter is necessary. Hence, a 5th order comb filter with differential delay of one and decimation ratio M=16 was designed for the GSM standard as in equation (29). For DECT, 5th order comb filter with differential delay of two and decimation ratio M=8 was designed. Higher differential delay is used for DECT to achieve higher attenuation since decimation, M, is low.

$$H(z) = \left[\frac{\sin \pi f}{\sin \pi \frac{f}{M}} \right]^N \tag{29}$$

However, the drawbacks of this filter are insufficient attenuation in stopband and distortion in passband. The stopband insufficient attenuation can be overcome by the attenuation in the follow up filters. To solve the inband attenuation problem, an inverse sinc filter is applied in the second stage of filtering to correct the droop caused by the comb filter. The inverse sinc filter has a cubic response of the form:

$$H(z) = \left[\frac{\pi f}{\sin \pi f} \right]^N \tag{30}$$

This filter compensates the attenuation caused by the comb filter in the inband signal so that this band will be free from distortion. By referring to CNR requirement for the worst case blocking profile and adjacent channel interferers, the second stage filter is designed by considering the out of band noise centered at the frequency of decimate by two, which follows the inverse sinc filter. This is because the Nyquist bandwidth surrounding this frequency will alias into the inband signal after decimation occurs. The filter is designed to attenuate out of band noise centered at the decimated frequency to a value below inband signal level by CNR of each standard.

Passband frequency of the inband signal is chosen equal to 82% of channel bandwidth, resulting in a filter with 23rd order for GSM and 15th order for DECT, designed using constrained equiripple algorithm to determine filter coefficients. The filter does not give sharp cutoff at the 100% of channel bandwidth but, since the main idea of using an inverse sinc filter is to correct the droop in passband and also to attenuate out of band noise centered at the decimated frequency to CNR below inband signal level, this filter is applied. Sharp cutoff frequency of the passband is only considered most in the last stage. For GSM standard, the filter is designed to have a passband of 82 kHz and a stopband rejection of –60 dB. For DECT standard, the filter is designed to have a passband of 574 kHz and a stopband rejection of –20 dB.

For the last stage of filtering, a generic FIR filter with a sharp passband cutoff frequency 82% of the signal channel bandwidth is applied to push out of band remaining undesired signal and also by considering the out of band noise centered at the frequency of decimate by two for the reasons mentioned earlier. The transition band is from 82% to 100% channel bandwidth. The filter is designed using Remez algorithm to determine a 47th order the filter coefficients. By using this sufficient amount of order, a filter with passband frequency of 82 kHz and a transition band ranging from 82 to 100 kHz attenuating at –20 dB is obtained for GSM standard. A 31st order filter is used to design the filter for DECT standard with passband frequency of 574 kHz and a transition band ranging from 574 to 700 kHz, attenuating at –13.4 dB.

4.0 DIGITAL FRONT-END IMPLEMENTATION AND RESULTS

The SDR terminal chosen in this work is the field programmable gate array (FPGA). FPGAs are re-configurable hardwares, composed of basic logic cells. FPGA implementation using fixed point architecture is chosen since it maximizes performance while minimizing cost.

4.1 I/Q Down-conversion Implementation

The conventional and most flexible approach to quadrature downconversion is to multiply the digitally sampled signal by a complex vector (e.g. numerically controlled oscillator) with periodic bit sequences [0 1 0 -1] and [1 0 -1 0] at fs, representing sine and cosine carriers, respectively. The usage of multiplier and complex vector oscillator consumes high logic resources and power.

Quadrature downconversion can be efficiently implemented by using multiplexers in a subsampling architecture, as shown in Figure 11, eliminating the use of two multipliers as in the conventional implementation. This approach is hardware and power efficient.

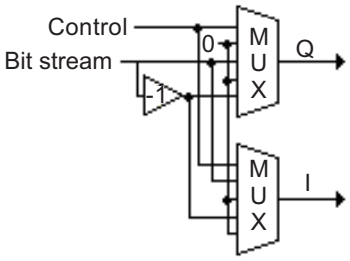


Figure 11 I/Q downconversion implementation architecture

4.2 Comb Filter Implementation

According to its transfer function given in equation (29), the comb filter can be efficiently implemented as shown in Figure 12. The magnitude response, H(z), (equation) is separated into numerator and denominator sections by moving the denominator section after the decimation operation. Hence, the filter can be implemented without multiplier. To avoid overflow problem, a 2's complement wrap-around arithmetic is used as long as the register width is greater or equal to the value given by equation (31).

$$\text{Reg\_Width} = N\log_2(M) + B_{in} \tag{31}$$

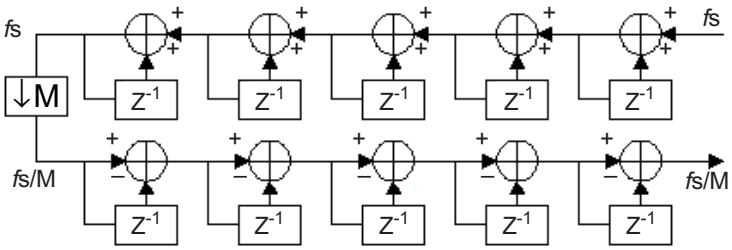


Figure 12 Comb filter implementation architecture

4.3 FIR Filter Implementation

For FIR filters in the second and last stage, two FPGA hardware efficient architectures have been envisaged. In both architectures, the FIR filter is implemented as a dual channel polyphase FIR filters in order to reduce the FPGA resource usage and power consumption. The first solution is based on single multiply-accumulate (MAC) engine to compute the sum of products. In the second solution, a distributed arithmetic (DA) FIR filter is considered. DA algorithm is a well-known method to save resources implementing DSP functions. It performs the multiplication using look-up table.

In an FPGA, a MAC type filter will occupy a fixed amount of logic resources for any N order of the filter, but will take additional N clock cycles for each sample as orders are added. A DA filter runs in the same number of clock cycles regardless of the number of filter order, but requires more logic resources as the filter order is increased. The hardware efficient implementation has been obtained by developing an FPGA-adapted model for the corresponding operators with VHDL.

The best compromise between logic resources and clock cycle for GSM and DECT filters is obtained with the dual channel polyphase MAC based implementation solution. In this approach, the I and Q input signals are time division multiplexed (TDM) to form a single line input sampled at 2*f*s and fed to a MAC based FIR filtering. The final output will be split back to I and Q form at *f*s/2. Though this implementation requires higher frequency clock cycle, the clock frequency value can keep pace with DSP task in FPGA since today's FPGAs can handle being clocked at frequencies more than 100 MHz. Logic resources saving using MAC implementation are very much higher compared to DA implementation.

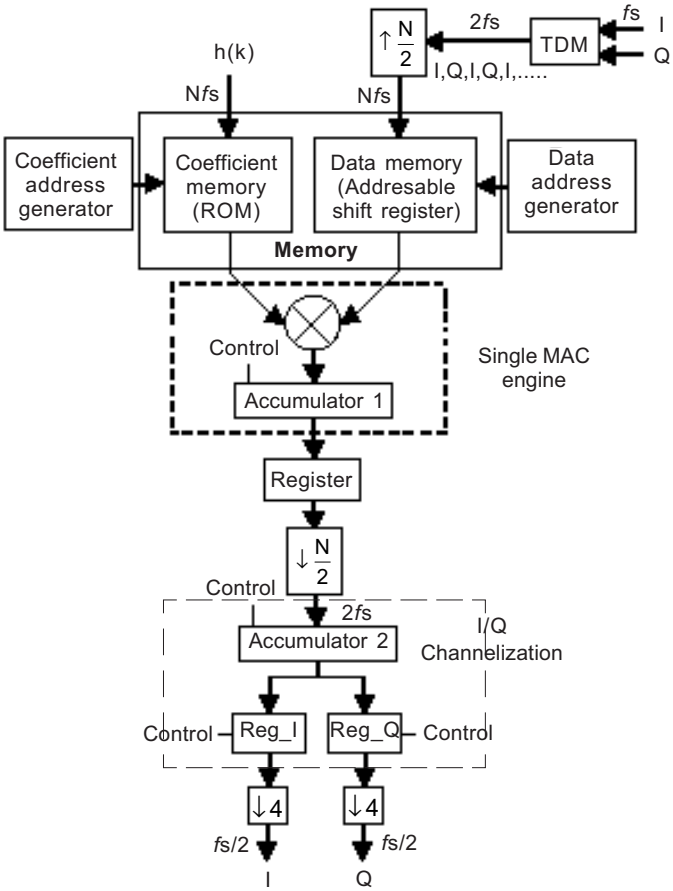
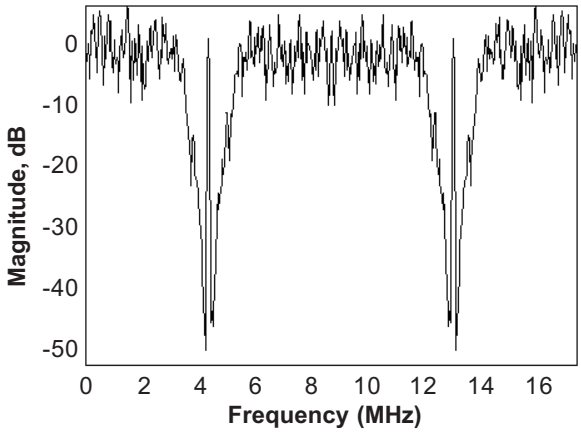


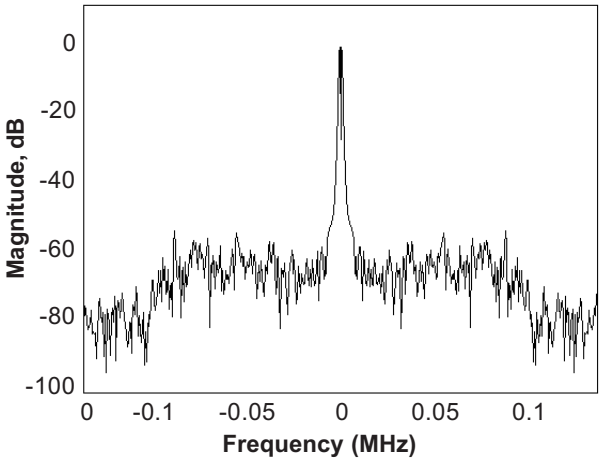
Figure 13 Dual channel polyphase MAC FIR filter implementation architecture

Note that the number of order for DECT FIR filters are lower compared to GSM filters. This is because, since the sampling frequency for DECT is much higher compared to GSM, increasing the number of order will increase the clock frequency required for the MAC operation. To avoid very high clock frequency requirement, which will increase the power consumption for computation, the reduced number of orders are used to design the FIR filters for DECT.

Figures 14 and 15 show the spectrum analysis of the digital front-end for both the standard. Figure (a) represents the input signal from sigma delta modulator for 1st and 2nd Nyquist zone. Figure (b) shows the signal in the 2nd Nyquist zone that is downconverted to baseband and filtered to match the CNR, bandwidth, channel ripple, and symbol rate according to its respective standard.

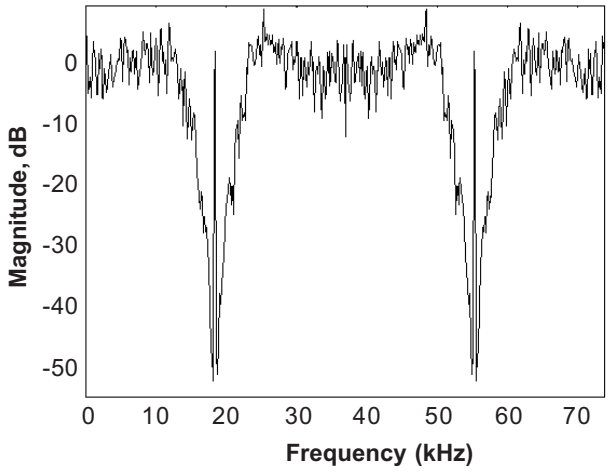


(a)

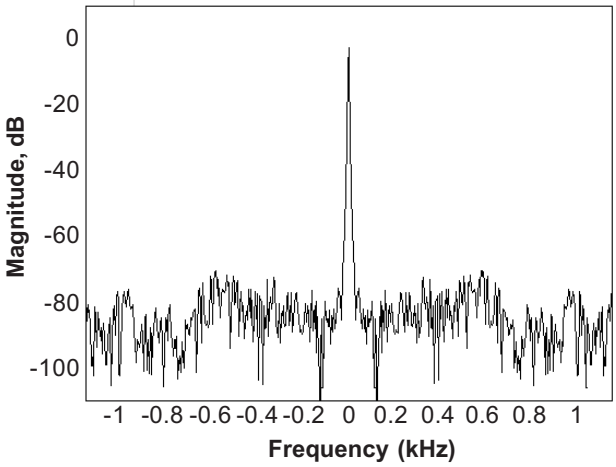


(b)

Figure 14 Experimental performance of GSM digital front-end



(a)



(b)

Figure 15 Experimental performance of DECT digital front-end

5.0 CONCLUSION

A number of different architectures for use as analog front-end in a multi-standard SDR receiver is discussed and analysed in this paper. A suitable architecture with regard to moving the digitising point one stage closer to the antenna, wideband IF subsampling, is considered for the approach of digital front-end of the receiver. The architecture and hardware implementation of the digital front-end designed for a 4th order bandpass sigma delta modulator have been described. Optimized architecture carried to multiplier less quadrature downconversion and multirate filtering composed of 5th order comb filter, an inverse sinc FIR filter and a generic FIR filter. Obtained

results show that the use of multiplexers for quadrature downconversion implementation, carry ripple adders for comb filter implementation, and a dual channel polyphase single MAC engine based filter for the inverse sinc and generic FIR filters implementation, minimize the FPGA logic resources requirement for a hardware efficient solution.

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