Jurnal
Teknologi

Full Paper

Fabrication of Pyramidal Cavity Structure with Micron-sized Tip using Anisotropic KOH Etching of Silicon (100)

Article history
Received
16 January 2015
Received in revised form
24 March 2015
Accepted
15 March 2015

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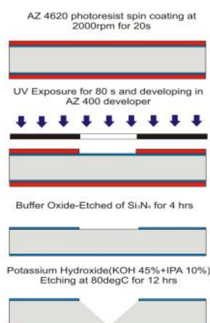
Graphical Abstract



Abstract

Microelectromechanical System (MEMS) are systems of micron-sized structures and typically integrated with microelectronic components. Bulk micromachining using wet anisotropic etching is able to etch silicon substrates to a desired three-dimensional (3D) structure, depending on the silicon crystallographic orientation. To date, MEMS components i.e. thermal, pressure, mechanical, bio/chemical sensors have been fabricated with wet anisotropic etching of silicon. This paper presents the fabrication of a 3D pyramidal cavity structure with micron-sized tip of silicon (100) using anisotropic KOH etching of w/w 45 % at 80 °C temperature. Volume percent of 10 % IPA as a less polar diluent is added to the KOH etching solution in saturating the solution and controlling the etching selectivity and rate. Smooth etched silicon surface of hillock free is able to be achieved with IPA addition to the KOH etching solution. A characteristic V-shaped cavity with side angle of 54.8 degrees has successfully been formed and is almost identical to the theoretical structure model. Comparison of two different silicon nitride window masks on the micron-size tip formation is also investigated. Under etch, over etch and etching selectivity, as common problems effecting the micron-tip size variation, are also addressed in this work. In conclusion, anisotropic KOH etching as a simple, fast and inexpensive bulk micromachining technique, in fabricating 3D MEMS structure using silicon (100), is validated in this work.

Keywords: MEMS, crystallographic orientation, pyramidal cavity structure, anisotropic, KOH etching

Abstrak

Sistem mikroelektromekanikal (MEMS) mempunyai struktur bersaiz mikro dan kebiasannya diintegrasikan dengan komponen elektronik. Pemesinan mikro pukal menggunakan punaran basah anisotropik dapat memunar substrat silikon untuk membentuk struktur tiga dimensi (3D) yang bergantung kepada orientasi hablur silikon. Kini, komponen MEMS seperti penderia i.e. terma, tekanan, mekanikal, bio/kimia telah difabrikasi dengan cara punaran basah anisotropik ke atas silikon. Kajian ini membincangkan proses fabrikasi caviti 3D berbentuk piramid berhujung bersaiz mikro dengan punaran anisotropik KOH w/w 45% dan suhu 80 °C ke atas substrat silikon. Tambahan IPA sebagai diluen dwikutub sebanyak 10 % dalam peratusan isipadu ke dalam larutan punaran KOH dapat menepukan larutan dan mengawal selektiviti punaran dan kadarnya. Penghasilan permukaan struktur silikon yang licin tanpa hilok dapat dihasilkan dengan penambahan IPA ini. Ciri caviti berbentuk-V dengan sudut sisi 54.8 darjah dapat dibentuk dan serupa dengan model struktur teori. Hasil hujung berbentuk-V dengan menggunakan dua jenis tetopeng silikon nitrid juga dibandingkan. Makan dalam (*underetch*), terlebih punar dan selektiviti punaran merupakan permasalahan utama dalam penghasilan hujung bersaiz

mikro juga diterangkan dalam kajian ini. Kesimpulannya, struktur MEMS 3D menggunakan substrat silikon berjaya dihasilkan dengan teknik punaran anisotropik yang mudah, cepat dan murah.

Kata kunci: MEMS, orientasi hablur, struktur kaviti piramid, anisotropik, punaran KOH
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1.0 INTRODUCTION

Over more than five decades, bulk micromachining using wet anisotropic etching has been intensively employed in MEMS technology. The demand of wet anisotropic etching as a vital process in silicon bulk micromachining is due to the formation of unique 3D structures depending on the silicon crystallographic orientation with various etchants. In addition, bulk micromachining using wet etching has the advantages of being lower in cost, having higher degree of selectivity and a faster etching rate in comparison to dry etching [1].

Anisotropic etching using alkaline aqueous solution of KOH has been practiced to fabricate a wide range of MEMS sensors i.e. mechanical, thermal or even bio/chemical sensors [2]. Besides MEMS sensors, silicon micro-needles, ink-jet nozzles and magnetic micron-sized cores have also been fabricated using KOH etching [3]–[5]. However, due to the crystallographic characteristics of silicon, the shape and size of the microstructure formation is limited [2]. Silicon diaphragm, cantilever and V-grooves are examples of 3D microstructures that can be formed by KOH etching. KOH concentrations ranging from 35 to 45 % at 80 °C have been investigated for low surface roughness [6]. The addition of IPA as a less polar diluent in the etching solution can result in better selectivity with more control etching processes and rates [7], [8]. A decrease of 20 % for <100> in KOH etching rate has also been evaluated [9]. In anisotropic etching, the etching rate is temperature dependent. An Etching process conducted at high temperature increases the etching rate and reduces the surface roughness [1]. To avoid solvent evaporation and temperature gradient effects, KOH etching experiment is conducted at temperatures between 80 and 85 °C [1].

In this work, investigation on the pyramidal cavity micron-size tips formation of single crystal silicon (100) is conducted. The anisotropic etching process parameter of 45% KOH concentration and 80 °C temperature have been selected. Volume ratio (v/v) 10 % of IPA as minimal polar diluent is added to the KOH etching solution for smooth and hillocks free silicon surface. The step by step processes from the mask design, photolithography, BOE etching and KOH etching are also described in this paper. In addition, comparison on two different silicon nitride masks used on pyramidal cavity micron-size tips formation is also observed.

2.0 THEORETICAL

By using alkaline etchants (i.e. KOH, NaOH, CeOH, RbOH) silicon is able to be etched anisotropically. Anisotropic KOH wet etching creates characteristic V-shaped or inverted pyramidal cavity structure in silicon (100). The etch rate for silicon is dependent on the crystallographic orientation. The <100> plane is the fastest etching plane while the <111> plane is the slowest etching plane with the ratio 400:1 [11]. The anisotropy effect from the etching process can be unambiguously observed from its structure profiles. The formation of four concave corners and faces are due to the fact that limiting shape is determined by the slowest etching plane [2]. In the KOH etching, reaction of silicon with water and an OH- ions creates hydroxide ions and hydrogen gas bubbles [1].

Silicon + Water + Hydroxide Ions → Silicates + Hydrogen (1)

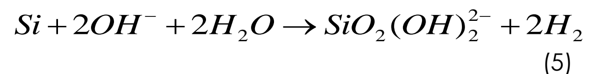
The basic chemical reaction that occurs as a result of alkaline solution etching of silicon are [11]

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e \quad (2)$$

$$4H_2O + 4e \rightarrow 4OH^- + 2H_2 \quad (3)$$

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2-} + 2H_2O \quad (4)$$

Therefore, the overall reaction can be written as



$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2 \quad (5)$$

A final result of the etched process is an inverted pyramid or a V-shaped cavity structure with an angle of 54.7 degrees between the <100> and <111> direction. Early hypothesis of the etched shape formation is defined as the existence of different activation energies and back bond geometries of silicon surfaces [9]. Furthermore, the well-known fluctuating energy level model at the silicon and etchant interface is assumed by Seidel. In the model, electrons in the conduction band of silicon are injected during the alkaline etching process and thus reacted with water to form hydroxide ions and hydrogens as depicted in equation 3 [9]. Later investigations on the etching rate and silicon morphology by Veenendaal *et al*. suggested the velocity source concept [12]. This forest of velocity sources is a kind of insistent corrugation that affects

the micro-morphology of the silicon surface regardless of the crystallographic orientation.

The dimension of the pyramidal cavity tip is determined by the thickness of the silicon substrate and the mask size. The equation developed on the tip dimension originated from the surfaces and planes orientation. Anisotropic silicon (100) etched a feature of a square shaped mask with the pyramidal cavity tip width and the mask opening width are as illustrated in Figure 1.

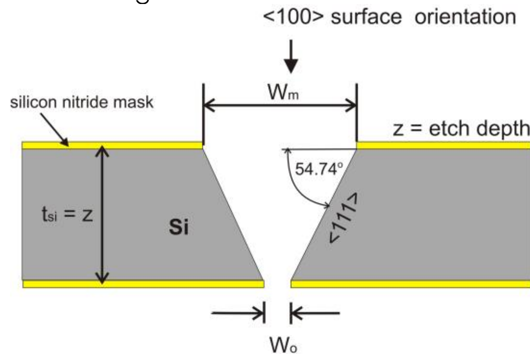


Figure 1 Anisotropic etching of (100) silicon

The pyramidal cavity tip width can be calculated, provided the mask opening, W_o and the silicon thickness, z are known [1]. The derived equation for the cavity tip width is

$$W_o = W_m - 2cotan(54.74^o)z \quad (6)$$

or, in a simplified form as

$$W_o = W_m - \sqrt{2}z \quad (7)$$

3.0 METHODOLOGY

3.1 Substrate Selection and Preparation

Silicon has been used as a substrate in the development of MEMS sensor due to its intrinsic stability and potential of electrical and electronic components integration [1]. In this work, single crystal silicon (100) is chosen as the substrate material due to its ability to be shaped into a pyramidal cavity structure using anisotropic KOH etching. Furthermore, it is possible to theoretically determine the cavity structure tip using equation (6). One of the important factors in considering silicon as a substrate is its high thermal conductivity and melting point. These factors are crucial whenever high heat generation is expected as a result of Joule heating effects from the application of conductor carrying currents i.e. electromagnetic coil. In this work, two different silicon nitride film thicknesses are used. Silicon with thick nitride film or silicon nitride substrate is chosen as a window mask due to its capability to withstand alkaline solution etching with minimal etching rate of less than 1 nm/hour [1]. The thickness of the silicon nitride thick layer is measured using F50 Thin Film Mapper (Filmetrics, USA). The silicon nitride film thickness will determine the BOE etching duration for bulk micromachining window masks using KOH etchant. Specification of the silicon substrate used in this work and the silicon physical properties are as listed in Table 1 and Table 2, respectively [1], [10], [13].

Table 1 Specification of the silicon nitride used in this work

Diameter	6 in (150.0 mm)	6 in (150.0 mm)
Thickness (μm)	670-685	650-675
Type	{100} p-type	{100} p-type
Surface colour	metallic yellowish	metallic violet
Polishing	front side polished	front and back side polished
Nitride film thickness	147 nm	200 nm

Table 2 Material characteristics of single crystal silicon

Material Properties	Value
Yield strength (10^9 N/m2 = Gpa)	2.8-6.8
Specific strength [10^3 m^2 s^{-2}]	3040
Knoop Hardness (kg/mm²)	850-1100
Young Modulus (10^9 N/m² = GPa)	129 (100)
Poisson Ratio	0.22
Density (10^3 kg/m³)	2.32
Thermal conductivity at 300 K (W/cmK)	1.56
Linear Coefficient of Thermal Expansion (10^{-6}/°C)	2.616
Melting Point (°C)	1415

The substrate is prepared prior to a photolithography process. In this work, a square-shaped silicon chip of 1.0 in x 1.0 in (2.56 cm x 2.56 cm) is diced from a 6 inch (150.0 mm) P-typed silicon nitride wafer using a wafer scriber with a diamond tip. The chips are then cleaned using RCA-1 of hydrogen peroxide-ammonium hydroxide (H_2O_2-NH_4OH-H_2O_2), RCA-2 of hydrogen peroxide–hydrochloric acid (H_2O_2-HCl-H_2O_2). The RCA solution is heated to 75 degrees Celsius using the double boiler method and the silicon chip cleaning is performed for 15 minutes. Rinsing with DI water is performed at every completion of RCA cleaning. The RCA cleaning methods are purposely to clean organic, oxide and ionic contaminants that might prevent lithography and the reliability of the etching process [14]. A standard wafer cleaning method is conducted with a 5-minute ultrasonic agitation of acetone and 3-minute rinsing with flowing DI water. Oxide removal using 10 % hydrofluoric acid is then performed by dipping the chips for 10 second. A nitrogen gas gun is used to blow dry the chips to complete the cleaning step.

3.2 Photolithography Technique

Photolithography process starts with dehydration baking of the chip sample. Dehydration baking is performed to dry any excess moisture in the silicon substrate. In this work, chip samples are dehydration-baked at 150 °C hotplate for 30 minutes. The photolithography process is conducted using clean room facilities at the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia. The basic step in photolithography is the design mask drawing. The mask is drawn using CorelDRAW™ X4 drawing software and printed onto an A4-sized transparency using high resolution photo plotter (OG Graphics, Malaysia). A negative mask is prepared as the process requires the use of a positive-type photoresist. A sample of negative mask with five square-shaped etching windows of 920 μm x 920 μm is as shown in Figure 2. The square-shaped size dimension of the window mask with 920 μm x 920 μm and 890 μm x 890 μm are selected for the purpose of constructing the smallest tip structure corresponding to the silicon thickness. Moreover, the smaller size window mask opening is also designed to mitigate the undercut and over etching problems during the KOH etching process.

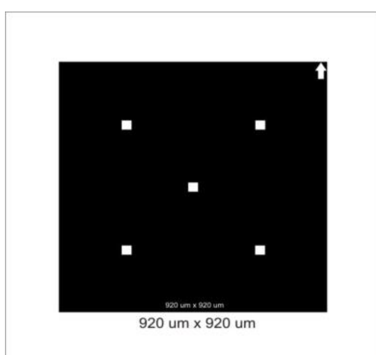


Figure 2 Negative mask with five etching windows for positive photoresist patterning

In photolithography process, by using positive photoresist, a transparent window will permit UV light through it and changes its chemical structures. The chemical structure change will prevent the photoresist to cross-link or cure. As a result, the photoresist is easily stripped off during the development process. The window mask pattern transfer is performed using AZ4620 positive photoresist (MicroChem, Germany).

AZ4000 series photoresist is formulated using *propylene glycol monomethyl ether acetate* (PGMEA) solvent intended for 3 to 60 μm thickness deposition [15]. The AZ4000 series has a good adhesion on silicon substrate after the soft-baking process even without any adhesion promoting agent. The photoresist thickness is determined by the spin coater rotation speed and can be referred in the photoresist manufacturer datasheet. In this work, a 2000 rpm spin coater rotation is selected whereby it is able to deposit 12.0 μm of photoresist layer onto the silicon chip. The photoresist is considered as optimum and expected to withstand 4 hours of BOE etching of the nitride mask.

In this work, a UV light mask aligner machine (Karl Suss, Germany) with light intensity of 2.6 W/cm^2 is used. The pattern transfer from the mask to the photoresist is by using i-line UV light of wavelength 365 nm. Proximity photolithography process of minimal distance between the pattern mask and substrate is conducted using the mask aligner. Photoresist development is a process of transforming the latent image produced by the UV light exposure to a visible pattern using a liquid developer. Ratio of 3:1 of DI water and AZ400K series developer is used. The AZ400K series is formulated for AZ4000 series positive photoresist stripping. The silicon chip is then rinsed with DI water and dried with the nitrogen gas gun. Hard baking process on a hotplate is performed for 20 minutes at a temperature of 120 °C.

3.3 Buffered-oxide Etching 10:1

In preparing the window pattern for the KOH wet etching, the silicon nitride layer needs to be etched first. In this process, Buffered-Oxide Etchant (BOE) 10:1 of CMOS grade (J.T. Baker, USA) is used. The BOE contains hydrofluoric acid (HF) of weight/weight (w/w) ratio 4.4 – 4.7 % and ammonium fluoride (NH_4F) of w/w 35.5 – 37.5 % as the buffer agent. NH_4F the buffer agent acts to maintain the HF concentration and the etchant pH value. Furthermore, NH_4F prevents damage on photoresist during BOE etching. BOE is a selective etchant, therefore an etch stop process will be initiated once it reaches the silicon. The BOE etching process duration is determined by the silicon nitride thickness. In this work, up to 4 hours is needed to etch through the 147 nm thick nitride layer and a maximum of 5 hours for 200 nm nitride layer.

Estimation of the nitride layer thickness that has been etched can be referred to the relative light intensity spectrum to the nitride film thickness. Apart from that, silicon surface of metal silver colour can be observed using naked eyes or by the aid of an optical microscope (Olympus, Germany) once the nitride layer has been etched. Hydrophobic surface test on the silicon surface can also be conducted to determine the completion of the nitride layer etching. The silicon chip is then cleaned with acetone to remove the photoresist protective layer.

3.4 Anisotropic KOH Etching

KOH wet etching is determined by solution concentration and temperature. In this work, KOH pellet of CAS No. 1310-58-3 (J.T Baker, USA) is mixed with DI water at 45 % w/w. After the exothermic reaction between KOH and water cools down, the solution is heated using double boiler method as shown in Figure 3. Double boiler heating method is

preferred due to its controllability and gives consistent heating of the etchant. Digital precise hot plate with feedback control (WiseTherm, Germany) is used. The 45 % KOH solution temperature is then set to 80 °C. The 45% KOH concentration and 80 °C temperature is chosen for smooth etched surface and good etching process. The silicon chip substrate is clamped using stainless steel screwed teflon clamp and silicone rubber O-ring to prevent unwanted etching of back and side surfaces. The KOH etching experimental set-up schematic is as shown in Figure 4. The etching rate is expected to be 55 µm/hour according to the theoretical chart [1]. Isopropanol (IPA) v/v 10 % is added to the etching solution to control and increase KOH etching selectivity. The KOH 45% with IPA addition took up to 15 hours to complete in etching approximately 680 µm silicon thickness. The characterization of the etched silicon thickness is done using Olympus optical microscope for every 3-hour intervals. Once the etching process is completed, the silicon chips are rinsed for 3 minutes under continuous DI water flow and dried using the nitrogen gas gun. The schematic of the simplified pyramidal cavity with micron-sized tip fabrication is as shown in Figure 4.

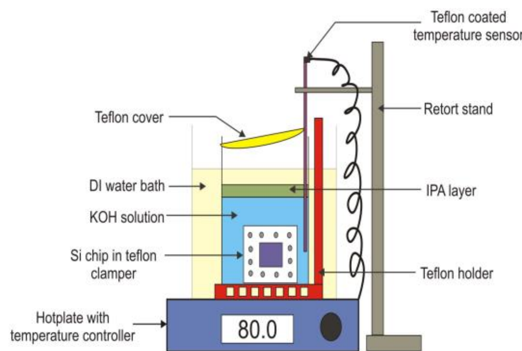


Figure 3 Schematic of the KOH etching experimental setup

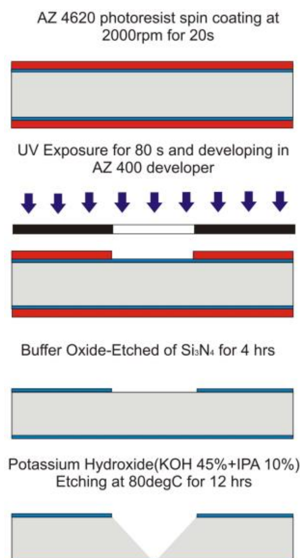


Figure 4 Schematic of the simplified pyramidal cavity with micron-sized tip fabrication steps

4.0 RESULTS AND DISCUSSION

The pattern of five photoresist mask windows of square-shaped with dimension (a) 920 µm x 920 µm (b) 890 µm x 890 µm are as shown in Figure 5. A good pattern transferred from the transparency mask to the silicon substrate by photolithography process is observed. However, there was an uncovered area of the silicon chip by the photoresist due to smaller area dimensions of the transparency mask in comparison to the silicon chip dimension. To alleviate the problem, a manual application of liquid photoresist using a nylon brush is performed. This touch-up step is required to prevent damages of the silicon nitride surface during BOE etching process. The close-up images of the pattern photoresist mask window are as shown in Figure 6. The thickness of the photoresist is measured to be an average of 10.0 µm by using an optical microscope. The slight disprecancy in comparison with the thickness of 12.0 µm from manufacturer datasheet can be due to inexact and higher fluctuations of spin coater speed. Evaporation of the photoresist solvent during the soft and hard baking processes also contributed to thickness suppression. A good and clean silicon nitride surface is observed for 920 µm x 920 µm square-shaped window. However, stain of undeveloped photoresist is detected by optical microscope digital camera and Analysis software. The adherence stain of the undeveloped photoresist is hard to clean even at increasing developing time and silicon chip agitation. Extended developing time needs to be avoided as to prevent any damages of the window pattern side surfaces. As a small tip area structure is desired, a very good window pattern, dimension and edges needs to be preserved during the overall processes.

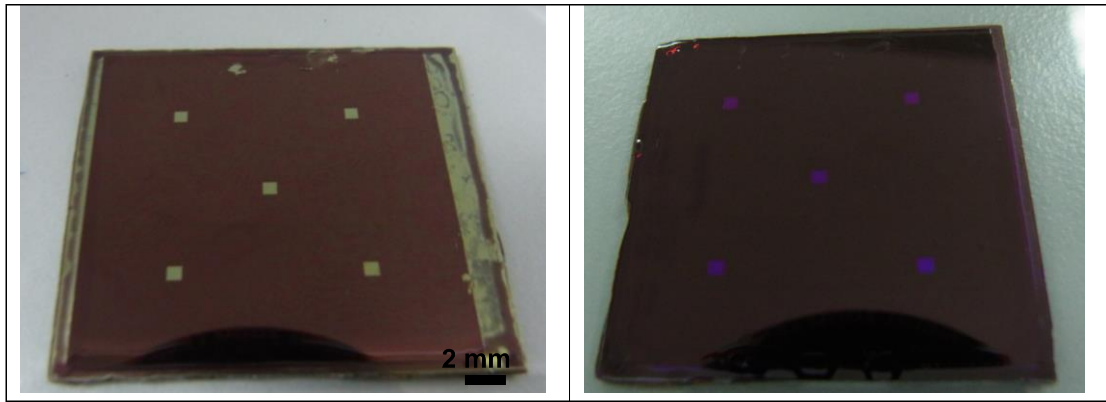
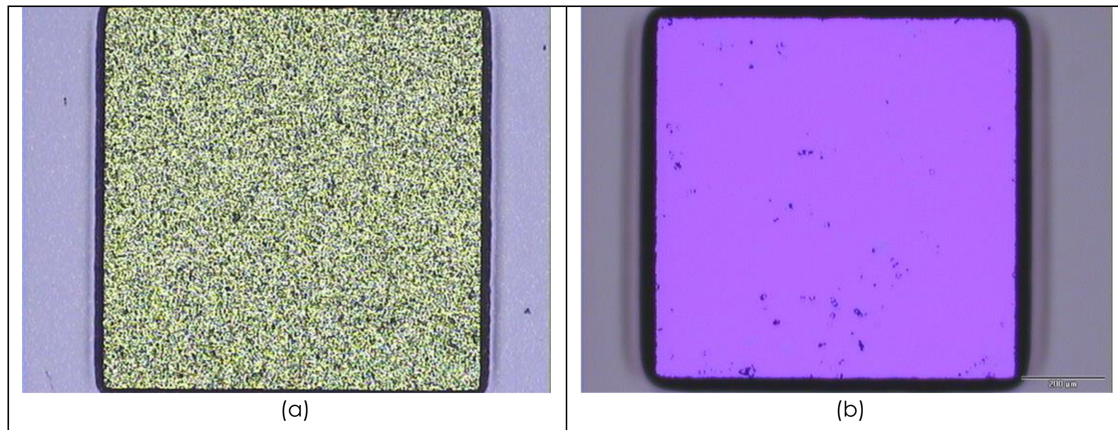


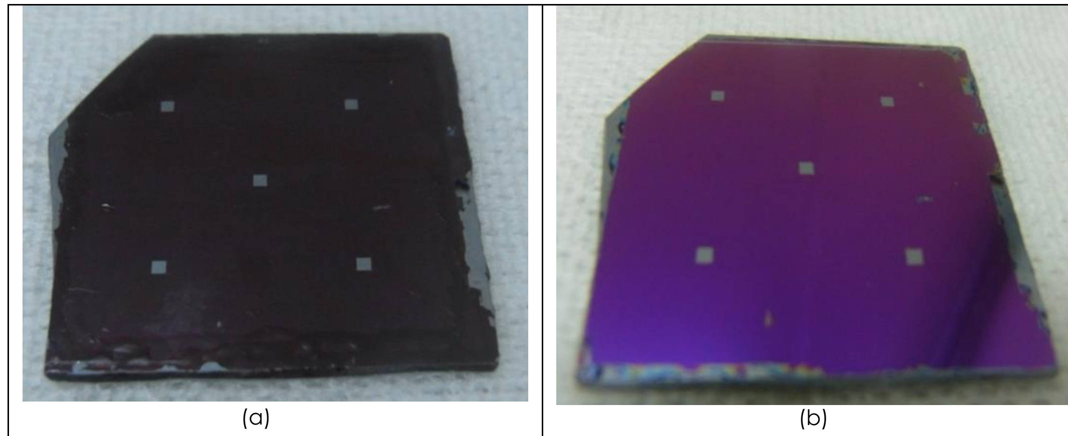
Figure 5 Lithography of the patterned photoresist mask



(a) (b)

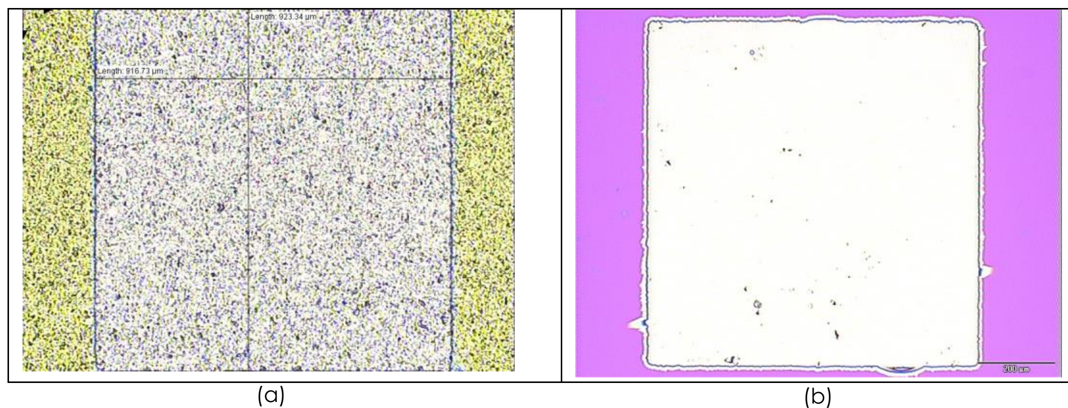
Figure 1 Square-shaped photoresist mask window opening (a) 920 μm x 920 μm (b) 890 μm x 890 μm

BOE etching has successfully stripped off the silicon nitride layer. The silicon nitride chip before and after the acetone cleaning of the photoresist are as shown in Figure 7. Bare silicon surface of silver colour is observed after the completion of nitride layer removal. Silicon chip side surface damages are also observed after the BOE etching process. This problem is due to peeling of the touched up photoresist in the BOE solution. The touch-up method using nylon brush was not a good solution in covering the exposed nitride layer after the photolithography process. This is suspected due to low adhesion of the thick photoresist on the silicon substrate in comparison to the photoresist spin coating process. From the optical microscope images, a course surface of silicon is observed for the square-shaped window with dimension of 920 μm x 920 μm in comparison to the 890 μm x 890 μm. This is due to the fact that fabrication of the square-shaped window with dimension of 920 μm x 920 μm is on the unpolished side of silicon nitride.



(a) (b)

Figure 7 Completed nitride layer removal with BOE process (a) before (b) after photoresist cleaning



(a) (b)

Figure 2 Square-shaped nitride mask window opening (a) 920 µm x 920 µm (b) 890 µm x 890 µm

In this work, an obvious overetched of silicon nitride window on the side areas are observed after the acetone cleaning step; as shown in Figure 9. The defected and skewed nitride mask edges are not desired in this work as it will affect the final structure shaped by KOH etching technique. The overetched or chipped nitride layer edges is significant with the 200 nm silicon nitride layer mask in comparison with 147 nm silicon nitride layer mask. The reason for this is due to the high internal and residual stresses of the thicker silicon nitride deposition by the surface micromachining chemical vapor deposition (CVD) process [16]. The damages on the silicon nitride layer is also a result of overdeveloping the photoresist pattern window during the photolithography development process.

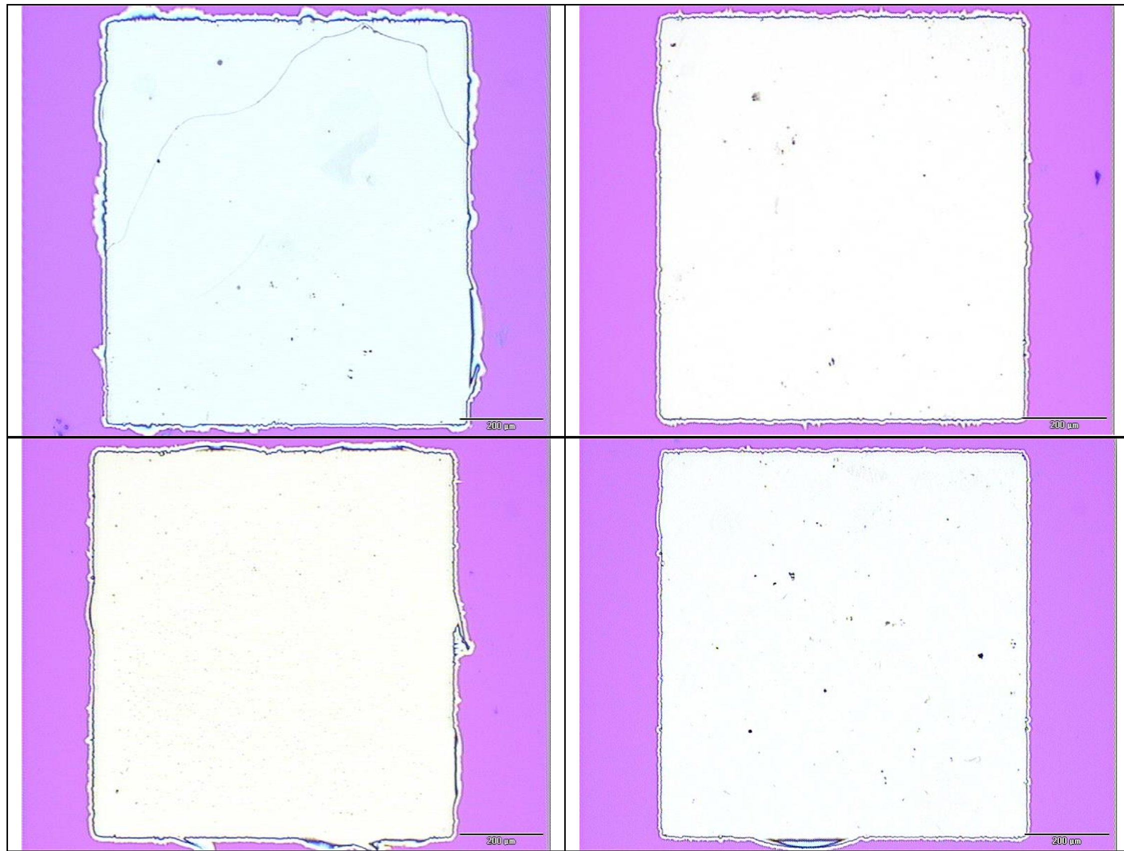


Figure 3 Defected nitride mask window pattern for square-shaped 890 μm x 890 μm after the BOE process

The etching rate of the pyramidal cavity structure using the square-shaped 920 μm x 920 μm mask window is as plotted in Figure 10. The time taken to complete the KOH etching is 12 hours and 45 minutes at approximately 46 μm/hr etching rate. On the other hand, the cavity structure using the square-shaped 890 μm x 890 μm took about 12 hours to complete with an etching rate of approximately 48 μm/hr. The silicon thickness etched from four cavity structures of the square-shaped 920 μm x 920 μm mask window are almost consistent. The reduction of the etching rate from the theoretical KOH etching rate is as expected due to IPA; less polar diluent addition acts in leveraging the etching process. The control etching rate is due to less evaporation of water molecules from the etching solution due to less dense IPA layer covering it. To get a good etching rate and process, the IPA layer needs to be maintained by adding up the solvent such that it remains at 10 % volume level.

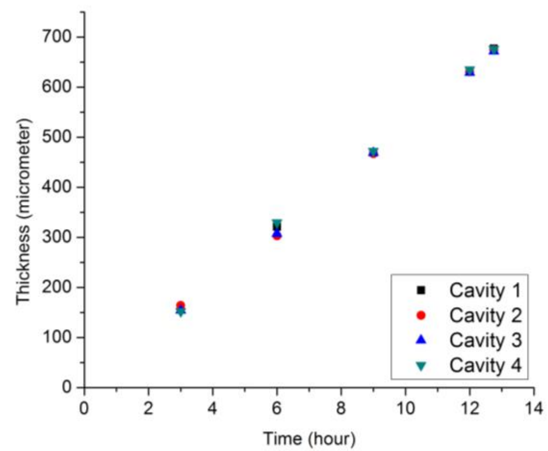


Figure 4 Etching rate of KOH 45 % with 10 % IPA at 80 °C for square-shaped nitride mask of 920 μm x 920 μm

Silicon inverted pyramidal cavity structure was successfully fabricated using KOH etching with silicon nitride window mask. SEM images of the front and side views of the structure are as shown in Figure 11 and Figure 12. A characteristic V-shaped feature of 54.8 degree side wall angle is clearly seen from Figure 12. There is a slight discrepancy of 0.14 degrees from the theoretical structure angle as explained in the theoretical part. A smooth and fine etching of the

silicon surface with free hillocks formation has also been observed from this work. The reason for this to happen is due to the high concentration of KOH and also IPA addition [7], [1], [17]. IPA addition into the KOH etching solution does not interrupt the KOH etching reaction, but controls the KOH etching by decreasing the etching rate. In addition, selectivity for <111> versus <100> planes is significantly increased with the IPA addition [8].

The undercut problem is obviously seen from Figure 12 and demonstrated again in the schematic shown in Figure 15 (b). For the 920 μm x 920 μm etching mask dimension, 10 % widening of the etching window mask was calculated after the etching was complete. The undercut problem is common and unavoidable in KOH etching process due to variations of etching rates of <100> to <111> plane. The undercut problem can be minimized by selecting the optimum temperature and etchant batch composition as to improve the <100> to <111> etching plane selectivity [1]. In addition, a high quality etching mask fabrication from lithography to BOE etching process are also required.

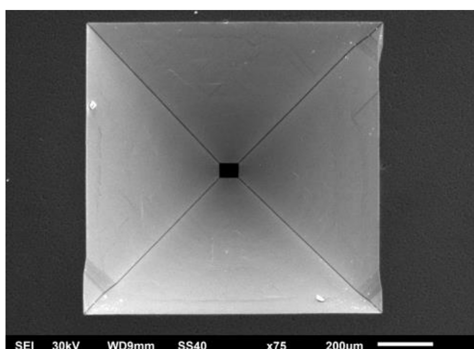


Figure 5 Top view of the pyramidal cavity structure of four concave sidewalls

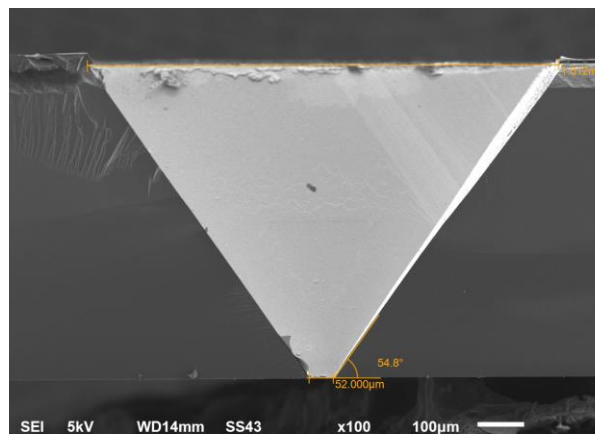


Figure 6 Cross-sectional view of the side wall angle of 54.8 degree using SEM

Other than the undercut problem, which is still an issue in KOH etching of silicon (100) surfaces, the etching window tolerance, etching rate, anisotropic selectivity, over etch, size control and load effects are also the factors that might influence the fabricated microstructure [1]. In this work, the small size pyramidal cavity structure tip is hindered by the combination of the KOH etching problems above. The tip area of size less than 20 μm x 20 μm was not achieved in this work. Examples of the different tip area sizes fabricated in this work are as shown in Figure 13 and Figure 14.

Early investigation between the 147 nm and 200 nm nitride mask thickness revealed that 200 nm nitride mask is proned to chip during long hours of KOH etching as shown in Figure 15(a). The cracked nitride mask edges might be due to the high residual stress of higher nitride film thickness deposited during the CVD surface deposition technique [16]. Less consistent dimensions of the pyramidal cavity tips were observed for 200 nm thickness nitride mask in comparison to 147 nm thickness mask as tabulated in Table 3.

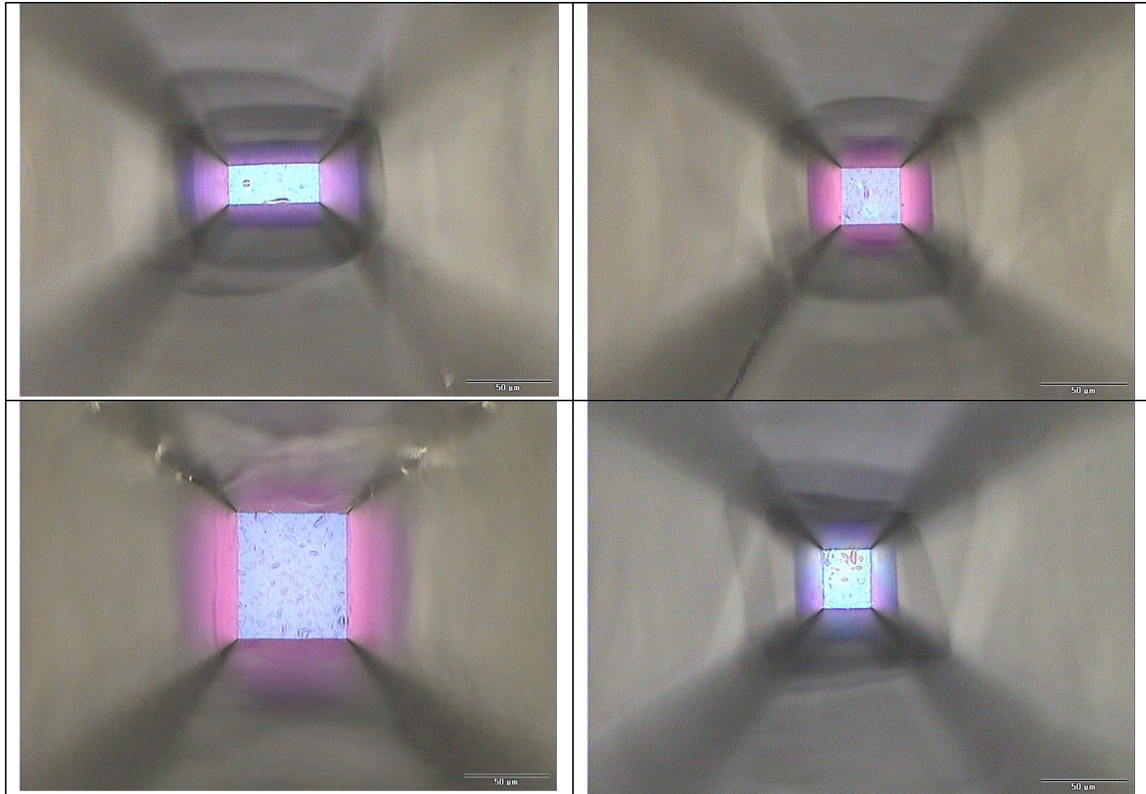


Figure 7 Pyramidal cavity tips fabricated using window mask of 920 μm x 920 μm

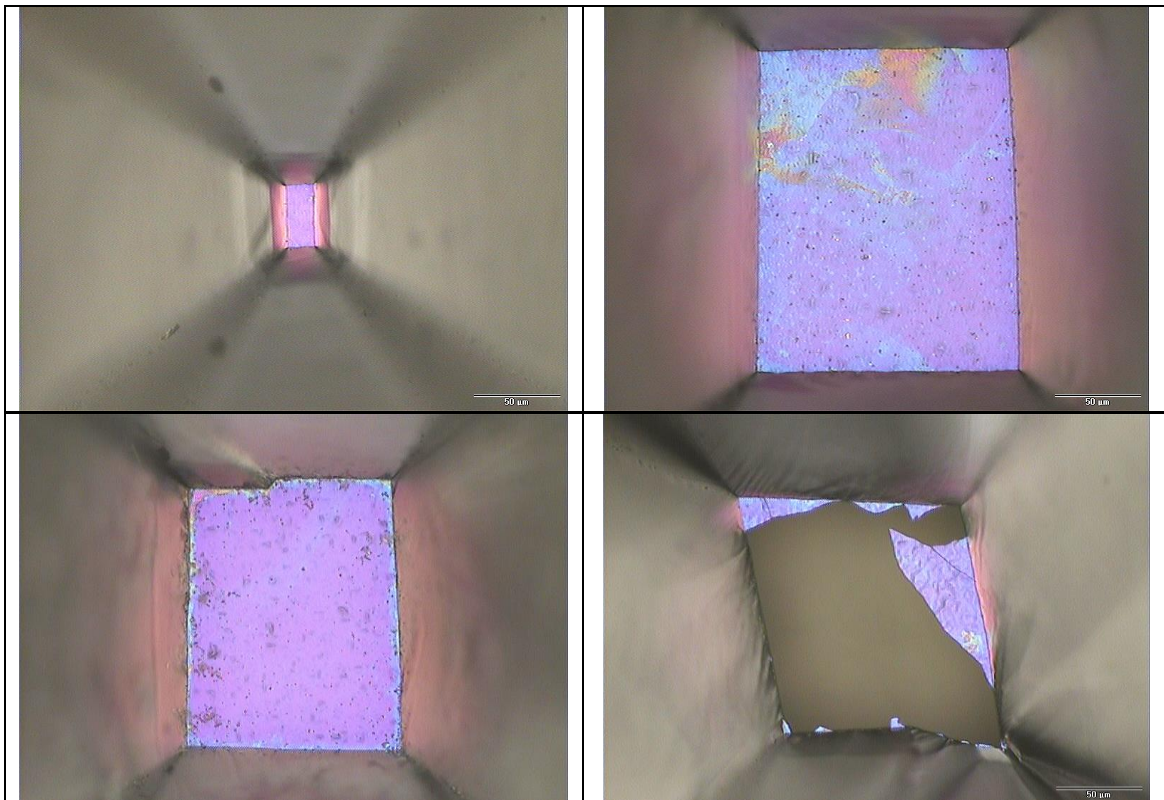


Figure 8 Pyramidal cavity tips fabricated using window mask of 890 μm x 890 μm

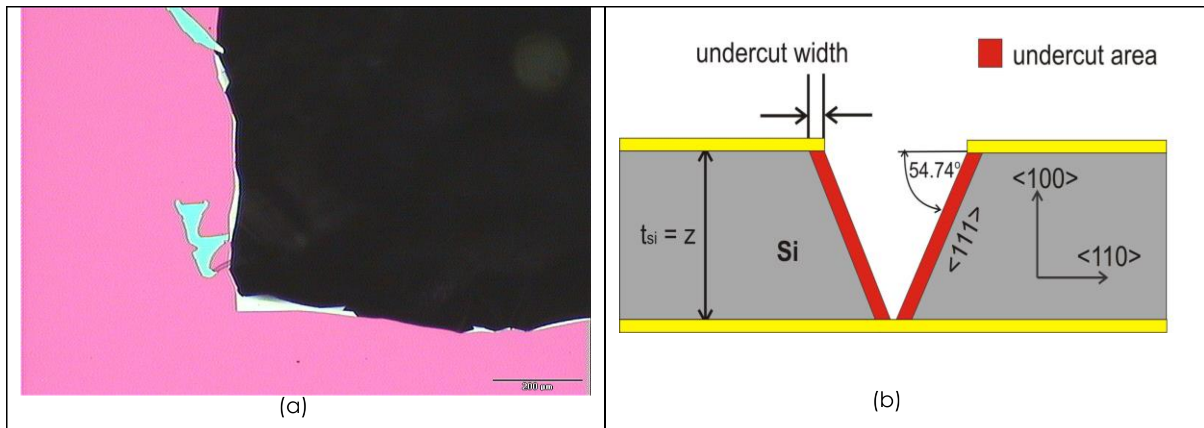


Figure 9 (a) Defected side edges of 200 nm thickness nitride mask during KOH etching (b) undercut problem

Moreover, larger cavity tip sizes are noticeable as a result of greater nitride mask dimension defects during the KOH etching. The comparison of the micron-size tips dimension in height (*h*) : width (*w*) between 147 nm and 200 nm thickness nitride masks are as shown in Table 3.

Table 3 Micron-size tips dimension formed with KOH etching

Cavity tip	Nitride window mask of 920 µm x 920 µm cavity tip dimension h : w (µm)	Nitride window mask of 890 µm x 890 µm cavity tip dimension in h : w (µm)
1	23.03 : 53.25	35.87 : 26.95
2	32.50 : 33.32	184.31 : 149.26
3	73.83 : 64.03	159.98 : 122.45
4	34.30 : 26.95	133.18 (h) : 126.17 (w1) : 125.35 (w2)

Another problem that deterred the small size pyramidal cavity tip formation is the silicon substrate thickness variation. The varying of the silicon substrate thickness originates from the manufacturing of silicon substrate i.e. slicing, lapping and polishing. As anticipated from manufacturing processes, zero tolerance is impossible to be achieved. The variation of the silicon substrate of 200 nm thickness is as shown in Figure 16.

5.0 CONCLUSION

In this work, silicon pyramidal cavity structures with micron-size tip have been successfully fabricated from anisotropic KOH etching. A smooth and hillocks free silicon etched surface with a consistent etching process have been achieved by the application of KOH etchant concentration of 45 % with a 10 % IPA addition at a temperature of 80 °C. Variations in the dimensions of the cavity structure tips are mainly due to the undercut problem and nitride mask edges deterioration during photolithography, BOE and KOH etching processes. In addition, the variation of silicon substrate thickness also affects the micron sized cavity tip formation. In conclusion, the bulk micromachining using KOH etching as a simple, fast and inexpensive technique for 3D silicon microstructure formation in MEMS application has been demonstrated in this work.

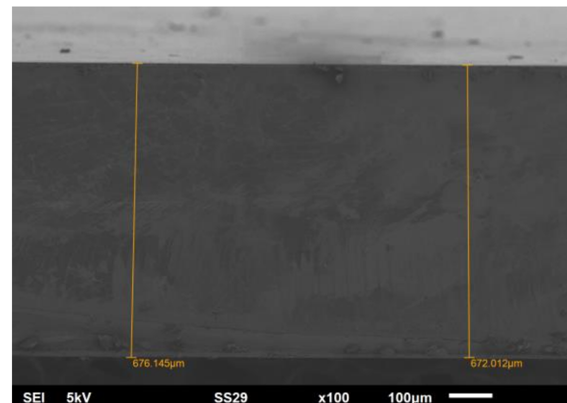


Figure 10 Silicon substrate thickness variation for nitride layer of 147 nm

Acknowledgement

We are grateful for the UTM scholarship and would like to thank the Ministry of Higher Education of Malaysia and Universiti Kebangsaan Malaysia for the research grant under the project NND/ND/(1)/TD11-002.

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