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TAGUCHI MODELING OF PROCESS PARAMETERS IN VDG-MOSFET DEVICE FOR HIGHER I_{ON}/I_{OFF} RATIO

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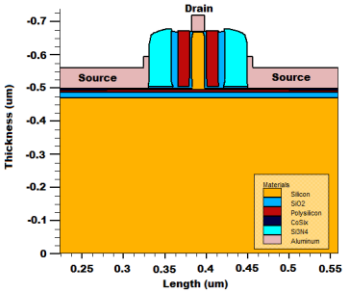
Graphical abstract



Abstract

The miniaturization in the size of planar MOSFET device seems to be limited when it reaches to 22nm technology node. In this paper, the vertical double gate architecture of MOSFET device with ultrathin Si- pillar was introduced by keeping both silicon dioxide (SiO_2) and polysilicon as the main materials. The proposed MOSFET architecture was known as Ultrathin Pillar Vertical Double Gate (VDG) MOSFET device and it was integrated with polysilicon-on-insulator (PSOI) technology for a superior electrical performance. The virtual device fabrication and characterization were done by using ATHENA and ATLAS modules of SILVACO Internationals. The process parameters of the device were then optimized by utilizing L_{27} orthogonal array of Taguchi method in order to obtain the highest value of drive current (I_{ON}) and the lowest value of leakage current (I_{OFF}). The highest value of I_{ON}/I_{OFF} ratio after an optimization approach was observed to be 2.154×10^{12}.

Keywords: ANOVA; ATHENA; ATLAS; Taguchi

Abstrak

Pengecilan saiz peranti planar MOSFET amat terhad untuk dilaksanakan apabila ianya menhampiri teknologi 22nm nod. Dalam kajian ini, struktur Vertikal Double Gate MOSFET serta dinding silicon yang amat nipis diperkenalkan dengan mengekalkan silicon dioksida (SiO_2) dan polisilikon sebagai unsur-unsur utama. Struktur MOSFET yang dicadangkan dikenali sebagai peranti Ultrathin Pillar Vertical Double Gate (VDG) MOSFET dan ianya diintergrasikan dengan teknologi polysilicon-on-insulator (PSOI) untuk pencirian elektrik yang lebih baik. Proses fabrikasi and pencirian elektrikal secara simulasi telah dilaksanakan dengan mengunakan modul ATHENA and ATLAS daripada SILVACO Internationals. Parameter-paramter proses peranti tersebut dioptimasikan dengan mengunakan susunan ortogonal L_{27} kaedah Taguchi bagi mencapai nilai tertinggi I_{ON} dan nilai terendah I_{OFF}. Nilai nisbah tertinggi I_{ON}/I_{OFF} selepas pendekatan optimasi ialah 2.154×10^{12}.

Kata kunci: ANOVA; ATHENA; ATLAS; Taguchi

1.0 INTRODUCTION

Producing planar MOSFET devices with a very short channel length seems to be very challenging and complicated, especially for below the 22nm technology node. The reduction of MOSFET's size is always related to the deterioration of the device's characteristics. The most critical device's characteristics that are important to be preserved are known as drive current (I_{ON}) and leakage current (I_{OFF}). An attempt to reduce the physical gate (L_g) of conventional MOSFET device has resulted in a very close proximity between the drain region and the source region thereby introducing various short channel effects (SCE) problems. These SCEs lead to the increase of leakage current (I_{OFF}) which will deteriorate the device's performance [1]. A lot of researches have been done in order to circumvent SCE problems. One of them is to integrate the combination of high permittivity (high-k) dielectric material and metal gate into the MOSFET's structure [2]. However, in the current research, traditional silicon dioxide (SiO_2) and polysilicon material are still being used by introducing ultrathin pillar (UTP) polysilicon-on-insulator (PSOI) Vertical Double Gate (VDG) design architecture.

The drive current (I_{ON}) is defined as a drain to source current when $V_{GS}=V_{DD}$ and $V_{DS}=V_{DD}$ [3]. The drive current (I_{ON}) is regarded as a very important device's characteristic as it decides the driving capability of the MOSFET device. As the channel length becomes very short, short channel effects (SCEs) arise. Majority carrier transport in the active mode may become limited due to velocity saturation. When velocity saturation dominates, the drive current (I_{ON}) or saturation drain current (I_{DS}) is more nearly linear than quadratic in V_{GS} Hence, the drain-induced barrier lowering (DIBL) increases the off-state leakage current (I_{OFF}) and requires an increase in threshold voltage (V_{TH}) to compensate, which in turn reduces the drive current (I_{ON}) [4].

The leakage current (I_{OFF}) is defined as a drain to source current when $V_{GS}=0$ and $V_{DS}= V_{DD}$. The MOSFET's leakage current or off-state current (I_{OFF}) is the drain current when no gate voltage is applied [3]. Leakage current (I_{OFF}) is influenced by several other parameters such as channel physical dimensions, source/drain junction depth, thickness of gate oxide and channel doping profile. The ratio of total drive current (I_{ON}) to the leakage current (I_{OFF}) is an important device's characteristic to be considered. The I_{ON}/I_{OFF} current ratio represents the power consumption of a device [3]. The higher I_{ON}/I_{OFF} ratio is, the lower power consumption of a device will be.

This paper emphasizes on utilizing L_{27} orthogonal array of Taguchi method that consists of 13 process parameters which are substrate implantation dose, V_{TH} implantation dose, V_{TH} implantation energy, halo implantation energy, halo implantation tilt, source/drain (S/D) implantation dose, compensation implantation dose and etc. The gate oxide temperature and polysilicon oxidation temperature are selected as noise factors in order to get optimum results. The main objective of the current work is to obtain the possible highest value of I_{ON}/I_{OFF} ratio by maximizing the drive current (I_{ON}) value and minimizing the leakage current (I_{OFF}) value. Besides that, the threshold voltage (V_{TH}) value must be ensured to be within ±12.7% of low power (LP) multi-gate (MG) requirement in ITRS 2013 prediction (0.447V) for year 2020 [5].

2.0 MATERIALS AND METHODS

The virtual fabrication process of VDG-MOSFET device was simulated by using ATHENA and ATLAS modules of SILVACO International. ATHENA module was used for process simulation of the MOSFET's device. Meanwhile, ATLAS module was used for device simulation and electrical characterization.

2.1 Virtual Fabrication Process

The process initiated with the selection of a P-type silicon with <100> orientation as the main substrate. Next, 1 x 10^{14} atom/cm3 of boron was implanted into the silicon substrate. Buried oxide (BOX) of 16nm (t_{BOX}) was then developed. The silicon was etched by using the retarded etching technique in order to ensure the very thin pillar with diameter of 12nm (Lp) was well constructed. The ultrathin pillar was able to form a very sharp vertical channel that could tremendously increase the drive current (I_{ON}). The virtual process was followed by the gate oxidation process at temperature of 920° C. Since the device was a n-channel type, 9.81 x 10^{12} atoms/cm^3 of boron was implanted into the substrate in order to form p+ region.

After that, polysilicon material was deposited at the top of the gate oxide. Then, both polysilicon and polysilicon oxide were etched away to form a very thin gate with a diameter of 12nm (Lg). In order to optimize the performance of UTP PSOI VDG-MOSFET device, indium with a dosage of 1.33 x 10^{13} atom/cm^3 was doped at an energy level of 170 Kev and tilt angle of 24°. Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were then used as a mask for source/drain implantation. An arsenic atom with concentration of 1.25 x 10^{20} atom/cm^3 was implanted in order to supply free electron to form a n+ region as conductive channel.

Compensation implantation was utilized later by implanting phosphor dosage of 2.51 x 10^{12} atoms/cm^3 with an energy level of 63 Kev and tilt angle of 7°. This step is taken in order to reduce parasitic effects that could increase the leakage current (I_{OFF}). Next, silicide (CoSi) was formed at the top of the source and drain region by sputtering cobalt on silicon surface. This transistor was then connected with aluminum metal. The aluminum layer

was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [6-7]. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. The final structure of VDG-MOSFET device was completed by mirroring the right-hand side structure. The completed structure of VDG-MOSFET device is illustrated as in Figure 1.

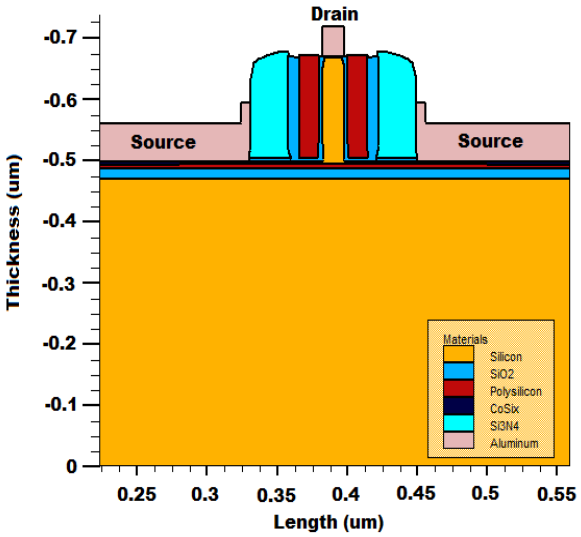


Figure 1 Structure of Vertical DG-MOSFET device with PSOI Technology

2.2 Taguchi L_{27} Orthogonal Array Method

In the current research, Taguchi L_{27} orthogonal array is developed in order to investigate the impact of thirteen process parameters variation on I_{ON}/I_{OFF} ratio. The target value of I_{ON}/I_{OFF} ratio is expected to be as high as possible. The higher value of I_{ON}/I_{OFF} ratio is, the lower power consumption of the device will be. Therefore, a total of 108 runs are required to optimize the process parameters in VDG-MOSFET device. All the values of process parameters and noise factors with their corresponding levels are listed in Table 1 and Table 2 respectively.

Table 1 Process Parameters and Their Levels

Sym	Process Parameter	Units	Level 1	Level 2	Level 3
A	Substrate Implantation Dose	atom/cm³	1E14	1.03E14	1.06E14
B	V_{TH} Implantation Dose	atom/cm³	9.81E12	9.84E12	9.87E12
C	V_{TH} Implantation Energy	kev	20	21	22
D	V_{TH} Implantation Tilt	degree	7	10	13
E	Halo Implantation Dose	atom/cm³	2.61E13	2.64E13	2.67E13
F	Halo Implantation Energy	kev	170	172	174
G	Halo Implantation Tilt	degree	24	27	30
H	S/D Implantation Dose	atom/cm³	1.22E20	1.25E20	1.28E20
J	S/D Implantation Energy	kev	43	45	47
K	S/D Implantation Tilt	degree	80	83	86
L	Compensation Implant Dose	atom/cm³	2.51E12	2.54E12	2.57E12
M	Compensation Implant Energy	kev	60	62	64
N	Compensation Implant Tilt	degree	7	10	13

Table 2 Noise Factors and Their Levels

Sym.	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temperature	C	920	923
V	Polysilicon Oxidation Temperature	C	870	873

3.0 RESULTS AND DISCUSSION

After the VDG-MOSFET device was virtually fabricated by using ATHENA module, the electrical characterization of the device was then simulated by using ATLAS module. Next, L_{27} orthogonal array of Taguchi method was implemented to acquire the highest possible value of drive current (I_{ON}) and the lowest possible value leakage current (I_{OFF}). Later, the comparative analysis was conducted in order to select the highest percentage of factor effect as the best optimum setting of I_{ON}/I_{OFF} ratio.

3.1 Characterization of VDG-MOSFET device

Figure 2 shows the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05V and V_D = 1.0V for VDG-MOSFET device. The value of off-leakage current (I_{OFF}) and drive current (I_{ON}) were extracted from the graph.

From the graph, it was observed that the value of drive current (I_{ON}) was 726.4 µA/µm. The high drive current (I_{ON}) was desired in achieving high speed transition from "ON" to "OFF" state or vice-versa. Meanwhile, the off-leakage current (I_{OFF}) was observed to be 1.253E-15 A/µm. A very low leakage

current (I_{OFF}) indicates a better suppression of the short channel effect (SCE) problems. Finally, the initial value of I_{ON}/I_{OFF} ratio was calculated by using (1) [3]:

$$I_{ON} / I_{OFF} Ratio = \frac{I_{ON}}{I_{OFF}} \quad (1)$$

The initial value of I_{ON}/I_{OFF} ratio was observed to be 5.797E11. The I_{ON}/I_{OFF} ratio was the desired electrical response to be optimized by utilizing Taguchi method.

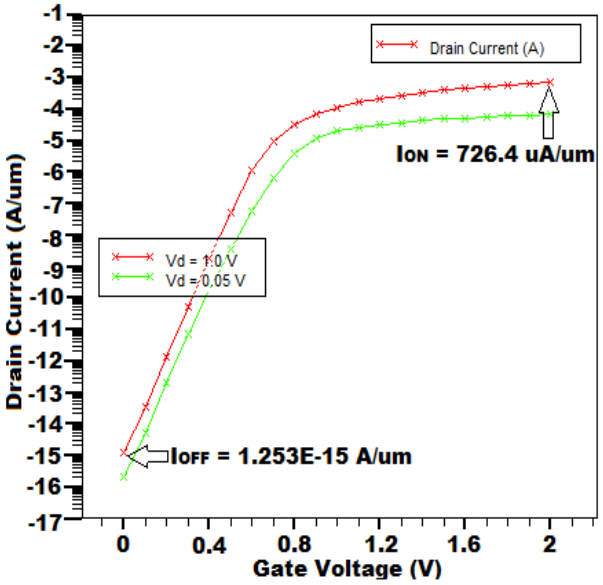


Figure 2 Graph of subthreshold drain current (I_D) versus gate voltage (V_G)

3.2 Signal-to-noise Ratio (SNR) Analysis

Before an attempt to maximize I_{ON}/I_{OFF} ratio of VDG-MOSFET device was performed, the values of drive current (I_{ON}) and leakage current (I_{OFF}) were first to be optimized. This was because the signal-to-noise ratio (SNR) analyses for both drive current (I_{ON}) and leakage current (I_{OFF}) fell into different categories. The SNR analysis of the drive current (I_{ON}) was categorized in higher-the-better type. For leakage current (I_{OFF}), the SNR analysis was categorized in lower-the better type.

The L27 orthogonal array analysis of both output responses, drive current (I_{ON}) and leakage current (I_{OFF}) were simulated and recorded. After retrieving the results for both drive current (I_{ON}) and leakage current (I_{OFF}), the process parameters of VDG-MOSFET device was then statistically modelled by using Taguchi method. Taguchi method was assigned to analyze the drive current (I_{ON}) values using SNR analysis of the Higher-the-better. The SNR (Higher-the-better), ηHTB can be expressed as [8]:

$$\eta_{HTB} = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n}\frac{1}{y_i^2}\right] \quad (2)$$

Meanwhile, analysis for leakage current (I_{OFF}) was implemented using SNR analysis of Lower-the better. The SNR (Lower-the-better), η_{LTB} can be expressed as [8]:

$$\eta_{LTB} = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n}y_i^2\right] \quad (3)$$

where *n* is the number of tests and *yi* is the experimental values of subthreshold swing (SS). By utilizing formula given in (2), the SNR for each row of experiments were computed and recorded in Table 3.

Table 3 SNR for I_{ON} and I_{OFF} in VDG-MOSFET Device

Exp. no	SNR (dB)	
	Drive Current, I_{ON} (Higher-the-better)	Leakage Current, I_{OFF} (Lower-the-better)
1	57.00	299.54
2	56.98	295.87
3	57.13	286.83
4	57.07	300.15
5	56.99	294.17
6	57.26	283.52
7	57.04	297.46
8	57.07	293.91
9	57.24	280.66
10	57.44	275.51
11	56.96	299.97
12	56.96	296.97
13	57.46	276.29
14	56.75	302.26
15	56.80	301.28
16	57.42	279.52
17	56.80	300.48
18	56.87	302.52
19	57.12	292.54
20	57.34	277.44
21	56.83	304.37
22	57.09	294.19
23	57.37	283.36
24	56.74	302.69
25	57.11	292.67
26	57.36	280.21
27	56.69	305.52

Based on Table 4, the factor effects graph for SNR (Higher-the-better) and SNR (Lower-the-better) were plotted as illustrated in Figure 3 and Figure 4 respectively. The dashed horizontal lines in both graphs represent the overall mean of SNR (Higher-the-better) and SNR (Lower-the-better) which were 57.07 dB and 292.59 dB. From Figure 3, it was observed that factor A1, B1, C2, D3, E1, F1, G3, H2, J3, K1, L3, M1 and N1 have been selected as the optimum value for drive current (ION) due to their highest SNR. Meanwhile, Fig. 4 indicates that factor A2, B2, C1, D1, E3, F1, G1, H3, J2, K1, L1, M3 and N3

were the most optimum value for leakage current (I_{OFF}).

Table 4 SNR of Process Parameters in VDG-MOSFET Device

Process Parameter	Output Response	SNR Level 1	SNR Level 2	SNR Level 3	Total Mean SNR
A		57.09	57.05	57.07	
B		57.09	57.06	57.07	
C		57.05	57.09	57.07	
D		57.03	57.08	57.10	
E		57.20	57.07	56.95	
F		57.10	57.07	57.05	
G	I_{ON}	56.88	57.00	57.33	57.07
H		57.07	57.08	57.07	
J		57.07	57.07	57.08	
K		57.11	57.07	57.03	
L		57.06	57.07	57.09	
M		57.08	57.07	57.07	
N		57.08	57.07	57.06	
A		292.46	292.75	292.56	
B		292.12	293.10	292.55	
C		293.89	292.08	291.80	
D		293.39	292.75	291.63	
E		289.76	291.96	296.04	
F		293.21	291.98	292.57	
G	I_{OFF}	301.38	296.01	280.37	292.59
H		292.19	292.51	293.07	
J		292.54	292.71	292.52	
K		292.90	292.32	292.54	
L		292.90	292.27	292.60	
M		291.21	292.88	293.68	
N		292.66	292.44	292.66	

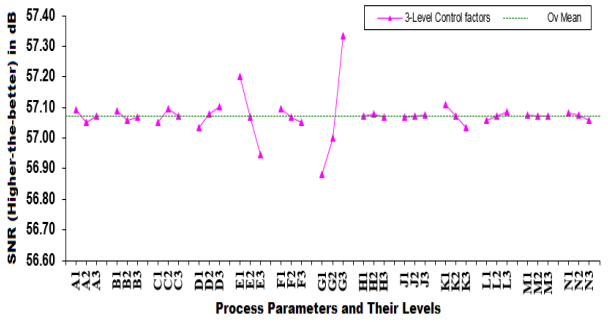


Figure 3 Factor effect plot for SNR (Higher-the-better) for I_{ON}

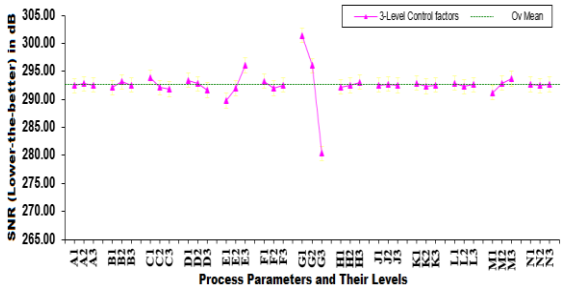


Figure 4 Factor effect plot for SNR (Lower-the-better) for I_{OFF}

3.3 Analysis of Variance (ANOVA)

The common practical method in investigating the relative effect of different process parameters on both drive current (I_{ON}) and leakage current (I_{OFF}) was realized by decomposition of variance which was called analysis of variance (ANOVA) [9]. The results of ANOVA for both drive current (I_{ON}) and leakage current (I_{OFF}) in VDG-MOSFET device are listed in Table 5. F-test was statistically conducted in order to provide a decision at some confidence level to determine the significance of certain process parameters. A larger F-value implies that the variation of certain process parameter has contributed a large effect on the device performance [10].

Table 5 Results of ANOVA

Process Parameters	Output Response	Degree of Freedom (DF)	Sum of Square (SSQ)	Mean Square (MS)	F-value	Factor effect on SNR (%)
A		2	0	0	-	0.50
B		2	0	0	-	0.33
C		2	0	0	-	0.65
D		2	0	0	-	1.56
E		2	0	0	38	21.00
F		2	0	0	-	0.68
G	I_{ON}	2	1	0	131	72.88
H		2	0	0	-	0.03
J		2	0	0	-	0.01
K		2	0	0	-	1.88
L		2	0	0	-	0.26
M		2	0	0	-	0.01
N		2	0	0	-	0.20
A		2	0	0	-	0.02
B		2	4	2	-	0.18
C		2	23	12	-	0.96
D		2	14	7	-	0.59
E		2	183	91	24	7.57
F		2	7	3	-	0.28
G	I_{OFF}	2	2145	1072	278	88.92
H		2	4	2	-	0.15
J		2	0	0	-	0.01
K		2	2	1	-	0.06
L		2	2	1	-	0.07
M		2	28	14	-	1.18
N		2	0	0	-	0.01

At least 95% confidence

According to Table 5, the most dominant process parameters with respect to drive current (I_{ON}) were observed to be process parameter E (21%) and G (72.88%). For leakage current (I_{OFF}), process parameter E with contribution effect on SNR of 7.57% was considered to be a significant process parameter. Meanwhile, process parameter, G with contribution effect on SNR of 88.92% was considered to be a dominant process parameter. The level of each dominant and significant process parameters are not recommended to be changed due to their

large influence on device characteristics. The remaining process parameters were recognized as neutral as they did not have much effect on both drive current (I_{ON}) and leakage current (I_{OFF}) values. Both process parameters, E and G represent halo implantation dose and halo implantation tilt respectively.

3.4 Comparative Analysis of Process Parameter Effect on SNR for I_{ON} and I_{OFF}

In order to obtain the overall best setting that satisfy both drive current (I_{ON}) and leakage current (I_{OFF}), some comparative analysis of process parameter effects on SNR has to be implemented. The best level setting of each process parameter was obtained by selecting the highest process parameter effect on SNR. Table 6 shows the level of each process parameters and their corresponding process parameter effects on SNR.

Table 6 Process Parameters and Their Effects on SNR

Process Parameter	Drive Current (I_{ON})		Leakage Current (I_{OFF})		Overall Best Setting
	Level	Process Parameter Effect on SNR (%)	Level	Process Parameter Effect on SNR (%)	
A	1	0.50	2	0.02	A1
B	1	0.33	2	0.18	B1
C	2	0.65	1	0.96	C1
D	3	1.56	1	0.59	D3
E	1	21.00	3	7.57	E1
F	1	0.68	1	0.28	F1
G	3	72.88	1	88.92	G1
H	2	0.03	3	0.15	H3
J	3	0.01	2	0.01	J2
K	1	1.88	1	0.06	K1
L	3	0.26	1	0.07	L3
M	1	0.01	3	1.18	M3
N	1	0.20	3	0.01	N1

From Table 6, it can be observed that the best level setting of process parameter was determined by comparing the percentage of process parameter effect on SNR between drive current (I_{ON}) and leakage current (I_{OFF}). The level of output response that possesses the highest percentage process parameter effect on SNR will be selected as the overall best setting. For instance, process parameter, A1 had a higher percentage of process parameter effect on SNR (0.50%) than process parameter A2 (0.02%), hence this process parameter A1 was selected as the overall best setting. The same procedure was applied to the other process parameters. As a result, process parameter, A1, B1, C1, D3, E1, F1, G1, H3, J2, K1, L3, M3 and N1 have been identified as the overall best setting for both drive current (I_{ON}) and leakage current (I_{OFF}).

4.0 CONFIRMATION TEST

Confirmation run is the final step in the design of experiment (DoE) process. The main purpose of the confirmation run is to validate the results retrieved during analysis phase [6,8]. Confirmation run was performed by conducting an actual simulation test using the overall best level setting of process parameters as statistically predicted earlier. Table 7 shows the overall best setting of process parameters in VDG-MOSFET device.

Table 7 Best Combination Level of Process Parameters

Symbol	Process Parameter	Units	Best Value
A	Substrate Implantation Dose	atom/cm^3	1E14
B	V_{TH} Implantation Dose	atom/cm^3	9.81E12
C	V_{TH} Implantation Energy	kev	20
D	V_{TH} Implantation Tilt	degree	13
E	Halo Implantation Dose	atom/cm^3	2.61E13
F	Halo Implantation Energy	kev	170
G	Halo Implantation Tilt	degree	24
H	S/D Implantation Dose	atom/cm^3	12.8E18
J	S/D Implantation Energy	kev	45
K	S/D Implantation Tilt	degree	80
L	Compensation Implantation Dose	atom/cm^3	2.57E12
M	Compensation Implantation Energy	kev	64
N	Compensation Implantation Tilt	degree	7

The value of SNR (Higher-the-better) of the drive current (I_{ON}) for VDG-MOSFET device was observed to be 57.01 dB and still within the predicted range of 56.93 dB to 57.09 dB. On the other hands, the value of SNR (Lower-the better) of leakage current (I_{OFF}) was observed to be 298.56 dB. The SNR (Lower-the-better) value was still within the predicted range of 295.9 dB to 301.22 dB. The confirmation run was then conducted by utilizing ATHENA and ATLAS module. The electrical characteristic results of the confirmation run are listed in Table 8.

The highest I_{ON}/I_{OFF} ratio obtained was observed to be 2.154E12 where the optimum noise factor was 923° C for gate oxidation temperature and 873° C for polysilicon oxidation temperature as shown in Table 8. On the other hands, the values of threshold voltage (V_{TH}), drive current (I_{ON}) and leakage current (I_{OFF}) were observed to meet the ITRS 2013 prediction for low power (LP) requirement. Meanwhile, the subthreshold swing (SS) value was observed to be in

the range of 60 to 65 mV/dec. The maximum value of I_{ON}/I_{OFF} ratio was successfully achieved by using Taguchi method along with nominal threshold voltage (V_{TH}) of 0.437 V (±12.7% of 0.447 V), high drive current (I_{ON}) of 701.9 µA/µm (≥ 533 µA/µm) and low leakage current (I_{OFF}) of 3.258E-16 A/µm (≤ 20 ρA/µm) [5].

Table 8 Result of Electrical Characteristics in VDG-MOSFET Device

Electrical Characteristics	Noise Factors Combination			
	U1V1	U1V2	U2V1	U2V2
I_{ON} (µA/µm)	730.6	722.2	708.5	701.9
I_{OFF} (A/µm)	9.349E-16	1.018E-15	9.207E-16	3.258E-16
I_{ON}/I_{OFF} Ratio	7.815E+11	7.092E+11	7.69E+11	2.154E+12
V_{TH} (V)	0.404	0.415	0.422	0.437
SS (mV/dec)	63.63	63.71	63.85	63.66

The comparison of the optimal result of I_{ON}/I_{OFF} ratio value was also compared to the previous result of other researches. Table 9 shows the comparison of the optimal I_{ON}/I_{OFF} value of VDG-MOSFET device with the value before the optimization approach and the value of previous researches. It can be observed that there was a slight improvement of the I_{ON}/I_{OFF} ratio value in vertical DG-MOSFET device when the Taguchi method was applied for optimization purpose.

Table 9 Comparison of the Optimal I_{ON}/I_{OFF} ratio Value with the Previous Researches

I_{ON}/I_{OFF} ratio			
Results from this work (Before optimization)	Results from this work (After optimization)	Results from Atan et al. (2014) [11]	Results from Chaudary & Khanna(2014) [12]
5.797E11	2.154E12	1.326E12	0.84E12

5.0 CONCLUSION

In conclusion, the highest possible value of I_{ON}/I_{OFF} ratio in VDG-MOSFET device was successfully predicted and designed by utilizing combination of SILVACO International simulation software and Taguchi method. After the ideal recipe for the device has been found, Taguchi modeling was then implemented. Taguchi method was preferred to be an optimization tool for VDG-MOSFET device due to its capability of predicting which process parameters would contribute the most significant impact on both drive current (I_{ON}) and leakage current (I_{OFF}) with less number of experiments. The level of significance of each input process parameter on both I_{ON} and I_{OFF} was determined by using ANOVA. Based on the ANOVA method, halo implantation dose and halo implantation tilt have been recognized as the most significant process parameters for both drive current (I_{ON}) and leakage current (I_{OFF}). The maximum value of I_{ON}/I_{OFF} ratio was observed to be 2.154E12 with nominal threshold voltage (V_{TH}) of 0.437 V (±12. 7% of 0.447 V), high drive current (I_{ON}) of 701.9 µA/µm, low leakage current (I_{OFF}) of 3.258 x 10^{-16} A/µm and ideal subthreshold swing of 63.66 mV/dec. All of these values are well within the predicted range of ITRS 2013 for low power (LP) multi-gate (MG) technology requirement in the year 2020. A very high I_{ON}/I_{OFF} ratio indicates a better power consumption of the device. Thus, a L_{27} orthogonal array of Taguchi method was observed to be an effective tool in maximizing I_{ON}/I_{OFF} ratio in VDG-MOSFET device.

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