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STUDY OF ELECTRICAL CHARACTERISTIC FOR 50NM AND 10NM SOI BODY THICKNESS IN MOSFET DEVICE

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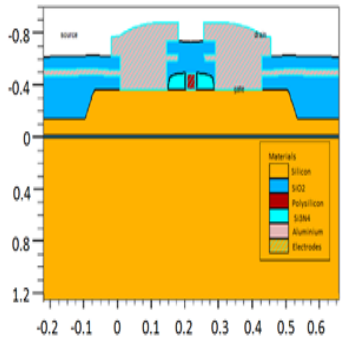
Graphical abstract



Abstract

Silicon-on-insulator (SOI) technology is an effective approach of mitigating the short channel effect (SCE) problems. The SOI is believed to be capable of suppressing the SCE, thereby improving the overall electrical characteristics of MOSFET device. SCE in SOI MOSFET is heavily influenced by thin film thickness, thin-film doping density and buried oxide (BOX) thickness. This paper will analyze the effect of BOX towards SOI MOSFET device. The 50nm and 10nm thickness of buried oxide in SOI MOSFET was developed by using SILVACO TCAD tools, specifically known as Athena and Atlas modules. From the observation, the electrical characteristic of 100nm thickness is slightly better than 50nm and 10nm. It is observed that the value drive current of 10nm and 100nm thickness SOI MOSFET was 6.9% and 11% lower than 50nm respectively, but the overall 50nm is superior. However, the electrical characteristics of 10nm SOI MOSFET are still closer and within the range of ITRS 2013 prediction.
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Keywords: MOSFET, Silvaco, drive current, SOI

Abstrak

Silikon pada penebat (SOI) ialah satu pendekatan berkesan mengurangkan masalah kesan saluran pendek (SCE). SOI dipercayai akan mampu menghalang SCE, sekaligus meningkatkan ciri-ciri keseluruhan peranti MOSFET. SCE di dalam SOI MOSFET dipengaruhi oleh ketebalan filem nipis, ketumpatan doping filem nipis and ketebalan oksida yang tertanam (BOX). Kertas kerja ini akan menganalisis kesan ketebalan BOX terhadap peranti SOI MOSFET. Ketebalan 10nm, 50nm and 10nm oksida yang tertanam dalam SOI MOSFET telah dihasilkan dengan menggunakan peralatan SILVACO TCAD, khususnya dikenali sebagai modul Athena dan Atlas. Dari pemerhatian yang dibuat, ciri elektrik bagi ketebalan 100nm adalah lebih baik sedikit daripada 50nm dan 10nm. Adalah diperhatikan bahawa nilai arus pacu bagi ketebalan 10nm and 100nm SOI MOSFET ialah 6.9% dan 11% lebih rendah dari 50nm tetapi secara keseluruhan 50nm lebih baik. Bagaimanapun, ciri-ciri elektrik bagi 10nm SOI MOSFET masih dalam julat dan menghampiri ramalan ITRS 2013.

Kata kunci: MOSFET, Silvaco, arus pacu, SOI

1.0 INTRODUCTION

Silicon-on-insulator MOSFET development has improved a lot lately with a lot of researchers trying to improve this technology with a new approach. Silicon-on-insulator, or known as SOI, is now not limited to single gate but now it will be implanted in double gate and maybe triple gate later. The history

of SOI MOSFET can be traced back from 80 years ago when J.E Lilienfield introduced a first field effect concept called method and apparatus for controlling electric current [1-2]. The researcher stated on his concept that there are three terminal devices where the source to drain current is controlled by a field effect from the gate and is dielectrically insulated from the rest of the device. The active part of the device was built on a thin semiconductor film, which is deposited on an insulator. Remarkably, this first proposed FET concept was indeed an introduction of SOI MOSFET, but due to lack of equipment and technologies, this concept has long been forgotten until the development of SIMOX or known as implanted oxygen technology in 1966 [3-5]. The main route for this silicon on insulator technology is using silicon dioxide (SiO2) as the main material. Short channel effect (SCE) was the main problem in MOSFET device when it comes to downscaling the thickness of the body or Ultra-thin Body (UT). Short channel effect (SCE) happens when the barrier of electron injection is accidently reduced due to the effective channel length (Leff) becoming too short [4-7]. This SCE can lead to several problems such as a shift of threshold voltage when the channel length is shortened and lack of pinch off. Furthermore, SCE might be able to reduce the controllability of gate voltage and drain current, thus increasing drain-off current and degradation of subthreshold slope. Therefore, SOI MOSFET architecture has been introduced to reduce the short channel effect (SCE). Although the SOI MOSFET architecture is not able to completely eliminate the short channel effect (SCE), it still has a better performance than the conventional bulk MOSFET device. Most of SCE in SOI MOSFET device was influenced by thin film thickness, thin-film doping density, substrate biasing and buried oxide thickness [8]. This paper attempts to investigate the effects of buried oxide thickness on SOI MOSFET device.

2.0 EXPERIMENT

The process and device simulations of SOI MOSFET used ATHENA and ATLAS modules of SILVACO TCAD tool respectively. Figure 1 shows the procedure of SOI MOSFET design structure. In this procedure, the substrate is prepared for further processing. The process simulation of SOI MOSFET device requires a series of processing steps called a process flow. The process modules start with wafer preparation, followed by well formation, isolation formation, transistor making and interconnection as shown in Figure 1.

2.1 Designing SOI MOSFET Device

Firstly, the main substrate, which is P-type silicon with <100> orientation, has been used, followed by Buried Oxide Layer (BOX) formation. 200Å oxide layer was grown on top of silicon bulk. This oxide layer is important as it has been used as a mask during P-well implantation process. After doping process was completed, the oxide layer has been etched and it was followed by annealing process. The function of annealing process is to strengthen the device's structure.

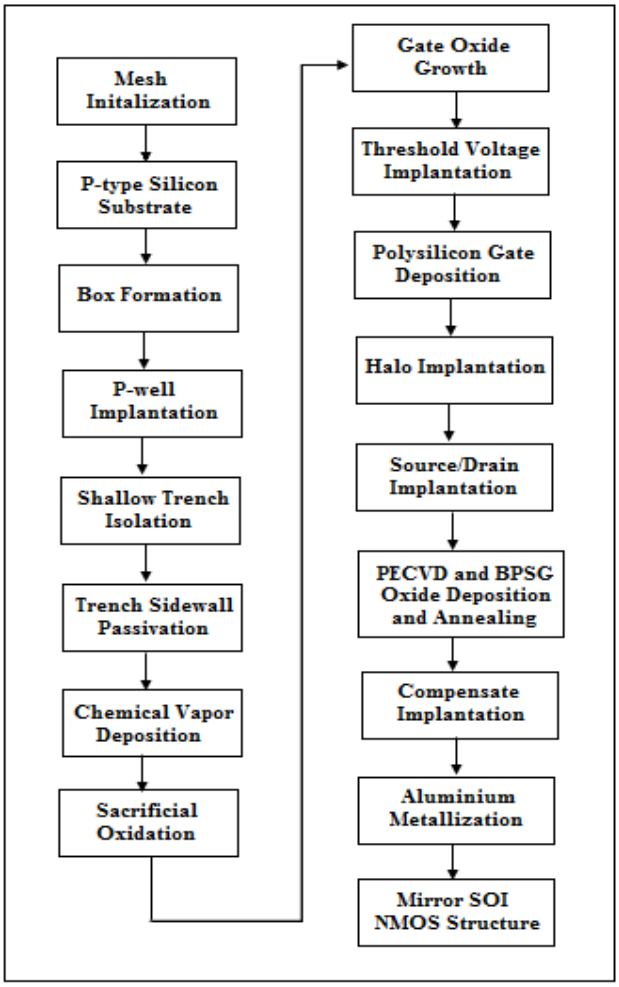

Figure 1 SOI Design Structure

After that, shallow trench isolation (STI) was conducted in order to isolate the neighbour transistor. A 130Å stress buffer has been applied on the wafers with 25 min diffusion processes. LPCVD process or known as Low-Pressure Chemical Vapour Deposition was used to deposit a 1350Å nitride layer. The purpose of nitride layer was to act as a mask when silicon was etched to expose the STI area. Photo resistor layer was then deposited on the wafer layer and any unwanted parts were etched away using the Reactive Ion Etching (RIE) process. The main purpose of oxide layer grown on the trench sides was to eliminate impurity from entering the silicon substrate. After that, to eliminate extra oxide on the wafer, the chemical Mechanical polishing (CMP) was applied. A sacrificial oxide layer was then grown and

etched to eliminate any defects on the surface. The gate oxide must be grown before the Boron Difluoride (BF2) threshold-adjustment process. The polysilicon gate was then deposited and followed by halo implantation. The polysilicon was etched accordingly to form a gate structure. For 40nm node technology, the gate and channel lengths of this device is 23nm and 18nm respectively [11]. To get a better and optimum performance for SOI MOSFET device, indium was doped. Sidewall spacer was then deposited to a mask for source/drain implantation. Arsenic was implanted with an appropriate value of concentration to get smooth current flow in NMOS device. After that, the silicide layer was developed and annealed at the top of polysilicon.

The next stage is to deposit Boron Phospor Silicate Glass (BPPG) layer. This layer was a Premetal dielectric (PMD), which is the first layer deposited in the wafer surface when transistor was produced. The transistor was then connected to aluminium metal. After that, the second aluminium layer was deposited on top of the Intel-Metal Dielectric (IMD) and unwanted aluminium was etched to create the contacts [8-10]. The step was completed when etching and metallization was performed for electrode formation and bonding pads were opened.

3.0 RESULTS AND DISCUSSION

There are three designs that will be introduced in this paper, namely 10nm SOI MOSFET, 50nm SOI MOSFET and 10nm SOI MOSFET. These three designs are actually developed using the same architecture. The only difference is the thickness of buried oxide (BOX). This BOX thickness was varied within certain depth. After the designs of these three MOSFETs were completed, the electrical characteristics of these devices were studied and investigated. The electrical characteristics that have been observed are known as Leakage current (I_{OFF}), Drive current (I_{ON}) and Sub-threshold voltage swing (S_S).

3.1 Structure Of 100nm, 50nm And 10nm SOI MOSFET Thickness

Figure 2 shows the structure of SOI MOSFET with 100nm thickness of BOX layer. Meanwhile, Figure 3 and Figure 4 clearly show the structure of 50nm and 10nm SOI MOSFET. These three MOSFET contain silicon, silicon dioxide, polysilicon, silicon nitride, cobalt nitride and aluminium. One of the significant factors that affect electrical characteristics is doping concentration.

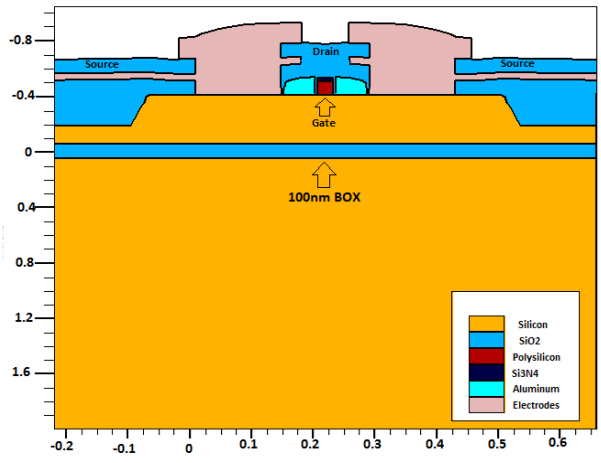

Figure 2 100nm SOI MOSFET

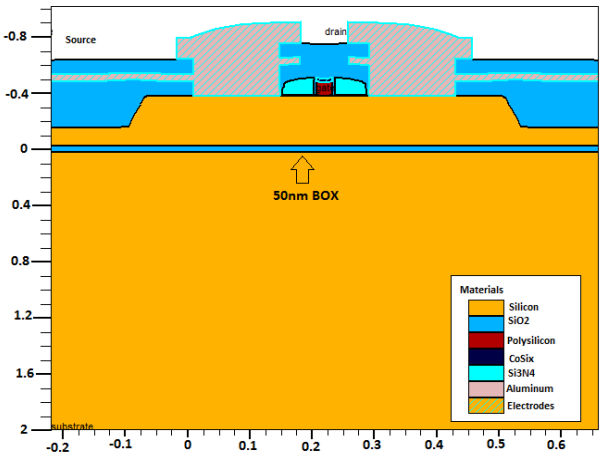

Figure 3 50nm SOI MOSFET

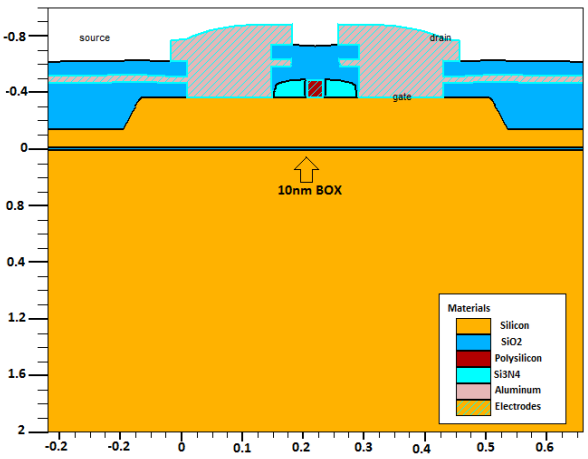

Figure 4 10nm SOI MOSFET

3.2 Electrical Characteristics Of 100nm, 50nm And 10nm SOI MOSFET

Figure 5 shows the I_D-V_D characteristic for different gate voltages (V_G) in 50nm SOI MOSFET. Gate voltage with three different values have been swapped to observe the relationship of drain current (I_D) and gate voltage (V_G). These values are 0.05V, 0.1V, and 1.0V. Based on the graph, it was examined that the drain current (I_D) was proportional to gate voltage (V_G). Drain current increases when the value of gate voltage increases and it can be concluded that this design exhibits I_D-V_{DS} characteristics for SOI MOSFET device [12].

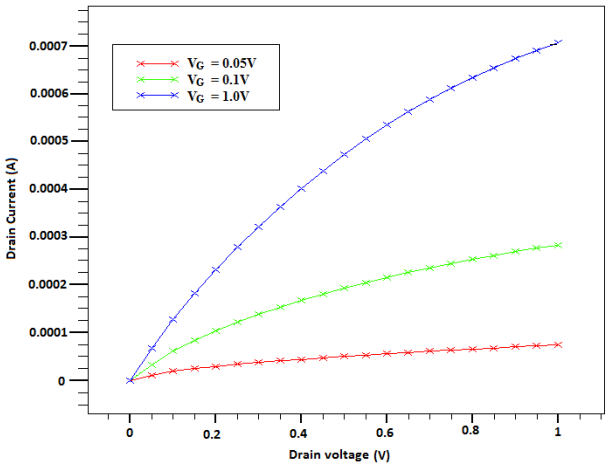

Figure 5 Graph I_D-V_D of 50nm SOI MOSFET

It was observed that the value of threshold voltage for this 50nm Buried oxide thickness is closer to the value of 0.289V of ITRS 2013 value [10]. Figure 6 indicates the level of I_{ON} and I_{OFF} for 50nm SOI MOSFET.

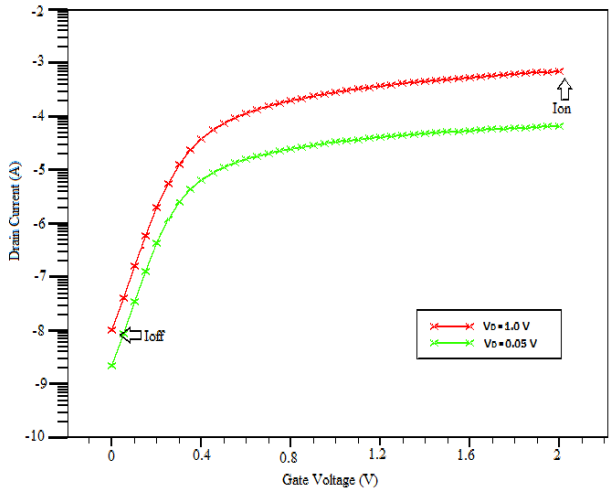

Figure 6 I_{ON} and I_{OFF} level for 50nm SOI MOSFET

Ideally, the transistor that is most needed is equipped with a high drive current and low sub-threshold voltage swing. This is needed to improve the switching speed of SOI MOSFET device. Meanwhile, Figure 7 clearly shows the value of electrical characteristics possessed by 50nm SOI MOSFET. It can be seen that the value of I_{OFF} of this SOI MOSFET is 10.64pA/μm while the value of I_{ON} is 707.48μA/μm. The sub-threshold (Sub_{VT}) swing is also displayed in Figure 7 with the value of 82.96mV/decade.

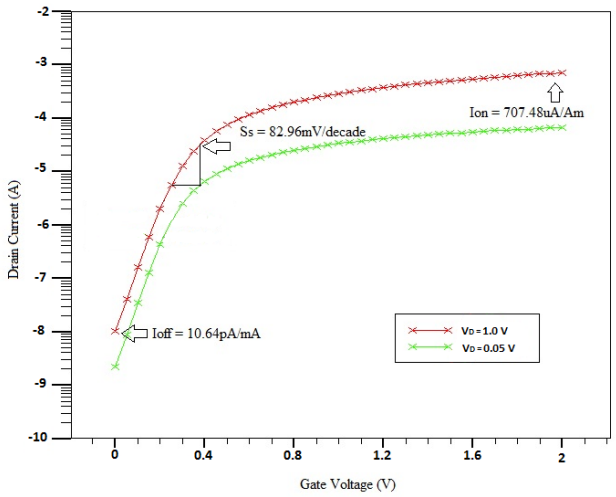

Figure 7 Electrical characteristic value of 50nm SOI MOSFET

Figure 8 shows the graph I_D versus V_D for 10nm SOI MOSFET device. This graph indicates the true behavior of MOSFET device on how the drain current saturates when it reaches the threshold value.

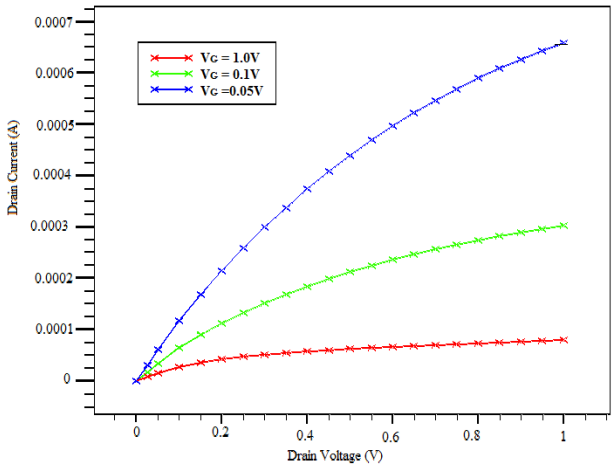

Figure 8 Graph I_D-V_D of 10nm SOI MOSFET

Figure 9 shows the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05V and V_D = 1.0V for 10nm SOI MOSFET device. The value of off-leakage current (I_{OFF}), drive

current (I_{ON}) and subthreshold swing (SS) can be extracted from the graph. From the graph, it was observed that the value of drive current (I_{ON}) was at 658.29μA/μm. The high drive current (I_{ON}) is needed for high speed switching operation. Meanwhile, the off-leakage current (I_{OFF}) was observed to be at 25.86pA/μm. A very low leakage current (I_{OFF}) will enhance the device's performance as it boosts the drive current (I_{ON}). The value of subthreshold swing (SS) for this structure is 85.59mV/decade. The initial value of subthreshold swing (SS) was extracted by using Equation (1) [8]:

$$SS = \left[\frac{dV_{GS}}{d(\log_{10} I_{DS})}\right] \quad (1)$$

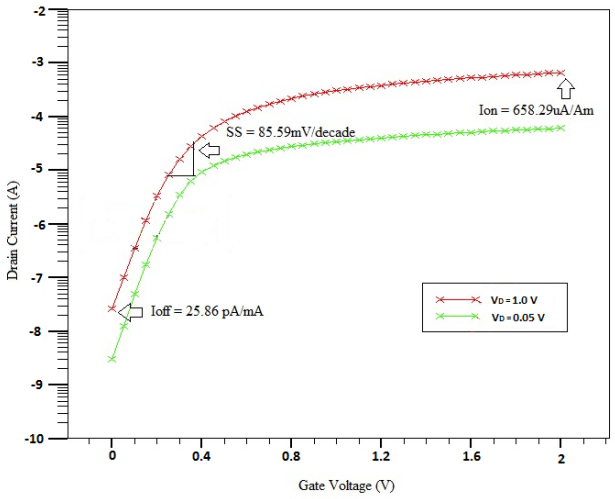

Figure 9 Electrical characteristic value of 10nm SOI MOSFET

Figure 10 shows the graph of 100nm SOI MOSFET between I_D versus V_G. The graph indicates the level of I_{ON} and I_{OFF} of 100nm SOI MOSFET. Then, the value of I_{ON} and I_{OFF} will be exracted from the graph. On the other hand, Figure 11 shows completely the value of three electrical characteristics, which are I_{ON}, I_{OFF} and S_S. The value of drive current (I_{ON}) in this particular SOI thickness was at 628.40μA/μm. Meanwhile, the off-leakage current (I_{OFF}) was observed to be at 3.364pA/μm. With these two values, the I_{ON}/I_{OFF} ratio was high to ensure the best performance of a SOI MOSFET device.

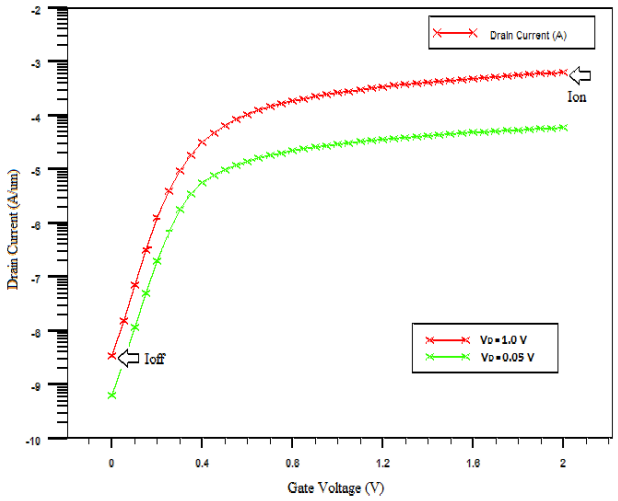

Figure 10 I_{ON} and I_{OFF} level for 100nm SOI MOSFET

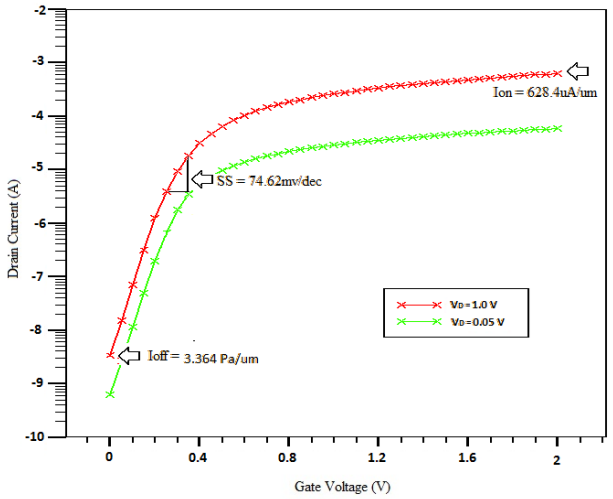

Figure 11 Electrical characteristic value of 100nm SOI MOSFET

Figure 12 shows the overlay graph Gate Voltage (V_G) versus Drain Current (I_D). It clearly shows that the value of I_{ON} for 100nm, 50nm and 10nm SOI MOSFET is 628.40μA/μm, 707.48μA/μm and 658.29μA/μm respectively. For I_{OFF} and subthreshold swing values, the difference between 100nm, 50nm and 10nm is not major. These values are still closer and within the range of ITRS 2013. Based on the analysis, it can be seen that both of them have a good transition between off and on states.

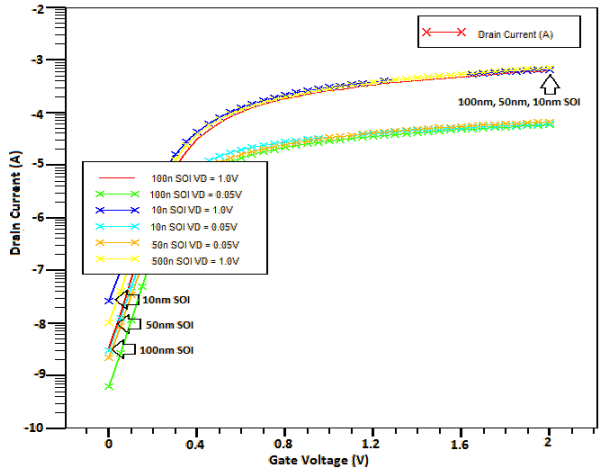

Figure 12 Overlay of 50nm and 10nm SOI MOSFET

Table 1 shows specifically the value of four electrical values that have been measured for 100nm, 10nm and 50nm SOI MOSFET devices. The minimum value of subthreshold swing (SS) was successfully achieved along with nominal threshold voltage (V_{TH}) of 0.289 V (±12.7% of ITRS 2013 prediction), very low leakage current (I_{OFF}) and high I_{ON}/I_{OFF} ratio. A very high I_{ON}/I_{OFF} ratio indicates the low power consumption of the device. The main reason why the performance of 50nm BOX device is slightly better than 10nm is the thickness of depletion layer. The 50nm BOX device generates a thicker depletion layer than the 10nm BOX device where the majority charge carriers in the channel region are trapped inside the region [11]. The thick depletion layer prevents the carriers from penetrating the source and drain region, thereby decreasing the leakage current.

Table 1 Electrical characteristics of 50nm and 10nm SOI MOSFET

Parameter	50nm	10nm	100nm	ITRS 2013 [11]
I_{ON} (µA/µm)	707.48	658.29	628.40	> 643 (multigate) >490 (Bulk MOSFET)
I_{OFF} (pA/µm)	10.64	25.86	3.34	< 10 (multigate) < 20 (Bulk MOSFET)
S_S (mV/dec)	82.96	85.59	74.62	60-100
V_{TH} (V)	0.2887	0.2896	0.2901	(0.289 ±12.7%)
I_{ON}/I_{OFF} ratio	66.49 x10⁶	65.83 x10⁶	188.14 x10⁶	

4.0 CONCLUSION

This report concentrates on the study of electrical characteristics of SOI MOSFET by varying the thickness of the Buried Oxide layer. These values were compared to ITRS 2013 prediction in order to ensure the values were within the predicted range. Based on the results, the 10nm device performance is slightly lower than 50nm device but 50nm device is less superior than 100nm device. The thick depletion layer prevents the carriers from penetrating the source and drain region, thereby decreasing the leakage current. However, the results of 10nm and 50nm SOI MOSFET device are still closer and within the range of ITRS 2013 prediction.

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