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ANALYSIS OF POWER CONSUMPTION SAR-ADC DYNAMIC COMPARATOR

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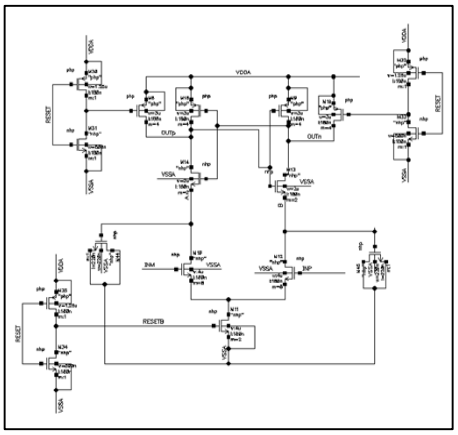

Abstract

Due to the high demand of ultra-low power in digital application, the needs of energy efficient analog-to-digital converter (ADC) are really essential. The comparator being an important part of successive approximation register (SAR)-ADC needs to have optimum performance under low power condition. This paper presents the comparison on power consumption together with the output performance flow power SAR-ADC dynamic comparators from three different design proposed by previous researchers. The three circuits is simulated and compared in terms of power consumption, regeneration time, reset time and output transient. The simulation is using Cadence Spectre and setup with 0.18µm CMOS technology, VDD at 0.8V and clock speed 2 at MHz. The analysis results obtained provides the lowest voltage input different (ΔVin) possible for double tail dynamic comparator using 0.18µm CMOS technology while adhering to the 45 corner process requirement. The results can be used as references for further design of ultra-low power dynamic comparator.

Keywords: SAR-ADC; dynamic comparator; double tail dynamic comparator.

1.0 INTRODUCTION

Most of digital circuits are using Analog-to-Digital Converter (ADC) to convert an analogue voltage into digital signal. In recent electronic devices, most of the application such as flash ADC, wireless mobile circuit required low power supply in order to turn ON the device. The fundamental of ADC architecture contain 3 main blocks such as comparator, DAC and Digital Logic. Among these, the comparator block is the major part in conversion process. Thus the needs of ultra-low power comparator circuit are really essential.

The design of ultra-low power comparator with low input supply and high digital output resolution will limit the voltage input different (ΔVin). As an example, for 0.8V input supply, input different of1.6mV is required to generate 10bits digital output resolution. The (ΔVin) load to the comparator is almost equal to the threshold voltage of the transistor which results in poor transistor performance [1]. Thus designing ultra-low power comparator has becomes more challenging with more research done on optimizing the power consumption and at the same time improves the performance of the comparator [1, 2, 3, 4, 5 and 6].

Dynamic comparator is one of the architecture used in ADC due to its ultra-low power features that operates within acceptable accuracy [2].This features only allows current to flow when the clock is triggered, hence it is able to improve the power efficiency compared to conventional comparator [2]. The conventional dynamic comparator as shown in Figure 1, has advantages on high input impedance, rail to rail output swing and no static power [1], [4] and [6]. However it's not suitable for low voltage supply due to

the number of stacking transistor that will limit the current flow.

In this paper, comprehensive study on power consumption and output performance of three double tail dynamic comparator circuits from previous researcher is presented. The circuits have been selected due to its performance in low power consumption with acceptable output performance. All of these three circuit are simulated and compared in term of power consumptions, regeneration time, reset time and circuit stabilities in 45 process corner simulation requirement by using same simulation setup of 0.18µm CMOS technology, VDD 0.8V and clock speed of 2MHz.The simulated circuits are built using input PMOS differential pair, in order to achieve rail-to-rail output swing.

This paper is organized as follow; *Section* 2presents the three different double tail dynamic comparator architecture from previous researcher together with simulation results of power consumption and output transient from 45 process corners. *Section 3* compares the performance of double tail dynamic comparators in term of power consumption, output performance and delay.

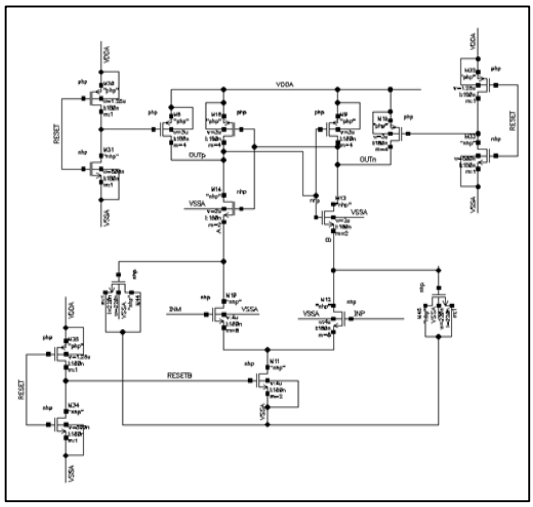

Figure 1 Schematic diagram of the conventional dynamic comparator

2.0 RESULT AND DISCUSSION

2.1 Conventional Dynamic Double Tail Comparator [3]

In 2007 Schinkel proposed new topology on dynamic comparator named as double tail dynamic comparator as shown in Figure 2(a). In double tail dynamic comparator architecture, the circuit is divided into two stages, where stage 1 is the pre-amp and stage2 is the latch part. This comparator circuit used less stacking of transistor compared to conventional dynamic comparator as in Figure 1. By reducing the staking of transistors from 5 to 3 stacks; the current flow through the path can be increased. Furthermore the double tails *M57* and *M71*can enable a large current in the latching stage [3].

Toward analyzing this comparator circuit, test bench as in Figure 2(b) are used as an input voltage to simulate the circuit with clock speed set at *2 MHz* and VDD used *0.8V*. The operation of the circuit is determined by the clock signal (CLK). The latch will start to regenerate when the CLK signal active *low* and differential input voltage from Figure 2(b) load to (*INM;INP*) of preamp at first stage. Then the pre-amp start to generate voltage different at the *fn* and *fp*as an input to the latch. As the latch being triggered by the differential signal in *fn* and *fp,* the *Out1* and *Out2* are generated as shown in Figure 2(c). The voltage at nets *fn* and *fp* are very critical, it has to be perfectly matched in order toreduce the offset voltage and maintain the performance of the output comparator [1]&[3].

For comparator in [3], the two nets are able to generate sufficient voltage different for the latch to operate in Vin=0.8mV and it has passed all 45 process corner required as shown in Figure 2(d). To check the robustness of the circuit, the process corner simulation needs to be executed. For this circuit, the 45 process corner parameter were set with the VDD(0.72V; 0.8V; 0.88V), temperature (-25; 27; 125) and fabrication process corner with(FS; SS; SF; TT; FF).

To analyze the energy efficiency for this circuit, the simulation has been done as shown in Figure 2(c). The total current measured in this circuit is around *77nA* and the power consume is around *61nW* which is the lowest power consumption among the analyzed comparator circuits in this paper.

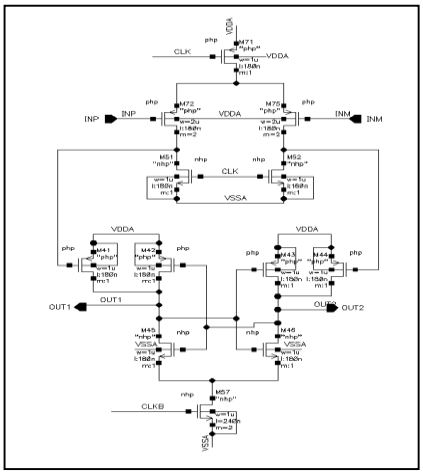

Figure 2(a) Schematic diagram of Comparator [3]

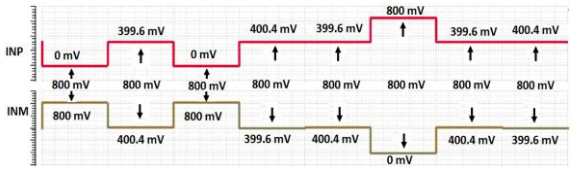

Figure 2(b) Input test bench for transient analysis simulation

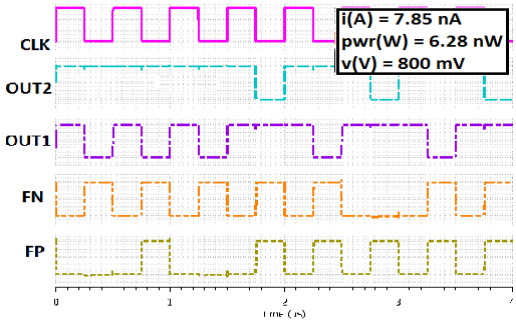

Figure 2(c) Simulated average power consumption from Comparator [3]

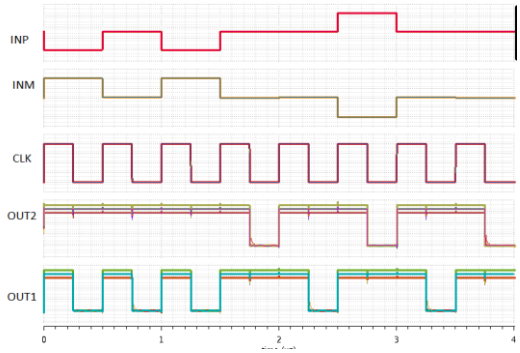

Figure 2(d) Corner simulation result (temp. = -25 to 125 degree) from Comparator [3]

2.2 Pseudo Different Dynamic Double Tail Comparator [2]

Pseudo differential dynamic comparator was proposed by *Paik, eta al.* in 2008 [2] as shown in Figure 3. This circuit is a modification from of the conventional double tail dynamic comparator proposed by *D.Schinkel,eta al*. in 2007[3]. In the design, the author proposed to reduce the latching clock from 2 phases to 1 phase. This is done by removing the tail current in the second stage *M57* as in [3], which was triggered by inverse phase of a latching clock (*CLKB*) and replace it with signal from output of a pre-amp *fn* and *fp* nets. As a result, the skew between two phases of latching clock can be improved. However, this also increased the number of transistor which will affect the output performance and increase the power consumption as summarized in Table1.

For this circuit the total power consumption is 252nW with the clock speed of 2 MHz and VDD 0.8V. The simulated output *Out1* and *Out2* are generated from nominal simulation shown in Figure 4. For condition of ΔVin = 0.8mV, the corner parameter of VDD 0.72V, temperature at -25°C and process corner FS and SS, the comparator will take longer time regenerate, as shown in Figure 5(a).However as the temperature range is reduced in the corner parameter from minimum -25 to 0 degree and maximum from 125 to 100 degree, the failed corner was improved as shown in Figure 5(b).

At lower temperature, this circuit is unstable due to less current flow through the device and also at FS and SS process corner, the transistor threshold voltage are varied almost equal to the small input voltage*INP* = 0.4mV.

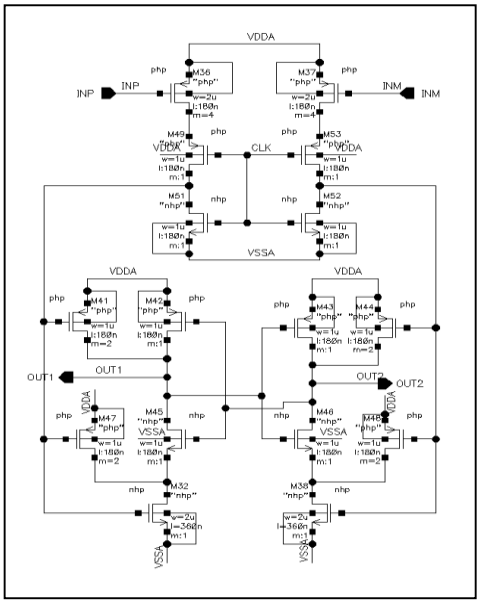

Figure 3 Schematic diagram of Comparator [2]

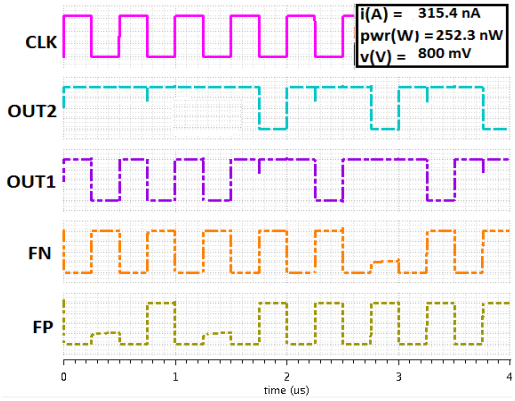

Figure 4 Simulated average power consumption from Comparator [2]

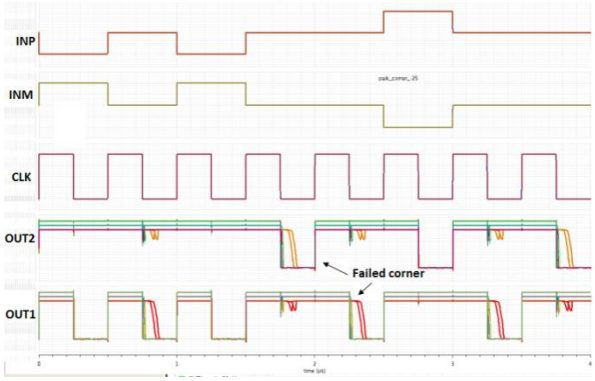

Figure 5(a) Corner simulation result (temp. = -25 to 125 degree) fromComparator [2]

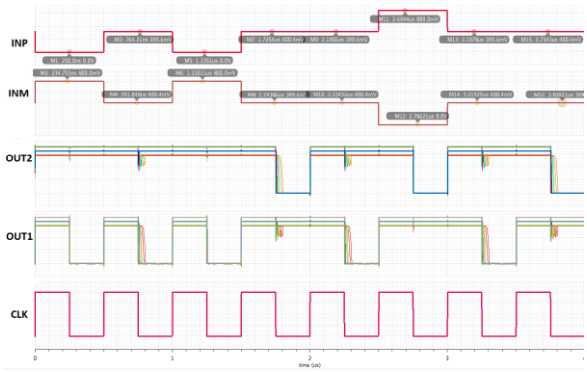

Figure 5(b) Corner simulation result (temp. = 0 to 100 degree) from Comparator [2]

2.3 Double Tail Dynamic Comparator by [1]

Babayan 2014 has proposed modification of conventional double tail comparator by *D.Schinkel, eta al*. in 2007[1]. In the design, the author focuses on improving the latch regeneration and reset time in order to improve the speed of the comparator. The proposed comparator still based on double tails dynamic comparator design due to its performance in low voltage architecture [1]. The author has added an additional control transistor *M51* and *M52* in order to increase the ΔV*fp/fn*at node *fp* and *fn*. By increasing the ΔV*fp/fn*, the latch regeneration and reset time can be reduced as shown in Figure 9.

However, the current drawn from the control transistor *M51* and *M52* has caused static power consumption to the circuit. Therefore the author proposed additional *M75* and *M74* to overcome the static power issues but the power consumption for this circuit is still higher compared to [2] and [3] circuit. By using 0.18µm CMOS technology, and VDD 0.8V, the power consumption for this design is around 25.44µW and current around 31.804µA as shown in Figure 7.

Throughout the corner test simulation with the test parameter VDD (*0.72V; 0.8V; 0.88V*) Temperature (*0; 27;100*) with Silltera process corner as shown in Figure 8(b), it has fail almost 50% of the process corner simulation which is mostly at VDD 0.72V. This circuit is not very stable when operate with ΔVin = 0.8mVtogether with 0.18 µm CMOS technology.

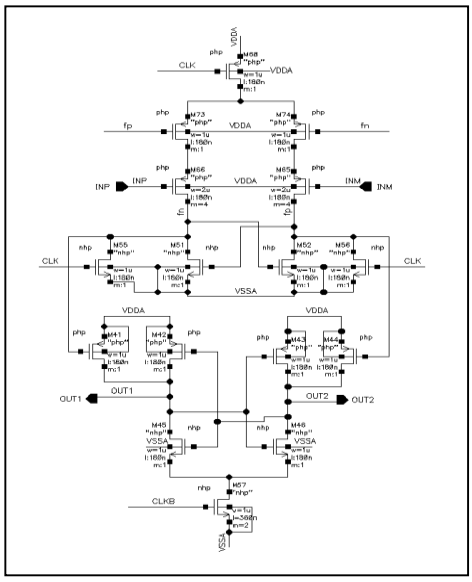

Figure 6 Schematic diagram of Comparator [1]

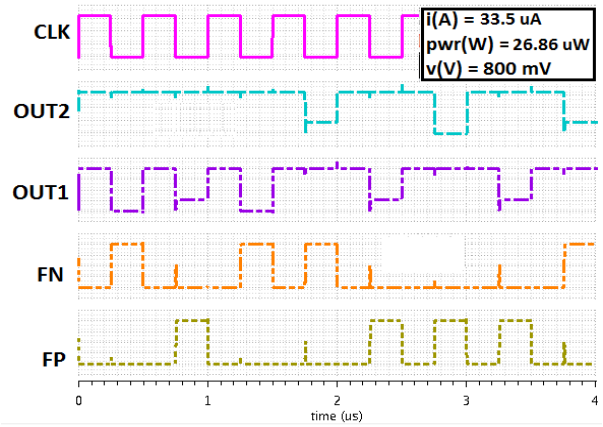

Figure 7 Simulated average power consumption from Comparator [1]

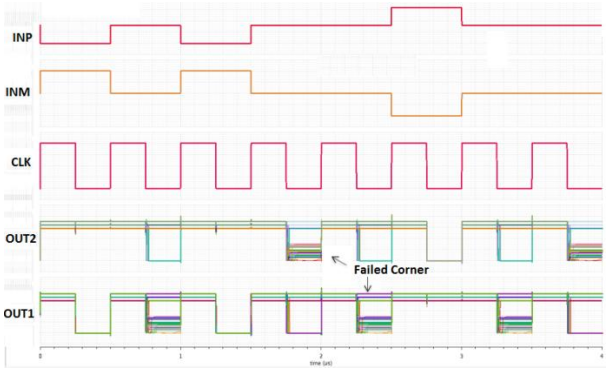

Figure 8(a) Corner simulation result (temp. = -25 to 125 degree) from Comparator [1]

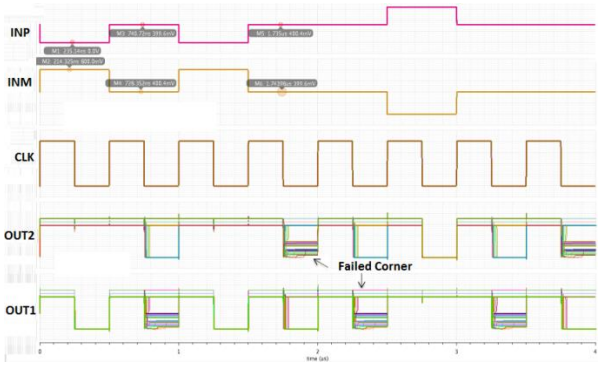

Figure 8(b) Corner simulation result (temp. = 0 to 100degree) from Comparator [1]

3.0 SUMMARY

In order to analyze the performance of all the three double tail dynamiccomparators, the circuits have been simulatedusing 0.18µm CMOS technology with VDD = 0.8V and clock speed 2 MHz. The transistor size for all three circuits is scale at the same size and PMOS are used as input differential to the circuit. The test-bench in Figure 2(b) is used as an input setup during the circuit simulation. The details of the performance comparison are shown in Table1.

Table 1 Summary of performance comparison

Double Tail Dynamic Comparator	Power Consumption	Regeneration time	Reset time	45 Process Corner Result
Comparator[1]	25.44µW	2.11ns	396ps	Passed 50%
Comparator[2]	252.32nW	2.13ns	552ps	Passed 98%
Comparator[3]	61.38nW	1.52ns	727ps	Passed 100%

3.1 Power Consumption Analysis

The analysis on power consumption for each comparator circuit has shown in Table1. The Comparator [3] proposed by [3] have less number of transistors 12 and less stacking 3 which only consumes 61nW. ForComparator [2] the total number of transistors is16 and stacking into 3, consume power 252.321nW. Finally Comparator [1] consumes power 25.44µW from total 16 numbers of transistors with stack of 4. From the comparison, Comparator [3] is the most suitable circuit for ultra-low power ADC due to the lower power consumption compared to Comparator [2] and [1]. However this circuit is not suitable for high speed ADC since it required longer time to reset.

3.2 Delay Analysis

From the simulation comparison as in Fig.8, it is found that Comparator [3] has less regeneration time 1.520ns compared to other two comparator but longer reset time 727ps as shown in Fig.9. From the comparison, Comparator [1] is more suitable for high speed ADC since it has average regeneration time 2.11ns and reset time 396ps compared to Comparator[2] and [3].

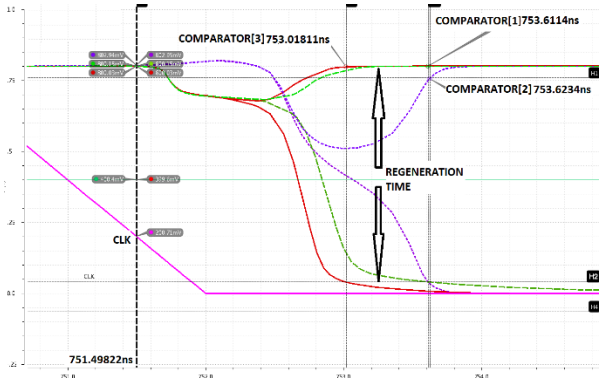

Figure 9(a) Regeneration time performance

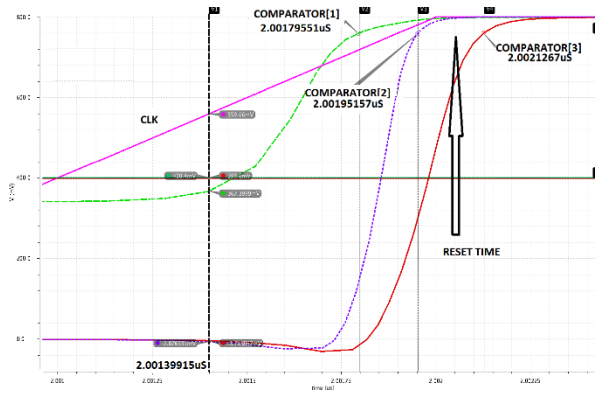

Figure 9(b) Reset time performance

4.0 CONCLUSIONS

In this paper, the analysis on power consumption and output performance from three different designs of double tails dynamic comparator has been compared. The analysis is based on circuit simulation using 0.18µm CMOS process with VDD 0.8V and small ΔVin up to 0.8 mV. We can conclude that, the performance of the comparators become more unstable when operate at ΔVin 0.8mV in 0.18µm CMOS process technology. This is due to the limited of common-mode input range.Therefore the comparator circuit with higher number of transistors facing more stability issues when operate with low supply voltage andthe small ΔVin since it limits the current flow in the circuit.

From the finding, Comparator [3] is the most suitable circuit for ultra-low power SAR-ADC however not for high speed application. Besides Comparator [1] is designed for high speed application but less efficient when operate at VDD lower than 0.8mV. Comparator [1] also not suitable for ultra-low power SAR-ADC due additional

transistor added in the circuit. Comparator [2] as in analysis, show batter performance in power consumption compared to Comparator [1] and average performance in term of delay and output stability.

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References

[1] Babayan S. and LotfiR. 2014. *Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator. IEEE Trans. On VLSI System.* 22(2): 343-352

[2] PaikD.,Miyahara M. and Matsuzawa A. 2011. An Analysis on a Pseudo-Diffrential Dynamic Comparator with Load Capacitance Calibration*inASIC (ASICON), IEEE 9th International Conference.* 461 - 464.

[3] Shinkel D.,KensinkE.,KlumperinkE., Van Tuijl E., and NautB.2007. A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time, *in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*. 314-415.

[4] Goll B. and ZimmermannH.2009. A comparator with reduced delay time in 65-nm CMOS for supply voltage down to 0.65.IEEE Trans. *Circuits Sys. II, Exp. Brief*. 56(11): 810-814.

[5] Elzakker M., Tuijil E., Geraedts P., SchinkelD., Klumperink E.A.M. and NautaB., 2010. *A 10-bit Charge-Redistribution ADC Consuming 1.9uW at 1 MS/s. IEEE Jounal of Solid-State Circuits.* 45: 1007-1015.

[6] Brenna S., and Bonfanti A.2014. *A 6-fJ/conversion-step 200-kSps asynchronous SAR ADC with attenuation capacitor in 130nm CMOS. i Analog Integr Circ Sig. Process.* 81: 181-194.