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PERFORMANCE ANALYSIS OF INDUCTIVELY DEGENERATED CMOS LNA

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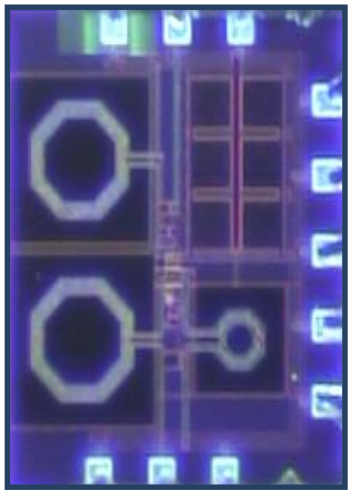
Graphical abstract



Abstract

This paper features the design approach of a low noise amplifier (LNA) which dissipates 19.89 mW from a 1.2 V power supply that was designed based on a 0.13 µm RFCMOS process. A detailed methodology that leads to a power-efficient design of the LNA is presented. A theoretical noise figure optimization using fixed power and physics-based gm/ID characteristics were used as a design optimization guide. Simultaneous noise and input matching under constrained power (PCSNIM) was achieved with an extra gate-source capacitor while gain enhancement was obtained by employing a capacitive feedback at the cascode transistor. The LNA is further optimized by implementing the forward biasing scheme to attain good LNA performance at low power. The end-design of the optimized LNA produces a noise figure of 3.55 dB, a power gain of 17.12 dB, a Third Order Input Intercept Point (IIP3) of -19.70 dBm, an input reflection coefficient of -14.15 dB and an output reflection coefficient of -18.37 dB. Simulated results validate peak performance at 2.45GHz, which makes the LNA suitable for Bluetooth and the industrial, scientific and medical (ISM) applications.

Keywords: LNA; CMOS; inductive source degenerated

1.0 INTRODUCTION

The wireless communication industry is currently undergoing incredible evolution. There is huge demand for low power, portable, battery-operated electronic devices. This introduces new design issues and challenges such a low power and good noise performance. These growing demands provide the motivation for further research and analysis toward achieving good LNA architecture for the wireless application. There are many problems in designing LNA because there are many requirements need to be satisfied in order to achieve high performance LNA. The parameters of interest are minimum noise contribution, maximum gain, low power consumption, source impedance matching, circuit stability and linearity.

In responding to the demand for a low-cost but high performance wireless front-end circuitry, many intensive studies on radio-frequency CMOS circuits have been conducted. Noise performance is a critical factor for the LNA. Most of the function of LNA are dependent on each other. Hence, to improve one function so the other function will be degraded. The goal is to reduce the trade-off between high performance and low-cost, low power consumption design. The objective of this project is to analyze the performance of the noise figure, gain, reverse isolation, impedance matching, linearity, power consumption and stability. Besides, this project is implemented by using the EDA and electromagnetic tool to simulate and analyzed the circuits design. The other objective is to use the inductive source degeneration topology as a basic circuit topology in order to obtain the impedance matching with the optimize gain and noise figure.

Low noise amplifier (LNA) is built on the RF receiver. In the RF receiver there were come out with the other component such band pass filter, mixer and the demodulator. The main function of LNA is it can amplify

weak signal that was received by the receiver. Obviously, the signal that was transmitted is in low signal and this LNA will amplify that signal to become it in high signal. LNA is the first active block in a receiver chain. It follows the antenna and its output drive a mixer. In many common cases, LNA always inserted between the filter and antenna. LNA is a circuit used to provide gain while maintaining noise as low as possible. LNA widely used in wireless receiver and sensor interfaces.

This paper is organized into four sections. The first part provides an introduction and background of the research topic, motivation of the research and outline of the paper. The second part is the theoretical design parameters, circuit architectures, design trade-offs and conventional LNA topologies are described. The current low power LNA designs and the important requirements in the IEEE.802.11 standard are also discussed. Results of the simulated design will be discussed in the third section. Performance comparison with other published works also discussed in this section. Lastly, the findings in this paper will be summarize in the conclusion part.

2.0 INDUCTIVE DEGENERATION TOPOLOGY

In LNA, there are many topologies which is resistive termination, series shunt feedback, common gate connection and inductive degeneration. Based on the literature, inductively degenerated common source is the most widely use topology in LNA circuit architecture due to its ability in good input impedance matching. Inductively degenerated cascode LNA is chosen to be implemented because it is the basic topology to most of varsities LNA presently available. It allow maximum gain under low power constraint [3]. Among the four topologies, the inductive degeneration is the best for the noise figure and gain specification. CMOS technology allow integration of both digital and analog circuits on the same chip in order to reduce cost, improve performance, increase manufacturability by reducing the number of chips and bond wires.

2.1 Circuit Diagram

The proposed structure of the LNA is a single-stage cascode LNA with inductive degeneration at the source. The cascode topology is embraced as it offers high gain and worthy input-output isolation, which increase stability and simplify input port matching [3]. The inductively common-source structure on the other hand allows for maximizing gain under a reasonably low power.

The simplified schematic of the proposed CMOS LNA for simultaneous noise and input matching is illustrated in Figure 1 and the simplified small-signal equivalent circuit is shown in Fig 2 where vRF and RS model the antenna.

The effects of the common-gate cascode transistor M2 on the noise and frequency response are neglected. Generally, the 0.13 µm LNA is to be designed such as to comply with the specifications whereby the LNA needs to provide a high gain of greater than 15 dB with a noise figure of lower than 4 dB operating at low power.

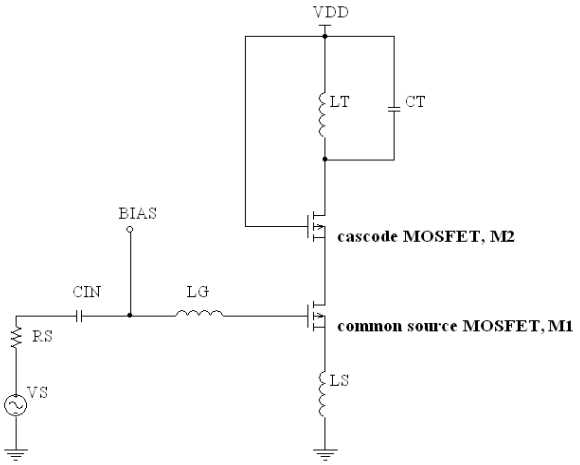


Figure 1 Proposed CMOS LNA for simultaneous noise and input matching

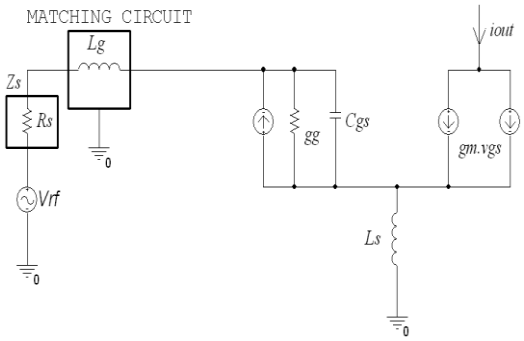


Figure 2 Simplified small-signal equivalent circuit

2.2 Theoretical Design

For the topology, the basic LNA has been used in this analysis. This basic LNA used the inductive degeneration as the impedance matching. Then the cascode LNA also used in this design. The calculation for this analysis is first starting with defining the value of the inductor. Basically the inductor that used is 1 nH. The cut-off frequency which used the below equation:

$$\omega_t = \frac{gm}{Cgs} = \frac{Rs}{Ls}$$

For the next, find the optimal Q for the inductor

$$QL = \sqrt{1 + \frac{1}{P}}$$

Where $P = \frac{\delta.\alpha^2}{5.\Upsilon}$

Parameter basically is dependent on the technology that is used but typically the value of is set between 2-4 (normally take value 4). δ is set 2-3 times of the value of (normally take 4). α is assumed 0.8-1 (normally take 0.9). Then find the value of Lg:

$$Lg = \frac{Q_L R_S}{\omega_0} - Ls$$

After that, find the gate source capacitance which is:

$$Cgs = \frac{1}{\omega_0^2 (Lg+Ls)}$$

Then find the width which is

$$W = \frac{3}{2} \frac{Cgs}{C_{ox} L_{min}}$$

Where,
εs = dielectric constant for silicon 3.9
εo = dielectric constant for free space 9.854E^{-14} F/cm
After the value of width have been found then next stages are to find the value of gm.

$$gm = \omega_t . Cgs$$

Now the value of $E_{ffective}$ can be found by using the equation

$$V_{eff} = (V_{gs} - V_T) = \frac{gm.L_{min}}{U_n.Cox.W}$$

Last the value of bias current can be calculated by using formula

$$Id = \frac{1}{2} gm.Veff$$

3.0 RESULTS AND DISCUSSION

3.1 Pre and Post Layout Simulation

Figure 3 below shows the pre and post layout simulation performance of single ended inductively degenerated cascode PCSNIM. It is designed for operating frequency at 2.45GHz. It can be seen that the S parameter curve for post layout simulation is shifted to lower frequency. This is due to the parasitic of the component lower down the frequency response of the LNA.

Comparing the pre- and post-layout simulation results, the post-layout simulation will normally produce results that are worse than the results generated by the pre-layout simulations. This is due to the parasitics that were included in the post-layout simulations. The results from the post-layout simulation are normally closer to the measured results as this type of simulation includes the parasitic effects of the substrate. However, the post-layout simulation, does at times over-estimates the design with parasitics and resulted in the measurement being better reflected by the pre-layout simulations. The problem with over-estimating the parasitics is that the design layout size and power consumption tend to be larger due to the designer's eagerness to overcome these parasitics. This is because special layout techniques were employed and higher current were set to achieve higher gain. On the other hand, if the parasitics were under-estimated, the circuit's performance may not be optimized or even functioning at all.

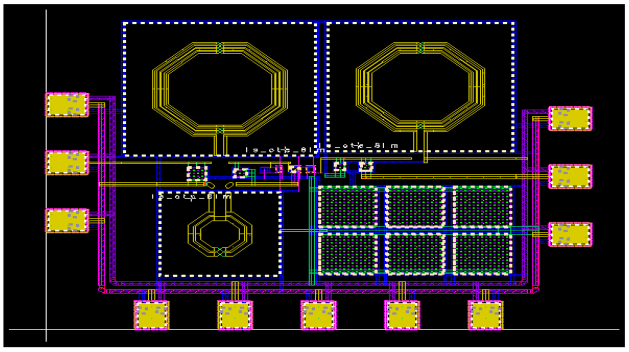


Figure 3 Layout

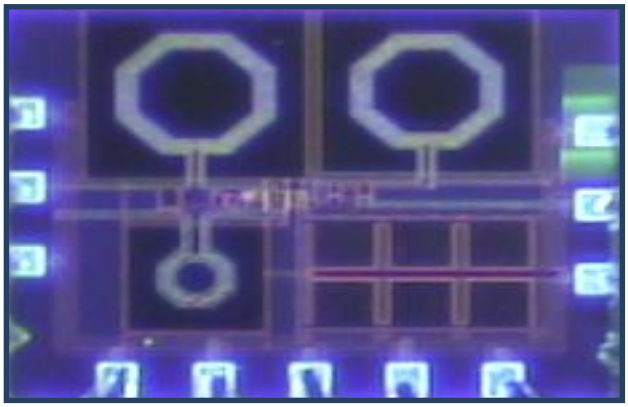


Figure 4 Fabricated chip micrograph

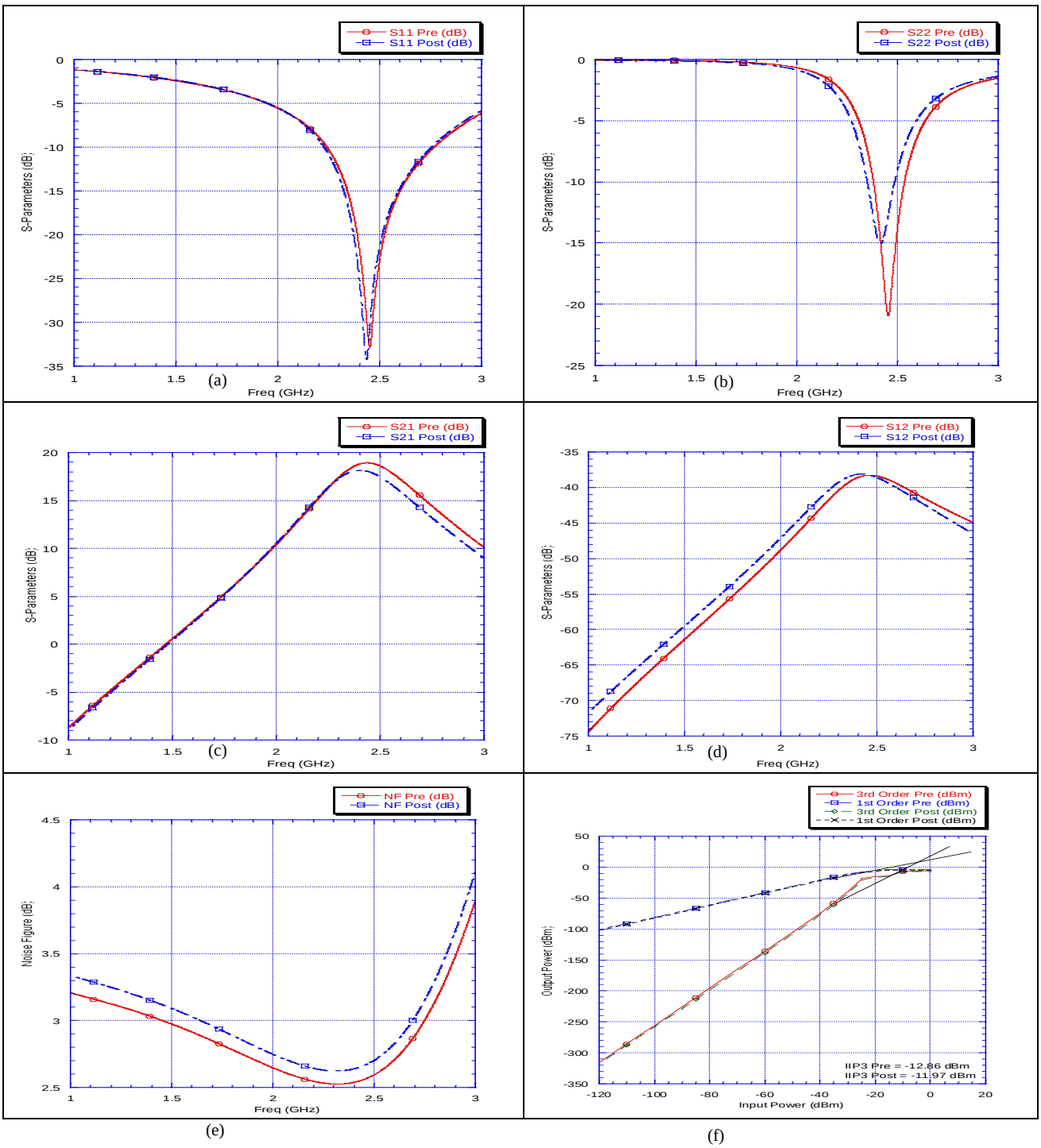


Figure 5 Pre and post layout simulation (a) S11 (b) S22 (c) S21 (d) S12 (e) NF (f) IIP3

4.0 CONCLUSION

In order to achieve the many design goals target for the LNA, the correct choice of LNA topology becomes very important. Many topologies were invented to optimize the performance of the LNA. SNIM offers simultaneous noise and input matching as oppose to the classical method of input matching. The constraint with this LNA is the minimum noise figure may become worse if smaller devices are used. Under this condition, a higher degeneration inductor is required which will move the noise figure away from the minimum noise figure of the classical input matching LNAs.

In the PCSNIM LNA, a capacitor is connected between the G-S of the device to relax the

requirement for large gate inductance if the device is small.

It is shown in this report that the performance of the LNAs will improve if the input and output stages of the LNA were properly matched. As for the cascode in PCSNIM, the LNA need to be matched to a 50Ω load. As for LNA for wireless LAN application, power consumption of the LNA is best kept to its minimum possible for implementations in mobile systems. For the IEEE802.11b/g standard, a typical current consumption for single ended input LNA is less than 4 mA and this result in power consumption of approximately 4 mW at a supply voltage of 1.2V for a design implemented on a 0.13 µm process.

Finally, gain and matching of the inductively-degenerated cascode LNAs are very dependent on their inductors. Therefore, good inductor models are very important in achieving good performances.

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