SOC-BASED BIOMEDICAL EMBEDDED SYSTEM DESIGN OF ARRHYTHMIA DETECTOR

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Graphical abstract
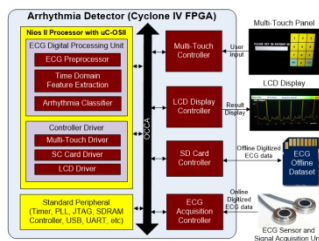
Abstract

Arrhythmia is an irregular heartbeat where the blood may not be delivered effectively throughout the body and cause sudden cardiac arrest (SCA). Immediate treatment is required to prevent SCA. However, most of the existing electrocardiogram (ECG) monitoring devices are bulky, cost expensive and lack arrhythmia detection and classification system. This paper proposes a front-end on-board graphical interface design of System-on-Chip (SoC) based arrhythmia detector which can be used as a first screening device for cardiac disease patient. The system consists of a knowledge-based arrhythmia classifier which is able to identify three types of arrhythmias which are ventricular fibrillation (VF), premature ventricular contractions (PVCs) and second-degree atrioventricular (AV) block. The system has been evaluated and benchmarked with ECG data from MIT-BIH arrhythmia database. The results show that its accuracy is up to 99.25% with a computation time of 6.385 seconds. It is highly portable and relatively inexpensive for installation in small clinics and home monitoring.

Keywords: Arrhythmia, electrocardiogram (ECG), Graphical User Interface (GUI), knowledge-based classifier, System-on-Chip (SoC)

Abstrak

Aritmia adalah gangguan irama jantung di mana darah tidak boleh disalurkan ke seluruh badan secara berkesan dan menyebabkan jantung berhenti berdetak secara tiba-tiba atau yang disebut Sudden Cardiac Arrest (SCA). Rawatan segera diperlukan bagi sesetengah jenis aritmia. Namun, kebanyakan peranti yang sedia ada untuk pemeriksaan elektrokardiogram (ECG) adalah bersaiz besar, mahal serta kekurangan sistem pengesanan dan klasifikasi aritmia. Dalam kertas kerja ini, pengesan aritmia berdasarkan Sistem-atas-Cip dengan *front-end on-board* antaramuka pengguna bergrafik(GUI) telah dicadangkan untuk digunakan sebagai peranti pemeriksaan bagi pesakit jantung. Sistem ini dapat mengelaskan tiga jenis aritmia iaitu fibrilasi ventrikel (VF), kontraksi ventrikel pramatang (PVCs) dan blok atrioventrikular (AV) tahap kedua dengan menggunakan algoritma klasifikasi aritmia berasaskan pengetahuan. Sistem ini telah dinilai dan ditanda aras dengan data ECG daripada pangkalan data aritmia MIT-BIH. Hasil keputusan menunjukkan bahawa ketepatan sistem ini mencapai 99.25% dengan masa pengiraan selama 6.385 saat.

Kata kunci: Aritmia, elektrokardiogram (ECG), Antaramuka Pengguna Bergrafik (GUI), pengelas berasaskan pengetahuan, Sistem-atas-Cip (SoC)

1.0 INTRODUCTION

Arrhythmia is a condition in which the electrical conduction system of heart is abnormal that causes irregular heartbeats, where the heart rate can be faster (tachycardia) or slower (bradycardia) [1]. Although most arrhythmias cause no prominent symptoms in the patient, there are some arrhythmias that can cause SCA such as VF where the blood is not delivered to the body. There are more than 4 million arrhythmia patients in the world and more than 400 thousand people died from this disease each year [2].

Electrocardiography (ECG) is the standard method used to diagnose arrhythmias. However, most of the ECG monitoring devices are cost expensive [3], bulky [4] and lack self-classification and interpretation abilities. Hence, it is not suitable to be used as home monitoring device or first screening device for small clinics. In addition, the ECG test is only available in specialist hospitals in the urban city. For patients who are suspected to have cardiac disease, they may need to travel for medical, especially in rural area [3, 4, 5]. Besides, most of the ECG monitoring devices lack a user-friendly Graphical User Interface (GUI). They are not fully standalone system as they still need to depend on a host personal computer (PC) for data analysis and ECG signal display.

In order to reduce the mortality rate, people are encouraged to check their heart condition frequently and a reliable combination of cost-effective ECG monitoring and accurate analysis is very important. This paper proposes a portable SoC-based arrhythmia detector with interactive touch screen GUI. The user-friendly GUI enables a non-expert user like a medical officer in general hospital to make good use of it as a cardiac disease screening device. If the patient is suspected to have arrhythmia, the medical officer can refer the patient directly to specialist hospital. This in turn reduces workload of nurse and medical staff in the urban city and improves the health care service in rural area. Furthermore, this portable standalone ECG monitoring device can also be used for home monitoring. If there is any arrhythmia detected, patient would be alerted to seek emergency medical attention.

2.0 ARRHYTHMIA

Arrhythmias are classified by where they originate: the atria (supraventricular arrhythmias), the ventricles (ventricular arrhythmias), or the heart's electrical system (other arrhythmias) [6]. Examples of supraventricular arrhythmias are atrial fibrillation, atrial flutter and premature atrial contractions (PACs) while premature ventricular contractions (PVCs), ventricular fibrillation (VF) and ventricular tachycardia are examples of ventricular arrhythmias. Other arrhythmias include sinus node dysfunction, bundle branch block and atrioventricular (AV) block.

The proposed system is able to identify three types of arrhythmias which are PVCs, VF and second-degree AV block where each of them will be further explained in the following subsections.

2.1 Premature Ventricular Contractions (PVCs)

PVCs are early depolarization of the myocardium originating in the ventricle in which there are extra beats that disrupt the regular heart rhythm as shown in Figure 1 [6]. The heartbeat is initiated by the Purkinje fibers in the ventricles rather than by the sinoatrial node, the initiator of normal heartbeat. Normally, PVCs are benign in the absence of structural heart disease. There are many causes of PVCs, typically caused by suffering a heart attack or excessive consumption of alcohol, cocaine, and caffeine [7].

Figure 1 ECG of bigeminy PVCs [8]

2.2 Ventricular Fibrillation (VF)

VF is the condition where the contraction of the ventricle chamber of the heart is uncoordinated and electrical impulses are disorganized as shown in Figure 2 [9]. The ventricles quiver and are unable to contract or pump blood throughout the body which will then cause SCA. VF is a medical emergency and the patient must be treated with cardiopulmonary resuscitation (CPR) or defibrillation as soon as possible in order to restore the normal rhythm.

Figure 2 ECG of VF [10]

2.3 Second-Degree Atrioventricular (AV) Block

AV block, or heart block, is a delay or complete block in the conduction of electrical impulses from the sinoatrial (SA) node, through the AV node, to the ventricles [11]. There are three degrees of AV block. In second-degree AV block, some of the electrical impulses do not reach the ventricles. Consequently, the heart beats are slow, irregular, or both as shown in Figure 3 The conduction failure of electrical impulses causes the ventricle chambers fail to

contract and hence fail to deliver the blood to the body. The symptoms of this type of arrhythmia include lightheadedness, dizziness, or blackout.

Figure 3 ECG of second-degree AV block - Mobitz Type II [12]

3.0 RELATED WORKS

Heart Rate Variability (HRV) is the variation of time interval between heartbeats. Analysis of HRV, or fluctuation of R-R intervals, reflects many physiological factors related to cardiac health such as arrhythmia [13, 14]. According to Tsipouras *et al*. [15], arrhythmias can be classified by analysing the R-R intervals (as indicated in Figure 4) extracted using the Pan and Tompkins algorithm [16]. The proposed method is a knowledge-based method which is able to classify four categories of beats which are normal beat, VF, PVCs and second-degree AV block. The classification algorithm can further classify six rhythm types of arrhythmias based on the beat classification. The six rhythm types of arrhythmias include the ventricular bigeminy, ventricular trigeminy, ventricular couplet, ventricular tachycardia, ventricular fibrillation, and second-degree AV block. This algorithm achieves high accuracy of detection that is 98% for beat classification and 94% for arrhythmic episode detection and classification. The disadvantage of this method is that it can only detect arrhythmias which can be determined by analysing the HRV. Besides, the significant noise in the signal could be misrecognised as R peak and cause the false positive result of arrhythmia detection.
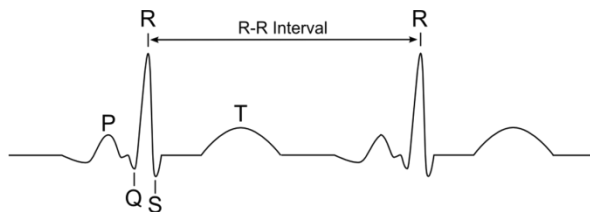

Figure 4 Indication of R-R interval

Another arrhythmia classification was proposed by Wang *et al*. [13] which was based on the feature reduction method and probabilistic neural network (PNN) classifier to classify eight types of arrhythmias. The eight types of arrhythmias include normal beat, PVCs, paced beat, right bundle branch block beat, left bundle branch block beat, PACs, ventricular flutter wave, and ventricular escape beat. There are

four steps for this method which are data acquisition, feature extraction and normalization, feature reduction, and classification. The classification accuracy of this method is up to 99.71% [13].

Apart from the software implementation (SW) as the works discussed above, an ECG pre-processing algorithm such as QRS detection can also be hardware (HW) implemented into a Field-programmable Gate Array (FPGA). For instance, the work from Knezevic *et al*. [17] which implement the Haar transform into Altera Cyclone II FPGA platform to extract the QRS complexes and detect the R peak of the ECG signal. Haar transform has a number of advantages, which include being fast, conceptually simple, memory efficient as it can be calculated without temporary array, and reversible without the edge effect. However, this implementation has several limitations, such as noise removal from faster signals and signal compression, which is not an issue in the case of processing the ECG signal.

There are also some examples of FPGA based arrhythmia classifier proposed by other researchers either using Xilinx [18, 19] or Altera [20] technologies. According to [18], the data processing speed for the HW/SW implementation of the proposed algorithm is up to 17 times faster than the SW implementation.

According to the previous research done by Norhayati *et al*. [21], the proposed system could only read offline ECG data. The dataset is executed by computing the ECG pre-processing and HRV feature extraction in the frequency domain. At each execution stage, an output file is generated and a graph is plotted on a host PC using MATLAB. The advantages of this system are that it is cost-effective and can be implemented into a portable device. However, the design does not include the classification algorithm and suffers from several design problems such as speed, noise and feature extraction accuracy. Besides, it lacks of a user-friendly GUI to retrieve the user input and display the processing and analysis result. In addition, it is not fully standalone system because it depends on the host PC. The proposed arrhythmia detector that is presented in the next section is the improvement of this in-house design of ECG biomedical embedded system.

4.0 PROPOSED ARRHYTHMIA DETECTOR

There are three main types of Altera Field-programmable Gate Array (FPGA) technology which consist of Stratix, Arria and Cyclone FPGAs. After comparing the Altera FPGA technology, Cyclone IV was chosen for this study because it has acceptable performance, low cost and suitable for a cost-effective solution of portable standalone arrhythmia detector.

Figure 5 shows the top-level system architecture of the proposed SoC-based arrhythmia detector, which uses the Altera Video and Embedded Evaluation Kit - Multi-touch (VEEK-MT) board for display purposes. The

system architecture consists of four main subsystems called ECG sensor and signal acquisition unit, ECG preprocessor and feature extraction, arrhythmia classifier and on-board touch-screen menu to provide user friendly interaction.

This system is able to process both offline ECG dataset which is stored on the SD card and also online ECG signal which is obtained from ECG sensor and signal acquisition unit. Both the pre-processing, feature extraction and arrhythmia classification are implemented as embedded software executed by the Nios II processor which also acts as the system's top level controller. It also executes embedded operating system (µC-OS II) to provide file management. The on-board touch-screen menu is meant to capture user input and display the classification result using the graphical user interface which is developed based on underlying peripheral controllers and associated device drivers. Each of the peripheral devices communicates to each other using the Avalon System Interconnect Fabric. The details of each part are described in subsections below.
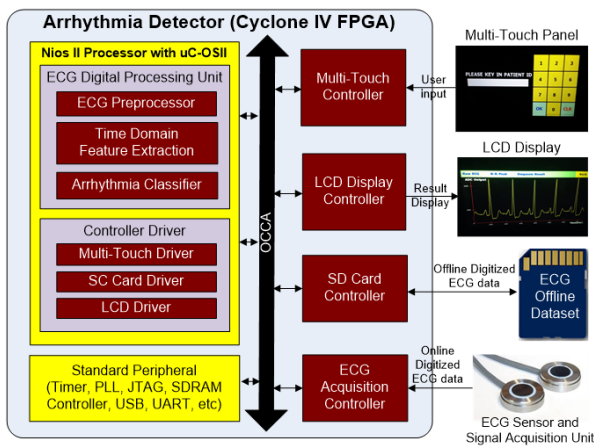
Figure 5 Top-level system architecture

4.1 ECG Signal Acquisition

The circuit design layout of ECG signal acquisition is as shown in Figure 6. The circuit is a 3-lead ECG system circuit [22]. The design is based on the Einthoven's Triangle [23]. The main component in the design is the AD624AD amplifier from Analog Devices. The band pass filter which consists of a 0.1 pF capacitor and 470 kΩ resistor is located at the output of the amplifier to band pass 0.5 Hz to 150 Hz signal frequency. The output of the band pass filter is then fed to an ADC circuit. The ADC circuit design is shown in Figure 7. It is based on the work in [24]. The ADC chip used is the ADC0804 from Texas Instruments. The output of the ADC is connected to the GPIO pin of the Altera VEEK-MT board. A General-purpose input/output (GPIO) controller is

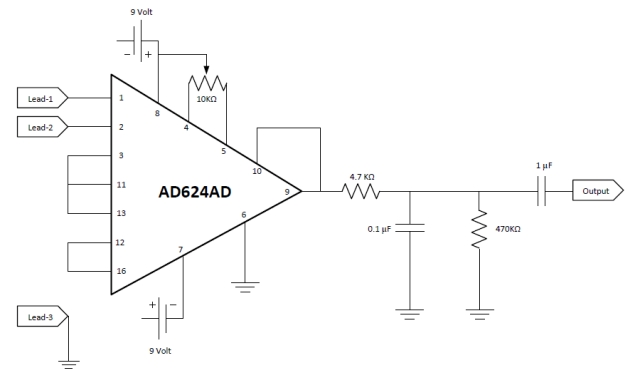added into the QSYS and the IOWR function is added into the program for reading the input value.
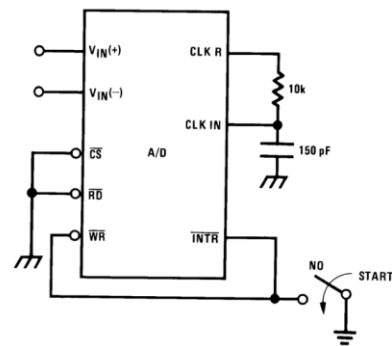

Figure 6 ECG circuit design [22]

Figure 7 ADC circuit design [24]

4.2 ECG Pre-processing and Feature Extraction

As shown in Figure 8, the ECG pre-processing unit consists of band pass filter, differentiator, squaring, and moving window integrator while the feature extractor unit consists of R peak detector before sending to the arrhythmia classifier. During ECG pre-processing, the QRS complexes are detected using Pan and Tomkins algorithm [16, 25] and the R peaks are then detected through feature extraction. Each of the processes in both units is discussed in detail in the following sub subsections.
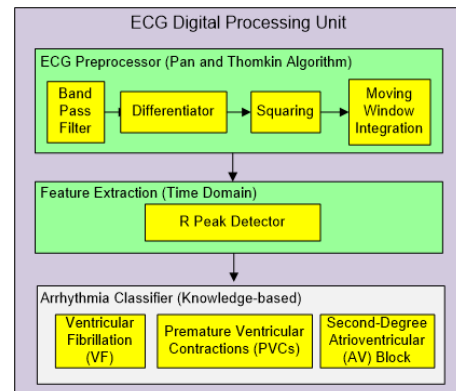

Figure 8 ECG pre-processing and feature extraction units

4.2.1 Band pass filter

The band pass filter, cascaded low pass and high pass filters, with a pass band of 5 Hz to 15 Hz is used to isolate the predominant QRS energy centered at 10 Hz. The low pass filter eliminates noise such as the electromyogram (EMG) and 50 Hz power line whereas the high pass filter eliminates motion artifacts, P and T waves. The difference equations of the high pass and low pass filters are shown in (1) and (2), respectively.

$$p(n) = x(n-16) - \frac{1}{32}[y(n-1)+x(n) - x(n-32)] \qquad (1)$$

$$y(n) = 2y(n-1) - y(n-2)+x(n) - 2x(n-6)+x(n-12) \qquad (2)$$

where $x(n)$ is the input ECG signal, $p(n)$ is the output of the high pass filter and $y(n)$ is the output of the low pass filter.

4.2.2 Differentiator

The differentiator is used to obtain information on the slope of the QRS complex, overcome the baseline drift problem and accentuate the QRS complexes relative to the P and T waves. The difference equation of the derivative filter is shown in (3).

$$y(n) = \frac{1}{8}[2x(n)+x(n-1) - x(n-3) - 2x(n-4)] \qquad (3)$$

where $x(n)$ is the input of the differentiator from band pass filter output and $y(n)$ is the output of the differentiator.

4.2.3 Squaring

The squaring operation emphasizes the higher frequency component and attenuates the lower frequency component. It makes the processed signal become positive values and amplifies the signal nonlinearly. The difference equation of the squaring function is shown in (4).

$$y(n) = [x(n)]^2 \qquad (4)$$

where $x(n)$ is the input from differentiator output and $y(n)$ is the squaring function output.

Figure 9 shows the flowchart of implemented squaring function which also aims to reduce the noise introduced to the moving window integrator.

4.2.4 Moving window integrator

The moving window integrator is used to smooth the processed signal from squaring function. As the sampling frequency of this work is 200 Hz, the window width is set to 32. The difference equation of the moving window integrator is shown in (5).

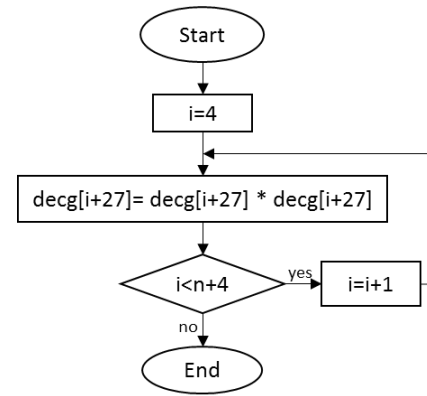$$y(n) = \frac{1}{32}\sum_{k=1}^{32} x(n-k) \qquad (5)$$

Figure 9 Process flow chart of squaring function with noise reduction

where $x(n)$ is the input of the moving window integrator from squaring function output, k is width of the window and $y(n)$ is the output of the moving window integrator.

Figure 10 shows the flow chart of implemented moving window integrator which aims to improve computation timing performance by skipping the repetition of the addition of 32 arrays for n – 1 times, therefore saving (32 × n – 1) – 32 cycles of repetition.
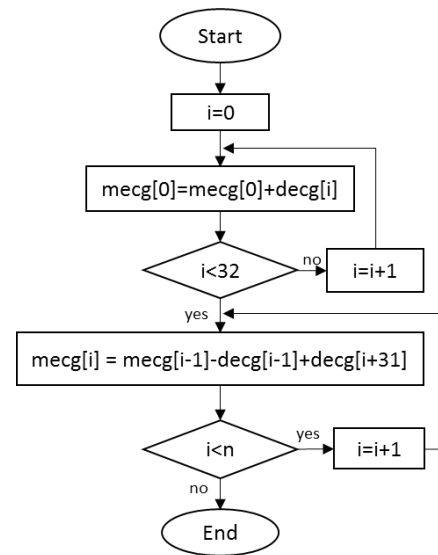

Figure 10 Process flowchart of moving window integrator algorithm with computation speed improvement

4.2.5 R peak detector

In R peak detection stage, a thresholding algorithm is introduced to the output of the moving window integrator. A flag will be introduced when the output of the moving window integrator passes the threshold and a peak is detected. The threshold peak detected will be compared with the next eight peaks and the highest peak value will be the R peak.

Figure 11 shows the flowchart of the new algorithm of the R peak detector. The *rri* is the array for the R

peaks data, *current* and *previous* are the values detected by the flag that has passed the threshold, f_s is the sampling frequency, which is 200 Hz, and *Temp* is the temporary data.
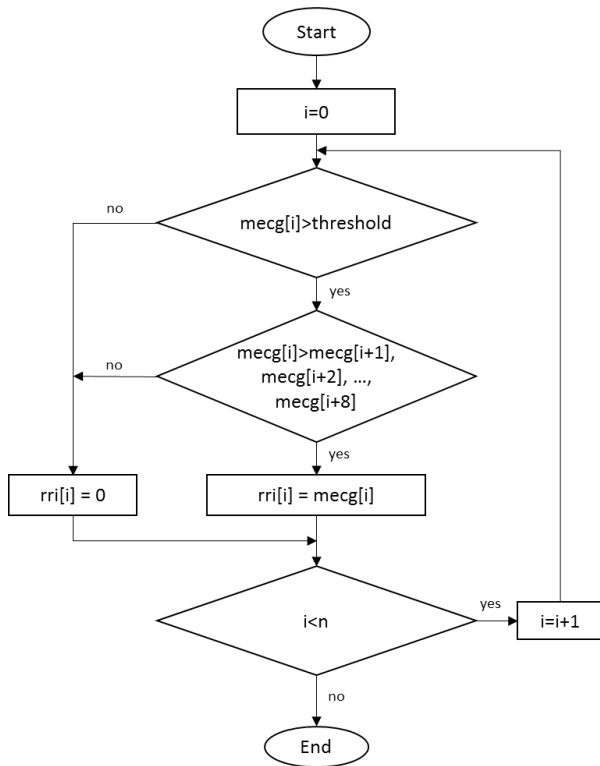

Figure 11 New R peak detection algorithm

4.3 Arrhythmia Classification

Figure 12 shows the flow chart of arrhythmia classification algorithm. The arrhythmia classification algorithm is referred from [15] with some modifications. The first classifier block which classifies the normal beat is moved to the last classifier block. This classification is based on the interval between the R-R peaks. A self-designed sliding window which consists of three R-R intervals is done and the middle R-R interval is targeted each time to be classified by comparing and calculating the intervals. This classification only selectively classifies PVCs, VF, and second-degree AV block.

4.4 On-board Touch Screen Menu

As shown in Figure 13, the on-board touch screen menu for SoC-based arrhythmia detector consists of five main menus which are *Welcome* menu, *Patient Retrieval* menu, *Patient Information* menu, *Computation* menu and *Result* menu. The GUI development of each menu utilizes the multi-touch controller, Liquid Crystal Display (LCD) controller and Secure Digital (SD) controller with their associated device driver. The design of each menu is provided in following sub subsections. Figure 14 shows the top-

level system functional flow chart of complete SoC-based arrhythmia detector.
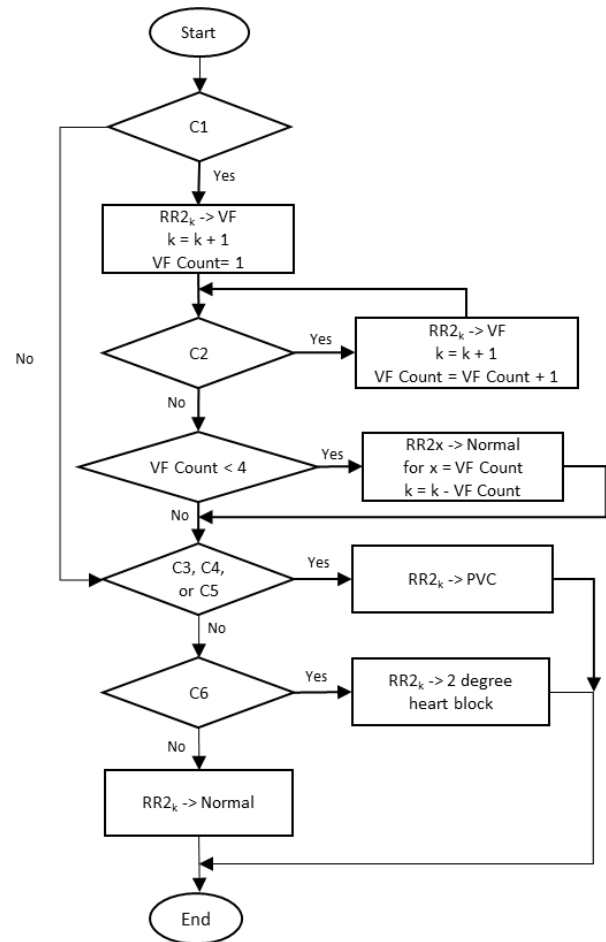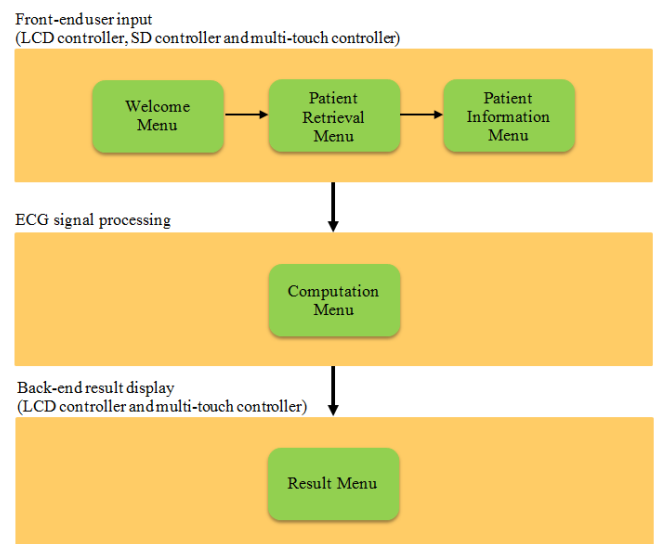

Figure 12 Arrhythmia classifier algorithm

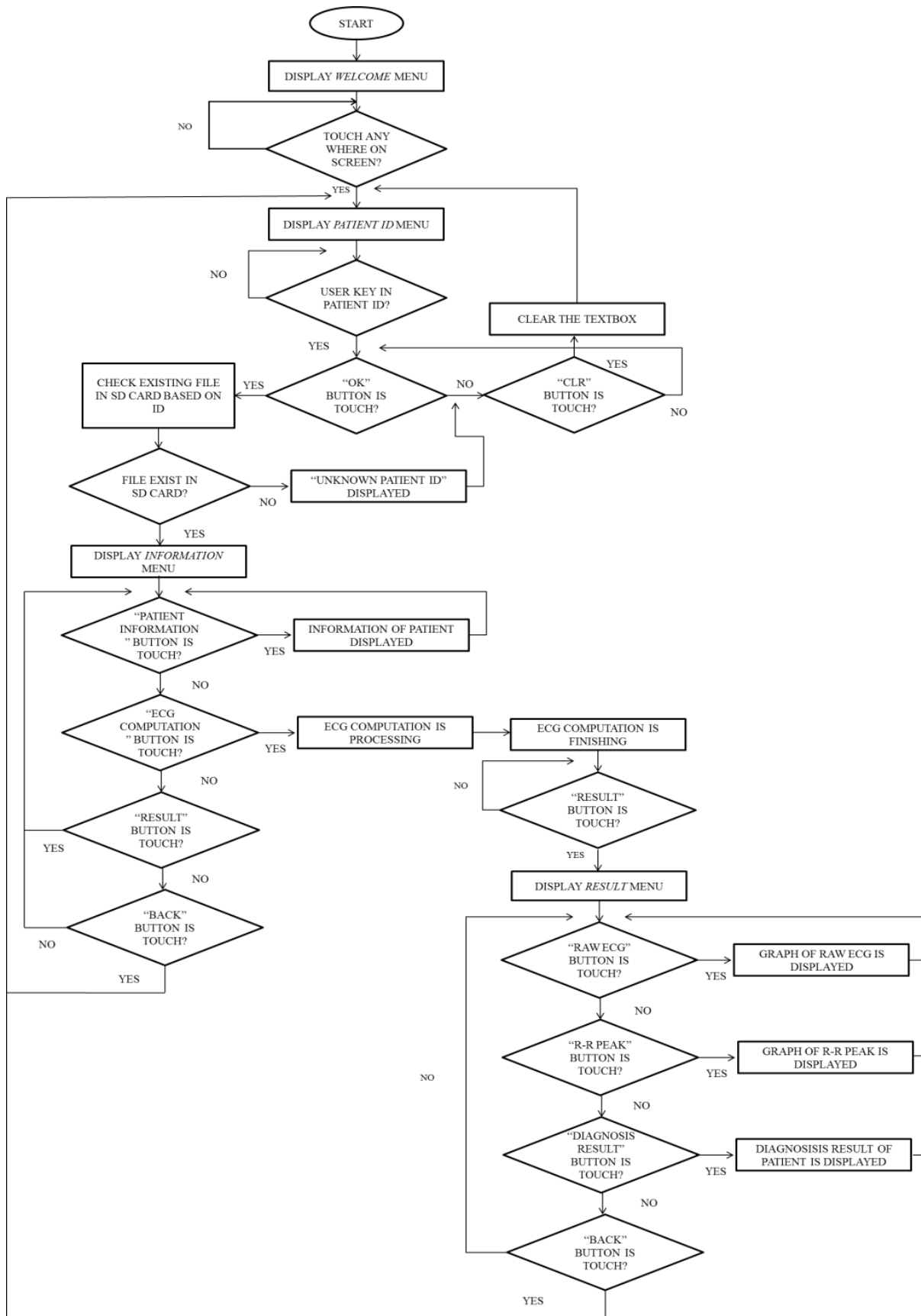**Figure 13** On-board touch screen GUI development

Figure 14 Top-level system functional flow chart

4.4.1 Welcome Menu

The *Welcome* menu is the first screen display when the system is started or reset. The design of *Welcome* menu is shown in Figure 15. The design is loaded onto the DE2-115 FPGA board after compilation in Quartus II.

In order to display any application on LCD touch screen, a handler has to be declared to handle the display task. In this case, the handler object is *pic_viewer* from *picture_viewer_control struct*. For displaying an item on screen in dedicated location, a command function of *<display_handler> ->display* has to be executed. In this case, it will be *pic_viewer->display*.
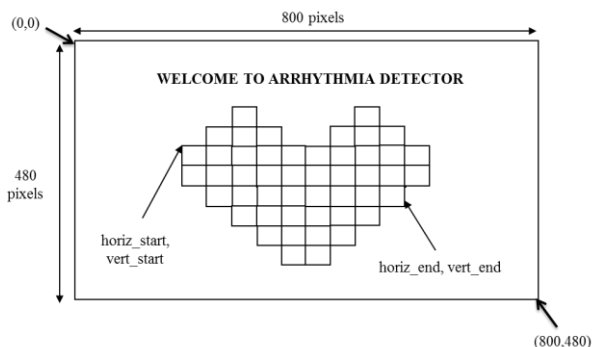
Figure 15 Design of *Welcome* menu

4.4.2 Patient Retrieval Menu

The *Patient Retrieval* menu is used to retrieve patient files stored in the SD card (as shown in Figure 16) based on a unique identification (ID). The design of *Patient Retrieval* menu is shown in Figure17. This menu consists of a ten-numbers keypad for the user to key in the patient ID. The number that is keyed in by the user will be shown on the screen (grey box). Besides, there is a "*CLR*" button for the user to reset the number as well as an "*OK*" button for number confirmation. The ID verification is done based on existing patient files stores on the SD card.
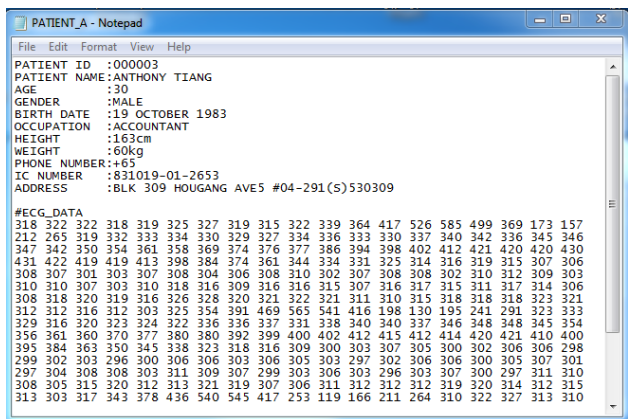

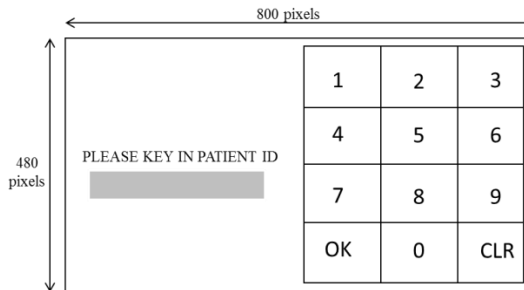**Figure 16** Examples of text file stored SD card

Figure 17 Design of *Patient Retrieval* menu

4.4.3 Patient Information Menu

The *Patient Information* menu displays the patient personal information from the retrieved patient file. The design of *Patient Information* menu is shown in Figure 18. There are four buttons on the top of this menu. The first button is the "*Patient Information*" button which enable user to view the detailed information of patient. Next is the "*ECG Computation*" button which displays the Computation menu. The "*Result*" button will only be enabled after the ECG computation is completed for the user to view the results of the analysis. Last is the "*Back*" button which is used to redirect user to the *Patient Retrieval* menu.
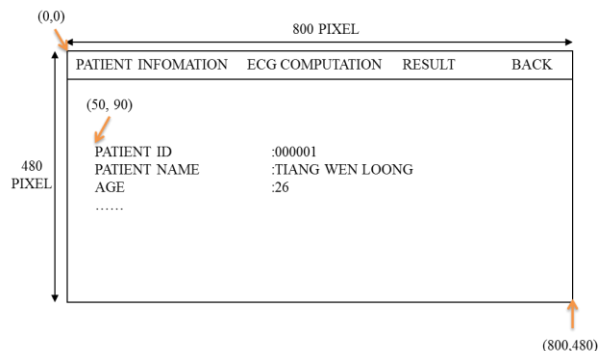

Figure 18 Design of *Patient Information* menu

4.4.4 Computation Menu

The *Computation* menu is used to display the computation status during the ECG processing, feature execution and arrhythmia classification processes. The design of *Computation* menu is shown in Figure 19.

4.4.5 Result Menu

There are three buttons on the top of Result menu which are "*Raw ECG*", "*R-R Peak*" and "*Diagnosis Result*" that is used to display the graphs of raw ECG and R peak detection as well as arrhythmia classification result as shown in Figure 20, Figure 21 and Figure 22, respectively. Besides, a "*Back*" button

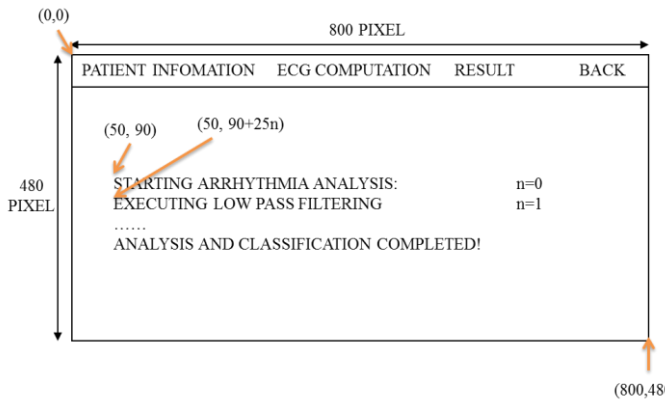is also provided to redirect user to the *Patient Retrieval* menu.

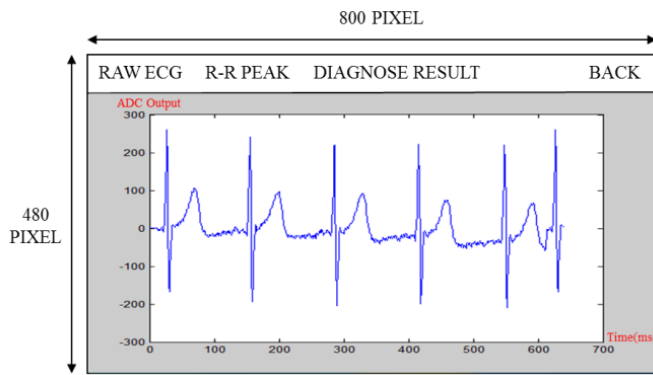**Figure 19** Design of *Computation* menu

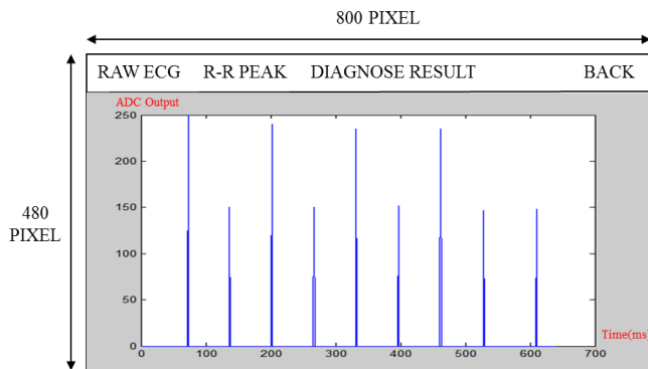**Figure 20** Design of *Result* menu to display raw ECG graph

Figure 21 Design of *Result* menu to display R-R interval graph

5.0 RESULTS AND DISCUSSION

The summary of timing analysis is shown in Table 1. The moving window integrator algorithm helps to save about $(32 \times n - 1) - 32$ cycles of addition which is 2.261 seconds of processing time for this block. The improved algorithm starts by adding the 32 arrays of data from squaring function for the first time and store into the moving window integrator array, then deduct the first squaring function array data from the

result, and add the 33rd data from the squaring array to the result.

Figure 23 shows the graph output after squaring with noise reduction, whereas Figure 24 shows the comparison between the R peak detector output with the reference moving window integrator output.
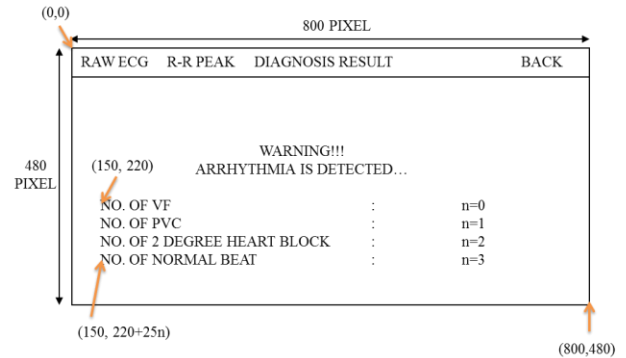

Figure 22 Design of *Result* menu to display diagnosis results

Table 1 Summary of timing analysis

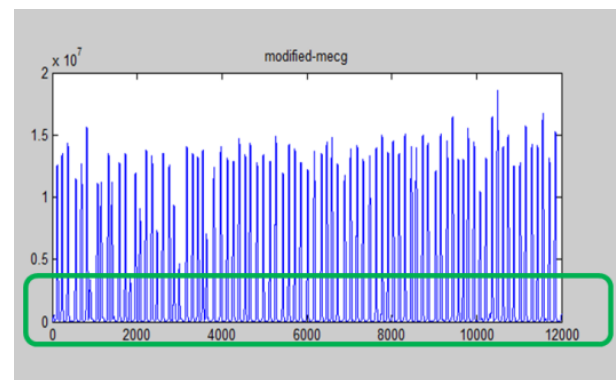| Process	Time Taken (s)
Reading Data	3.833
Band-Pass Filtering	1.116
Differentiation	0.601
Squaring	0.181
Moving Window Integration	0.222
R Peak Detection	0.025
Arrhythmia Classification	0.407
Total	**6.385**

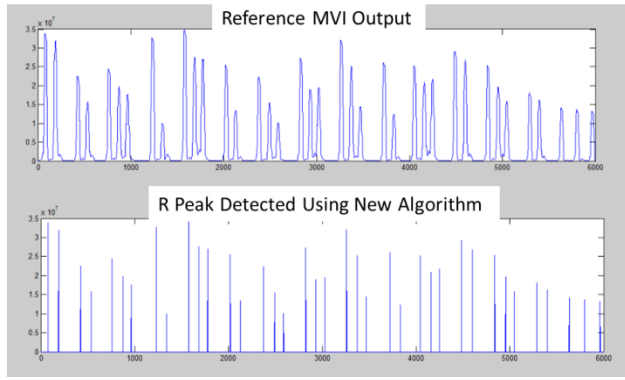**Figure 23** Squaring with noise reduction

Figure 24 Comparison between R peak detection algorithms with referenced MVI output

The developed arrhythmia detector was evaluated and benchmarked with ECG data from MIT-BIH arrhythmia database [26, 27] for functionality and performance verification. The analysis is done by using data size of 12000. There are ten samples of data taken for measuring the normal beat and PVCs classification accuracy, while one sample of data each for measuring the VF and second-degree AV block classification accuracy. The accuracy of classification is calculated by comparing the number of detected beat as arrhythmia with the MIT-BIH database results/annotations. The overall detection accuracy is shown in Table 2. The accuracy depends on the consistency of the ECG data. The higher the noise of the ECG data the lower the accuracy of the detection result.

Table 2 Overall arrhythmia classification accuracy

Classification	Total Sample	Detection Accuracy (%)
Normal beat	10	93.61 ± 5.64
PVCs	10	88.56 ± 9.04
VF	1	96.30
Second-degree AV Block	1	85.71

For system integration, the ECG pre-processor, feature extractor, and arrhythmia classifier were combined with the GUI driver and loaded into the Altera VEEK-MT board. Some modifications for coding were done in order to suit the compiler limitations. The performance of the on-board touch screen GUI for SoC-based arrhythmia detector after system integration is provided in the following subsections.

5.1 *Welcome* Menu

After the system is started or reset, the first *Welcome* menu will be shown on LCD touch screen as shown in Figure 25.
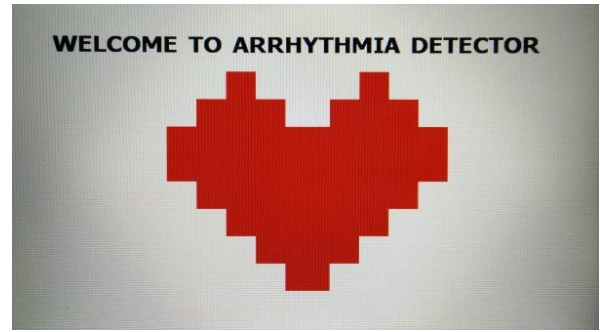

Figure 25 *Welcome* menu

5.2 *Patient Retrieval* Menu

By touching any part of the *Welcome* menu, the *Patient Retrieval* menu will be displayed as shown in Figure 26. If the patient ID keyed in does not match with any existing file stored in the patient database on the SD card, an error message box with "UNKNOWN PATIENT ID" will be displayed as shown in Figure 27.
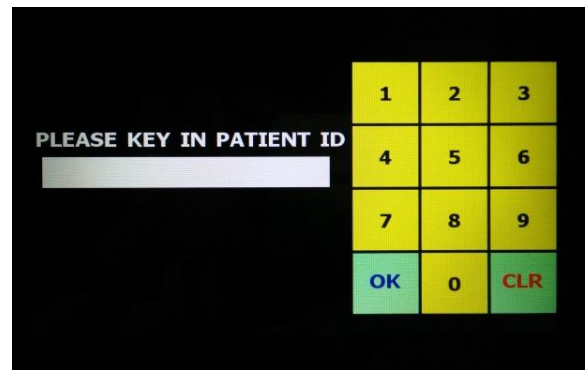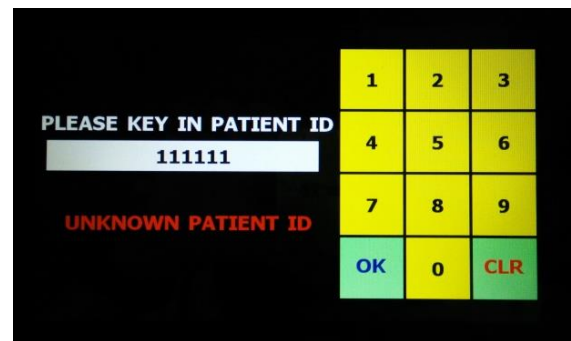

Figure 26 *Patient Retrieval* menu

Figure 27 Error message box with "UNKNOWN PATIENT ID"

5.3 *Patient Information* Menu

If a correct patient ID is keyed in, the *Patient Information* menu will be shown on the LCD touch screen as shown in Figure 28.
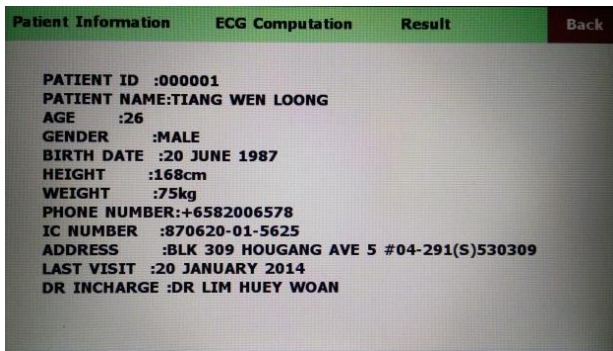
Figure 28 *Patient Information* menu

5.4 Computation Menu

After clicking the "*ECG Computation*" button, the patient offline ECG dataset from SD card is read and sent to the ECG processing module for signal pre-processing, feature extraction and classification. The intermediate computation processing status is displayed on LCD touch screen as shown in Figure 29.
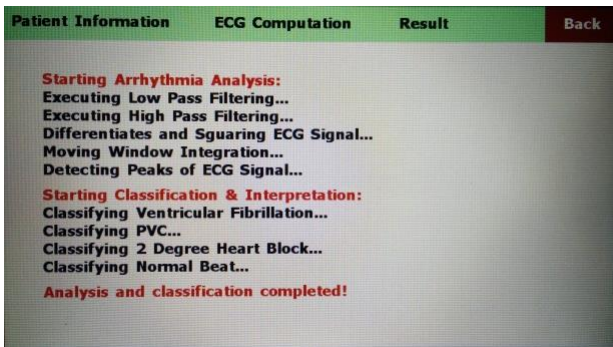

Figure 29 *Computation* menu

5.5 Result Menu

After completing the computation process, the user is able to check the raw ECG data and R peak detection graphs as well as the arrhythmia detection and classification results in the Result menu as shown in Figure 30, Figure 31 and Figure 32, respectively.
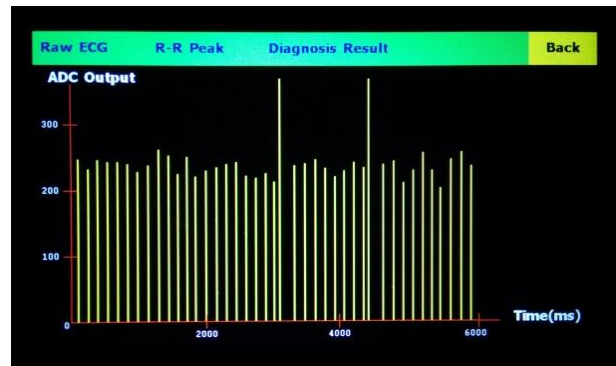

Figure 30 Graph of raw ECG data

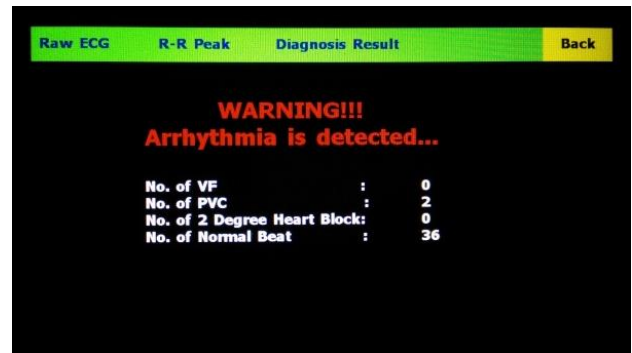**Figure 31** Graph of R peak detection

Figure 32 Arrhythmia detection and classification result

The limitation of this system is that it can only process 6000 ECG dataset which is 30 seconds data due to memory limitation. Moreover, only 640 out of 6000 ECG dataset can be used to plot the raw ECG and R peak detection graphs due to its resolution (480×800). In addition, the current system can only process one patient data. Besides, management of offline ECG dataset is not structured and organized as the system could only process one ECG computation attached to each patient.

6.0 CONCLUSION

The proposed SoC-based arrhythmia detector has a convincing performance on the processing speed, noise reduction, and R peak detection accuracy as well as some additional features which are added such as the arrhythmia classifier and interactive touch screen GUI. For further improvement, a higher accuracy and extended arrhythmia classification algorithm should be designed for detection of more types of arrhythmia. Besides, improvement on the FPGA platform should also be done by increasing the memory or improving the memory utilization algorithm so that more ECG dataset can be loaded and processed in the system.

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