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NANO-MOSFETs IMPLEMENTATION OF DIFFERENT LOGIC FAMILIES OF TWO INPUTS NAND GATE TRANSISTOR LEVEL CIRCUITS: A SIMULATION STUDY

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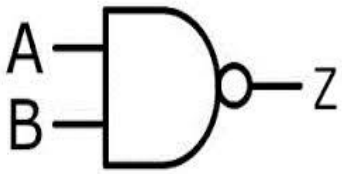
Graphical abstract



Abstract

In this paper, simulation study has been carried out on two inputs logic NAND transistor circuits with four different logic families, namely (i) nano-CMOS NAND gate, (ii) nano-MOSFET loaded n-type nano-MOSFET NAND gate, (iii) resistive loaded nano-MOSFET NAND gate, and (iv) pseudo nano-MOSFET NAND gate. The simulation tool used is WinSpice. All the n-type and p-type nano-MOSFETs have channel length (L) 10 nm with width (W) 125 nm or 250 nm, depending on type of logic families. The problem with downscaling of nano-MOSFET is the implementation of low power high speed nano-MOSFET transistor circuit. Simulated timing diagrams for input and output waveforms showed correct logical NAND gate operations for all four logic families. Transient analysis on nano-MOSFET loaded n-type nano-MOSFET NAND gate shows that theoretical modeling calculation of rise time (tr), fall time (tf) and maximum operating frequency (fmax) are reasonably matched simulated output result of WinSpice. All the logic family circuits studied shown reduction in dynamic power when MOSFET is downscaled to nanometer regime.

Keywords: Logic family, nano-MOSFET, NAND gate, simulation, theory

Abstrak

Penyelidikan simulasi terhadap logic NAND dua talian masukan dengan empat kumpulan logik yang berlainan telah dilaksanakan, iaitu (i) get NAND nano-CMOS, (ii) bebanan nano-MOSFET jenis n get NAND nano-MOSFET, (iii) rintangan get NAND nano-MOSFET, dan (iv) pseudo get NAND nano-MOSFET. Perisian yang digunakan ialah WinSpice. Kesemua nano-MOSFET jenis n dan jenis p yang digunakan mempunyai panjang terusan (L) 10 nm dengan lebar (W) 125 nm atau 250 nm bergantung kepada jenis kumpulan logik. Masalah pengurangan saiz nano-MOSFET ialah pelaksanaan kuasa rendah dan masa kendalian singkat bagi litar-litar transistor nano-MOSFET. Rajah masa untuk denyutan gelombang masukan dan keluaran menunjukkan kendalian logik NAND yang betul untuk kesemua kumpulan logik. Analisis terhadap bebanan nano-MOSFET jenis n get NAND menunjukkan masa bangkit, masa jatuh dan kalaan operasi maksima adalah lebih kurang sama dari segi teori dan simulasi. Kesemua kumpulan logic memaparkan pengurangan kuasa dinamik bila saiz MOSFET dikurangkan kelinkungan nanometer.

Kata kunci: Kumpulan logik, nano-MOSFET, get NAND, simulasi, teori

1.0 INTRODUCTION

Downscaling of MOSFET structural dimensions from micrometer regime to nanometer regime have occurred over the last few decades [1-6]. The conventional bulk CMOS technology is rapidly continuously downscaling until approaching the scaling limits. The MOSFET channel length L is approaching 10 nm. In order to enable gate to control charge in the channel, the requirement T_{OX}<< L must be met, where T_{OX} is the oxide insulator thickness [7, 8]. In this study, the gate oxide thickness is approaching 1.5 nm, that is the oxide insulator is few atoms thick. Meanwhile, the nano-MOSFET width W used in this study is 125 nm or 250 nm depending on the type of logic families [9-11]. In this study, NAND logical functions are implemented using four different logic families, namely: (i) nano-CMOS NAND gate, (ii) nano-MOSFET loaded n-type nano-MOSFET NAND gate, (iii) resistive loaded (748.8 Ω) nano-MOSFET NAND gate, and (iv) pseudo nano-MOSFET NAND gate. Timing requirements for these NAND gates are analyzed using WinSpice [12-14]. WinSpice output show correct logical NAND operation. Transient analysis on timing requirements are carried out on nano-MOSFET loaded n-type nano-MOSFET NAND circuit to compare theoretical modeling calculation results and simulation output results [15, 16]. The low power high speed characteristic of NAND designed using 10 nm nano-MOSFET logic circuit are benchmarked with NAND designed using 45 nm MOSFET [1, 10]. The simulation result in this project showed these characteristics.

2.0 METHODOLOGY

Device simulation is carried out by using on-line simulator NanoMOS developed by Purdue University. Then, the CIR Spice code files for four different logic families 2 inputs NAND circuit are simulated using WinSpice. The input timing diagrams and output timing diagrams are the output result of WinSpice simulation. To test the 2 inputs NAND circuits logical operation, two input signals with period 20 ns and 30 ns are used. Meanwhile, to analyze transient response (rise time, fall time and maximum operating frequency), two input signals with 20 ps and 30 ps are used.

2.1 Theory

By using on-line device simulator NanoMOS, the nano-MOSFET device parameters (refer to Table 1) and current-voltage (I-V) graphs (refer to Figure 1 and Figure 2) are obtained, which are used to calculate the timing response for nano-MOSFET loaded nano-MOSFET NAND circuit (refer to Table 2).

Table 1 Structural Dimension of nano-MOSFET

Double Gate nano-MOSFET Device Simulation Parameters	
Vgs	0.60 V
Vds	0.60 V
V_{TO}	0.20 V
Source/Drain Doping Concentration (N_D)	$1x10^{20}$ cm^{-3}
Channel Body Acceptor Impurity Concentration (N_A)	$1x10^{16}$ cm^{-3}
Channel Width (W)	125 nm
Channel Length (L)	10 nm
Source Length/Drain Length (L_{SD})	7.5 nm
Silicon Channel Thickness (T_{Si})	1.5 nm
Top/Bottom Oxide Insulator Thickness (T_{OX})	1.5 nm
Top/Bottom Insulator Relative Dielectric Constant	3.9
Channel Body Relative Dielectric Constant	11.7
Top/Bottom Gate Contact Work Function	4.1888 eV

Table 2 Theoretical Modeling Calculation Values of nano MOSFET Loaded nano-MOSFET NAND Circuit

Double Gatenano-MOSFET Loaded NAND Gate	
Gate Capacitance (Cg)	$5.7551x10^{-17}$ F
Area Capacitance (Ca)	$1.6125x10^{-19}$ F
Sidewall Capacitance (Csw)	$6.072x10^{-17}$ F
Total Drain Capacitance (Cd)	$4.6041x10^{-18}$ F
Total Source Capacitance (Cs)	$1.0469x10^{-17}$ F
nano-MOSFET Loaded Resistance (Rload)	748.8 Ω
nano-MOSFET on-state Resistance (Ron)	36.2 Ω
Loaded NAND Gate Total Capacitance at Output Node (Ctotal)	$1.3351x10^{-16}$ F
Total Capacitance between Two nano-MOSFETs Connection (Csd)	$1.5073x10^{-17}$ F
Rise Time Constant (τr)	$9.99688x10^{-14}$ s
Rise Time (tr)	$1.34158x10^{-12}$ s
Fall Time Constant (τf)	$1.02114x10^{-14}$ s
Fall Time (tf)	$2.24652x10^{-14}$ s
Propagation Delay (tp)	$3.81856x10^{-14}$ s
Maximum Signal Frequency (fmax)	$7.33113x10^{11}$ Hz

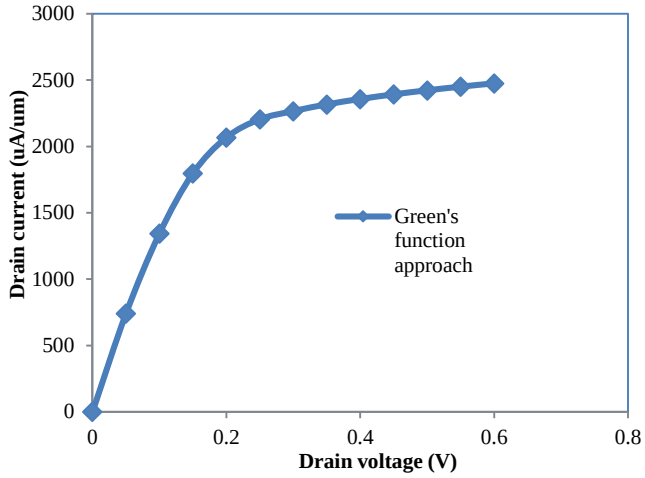


Figure 1 Drain Current- Drain Voltage Curve of nano-MOSFET

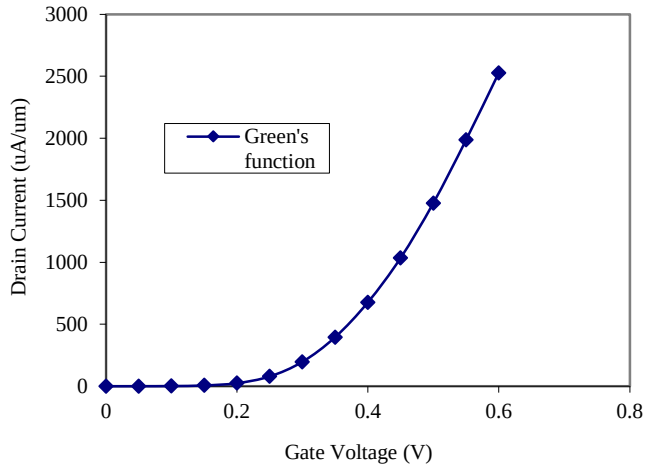


Figure 2 Drain Current- Gate Voltage Curve of nano-MOSFET

Equations and theories which are used to obtain data in Table 2 are listed below:

$$R_{Load} = \left(\frac{V_{DS}}{I_{DS}}\right) = \frac{V_{th}}{I_{on-state\ at\ linear\ region} \times W}$$

since digital logic gates operate at linear portion of I-V curve

$$R_{channel\ at\ on-state} = \frac{1}{\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{DD} - V_{th})}$$

μ_n =electron mobility at ballistic =1200 cm^2/Vs

C_{OX} = Oxide capacitance per unit area

Rise time constant (τr) = R_{Load} x NAND gate total capacitance

Rise time (tr) = 2.2 x τr x 6.1 , it takes 6.1 times duration to pass logic 1 than logic 0 through an n-channel MOS pass-transistor

Fall time constant (τf) = (Ctotal x 2 $R_{Channel\ on-state}$) + (Csd x $R_{Channel\ on-state}$), Elmore formula has been used since two nano-MOSFETs are connected in series

Fall time (tf) = 2.2 x τf

Propagation delay (tp) = 0.35(τr + τf)

Maximum signal frequency (fmax) = 1/(tr + tf)

The equation used to obtain dynamic power is:

$P(dyn) = a\ C\ f\ V_{DD}^2$

Where a is the activity coefficient, C is the capacitance at output node, f is the frequency of switching and V_{DD} is the voltage supply [17-19].

3.0 RESULTS AND DISCUSSION

Modern MOSFET devices operate between the drift-diffusion and ballistic regimes. So, quasi-ballistic transport is examined in this paper.

Figure 3, Figure 4, Figure 5 and Figure 6 show the schematic circuits of all four logic families NAND gate.

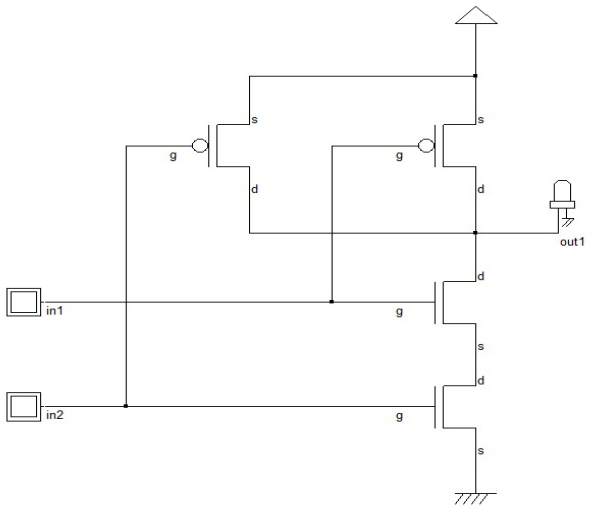


Figure 3 Two inputs nano-CMOS NAND circuit

Their timing diagrams are shown in Figure 7(a), 7(b) and 7(c), Figure 8(a), 8(b) and 8(c), Figure 9(a), 9(b) and 9(c), as well as Figure 10(a), 10(b) and 10(c), accordingly. The first input signal to all four logic families has a period of 20 ns (with 50% duty cycle).The second input signal to all four logic families has a period of 30 ns (with 50% duty cycle).

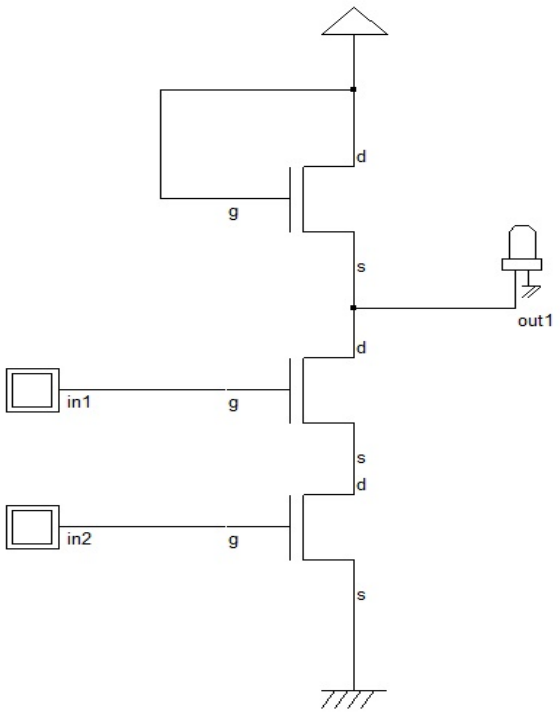


Figure 4 Two inputs nano-MOSFET loaded nano-MOSFET NAND circuit

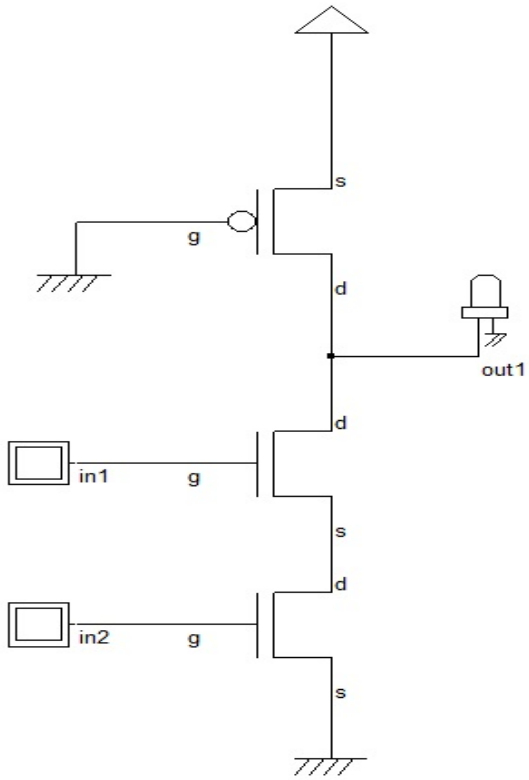


Figure 6 Two inputs pseudo nano-MOSFET NAND circuit

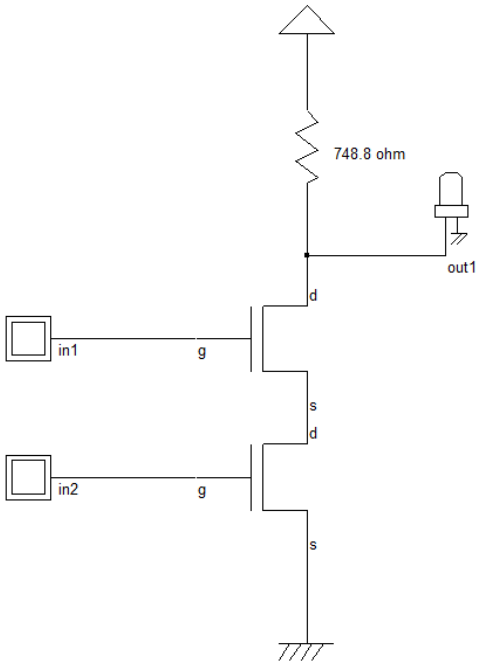


Figure 5 Two inputs resistive loaded nano-MOSFET NAND circuit

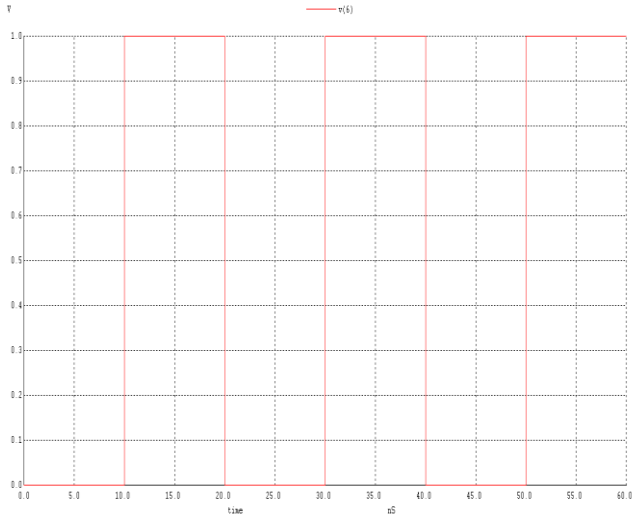


Figure 7(a) First input signal to nano-CMOS NAND circuit

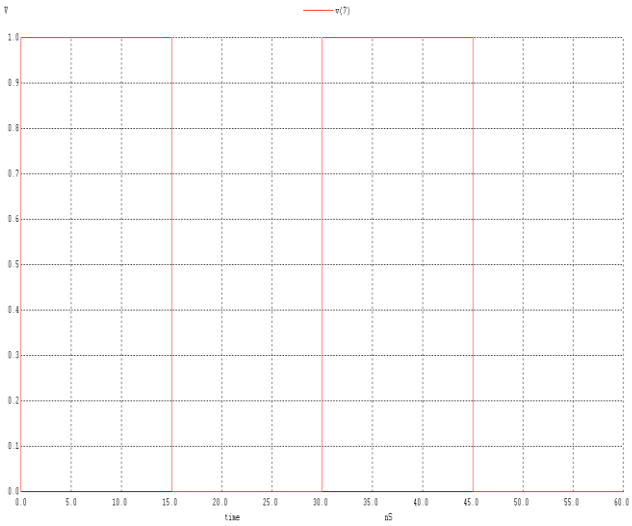


Figure 7(b) Second input signal to nano-CMOS NAND circuit

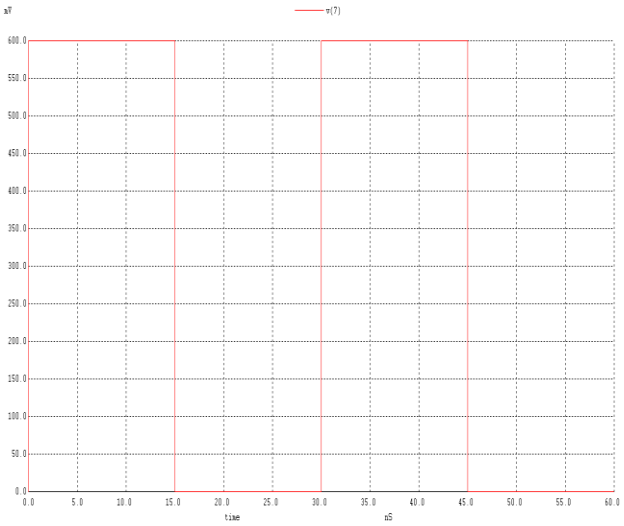


Figure 8(b) Second input to nano-MOSFET loaded nano-MOSFET NAND circuit

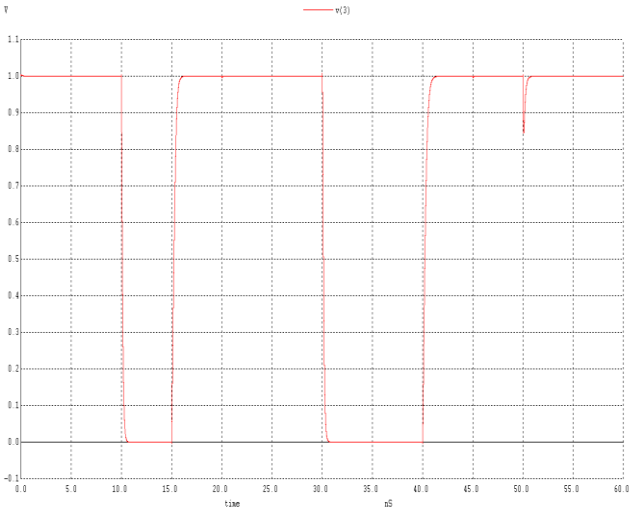


Figure 7(c) Output signal of nano-CMOS NAND circuit

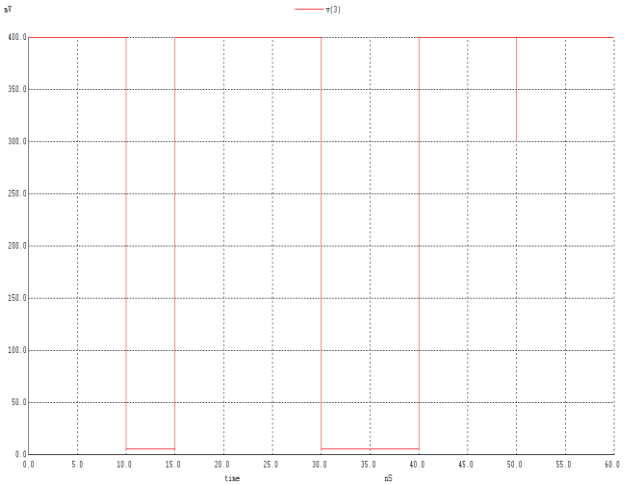


Figure 8(c) Output of nano-MOSFET loaded nano-MOSFET NAND circuit

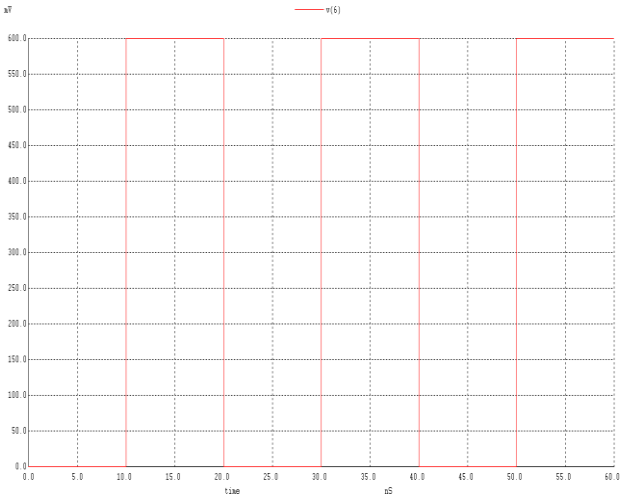


Figure 8(a) First input to nano-MOSFET loaded nano-MOSFET NAND circuit

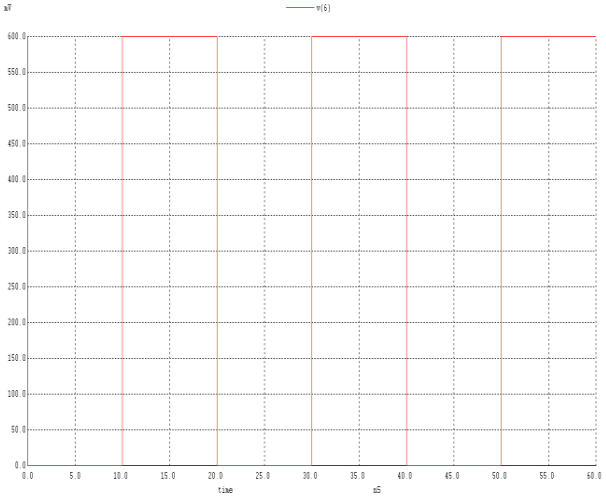


Figure 9(a) First input to resistive loaded nano-MOSFET NAND circuit

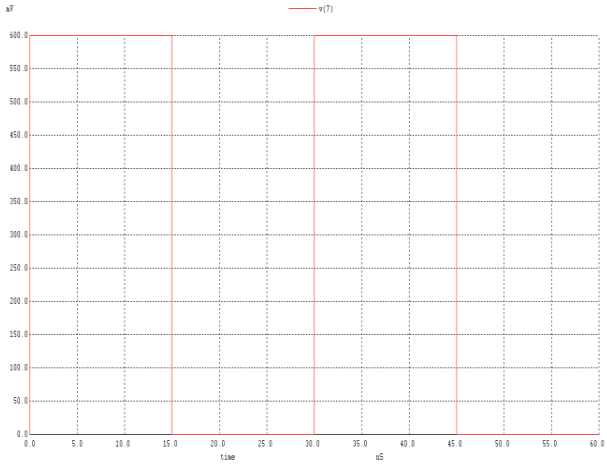


Figure 9(b) Second input to resistive loaded nano-MOSFET NAND circuit

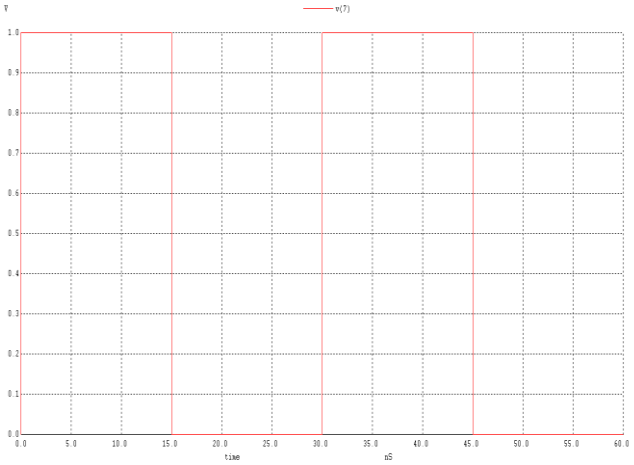


Figure 10(b) Second input to pseudo nano-MOSFET NAND circuit

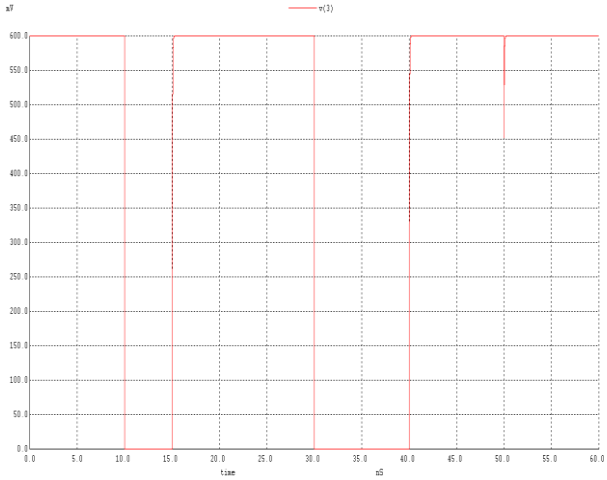


Figure 9(c) Output of resistive loaded nano-MOSFET NAND circuit

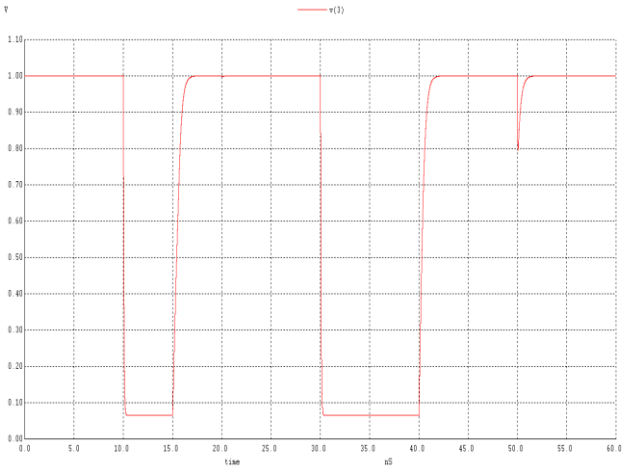


Figure 10(c) Output of pseudo nano-MOSFET NAND circuit

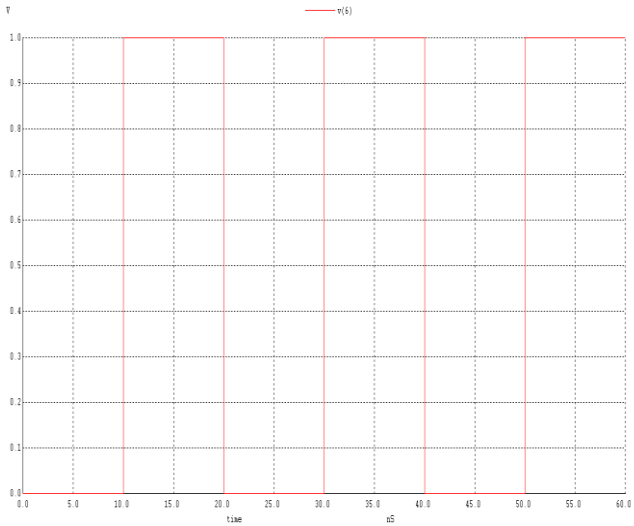


Figure 10(a) First input to pseudo nano-MOSFET NAND circuit

The above input and output signal timing diagrams show correct logical NAND operation for all four logic families. The output signal of nano-MOSFET loaded NAND circuit shows a threshold voltage loss of 0.2 V since the nano-MOSFET load acts as a pass transistor which passes a weak logic level 1 and passes a strong logic level 0. The threshold voltage loss 0.2 V corresponds to the threshold voltage of nano-MOSFET which is 0.2 V [20, 21]. The nano-MOSFET pass transistor load is equivalent to 748.8Ω load resistance. This 748.8 Ω resistance is calculated from the nano-MOSFET current-voltage (I-V) curve in the linear portion where digital operation occurred as shown in Figure 1. By this way, resistive loaded 748.8 Ω nano-MOSFET NAND circuit is formed as shown in Figure 5.

Figure 11(a), 11(b) and 11(c) show transient analysis timing diagrams for nano-MOSFET loaded NAND circuit.

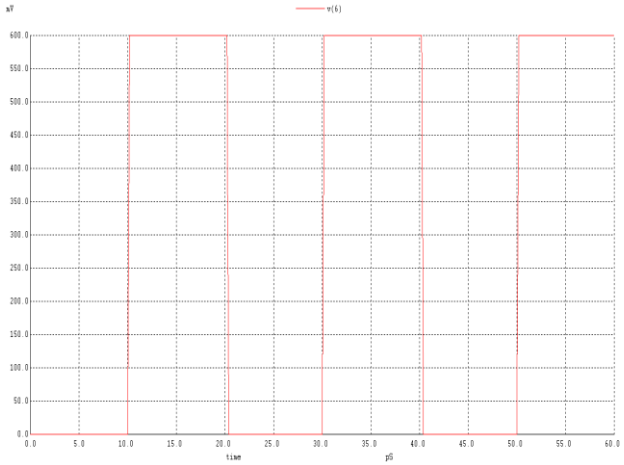


Figure 11(a) First input to nano-MOSFET loaded nano-MOSFET NAND circuit for transient analysis

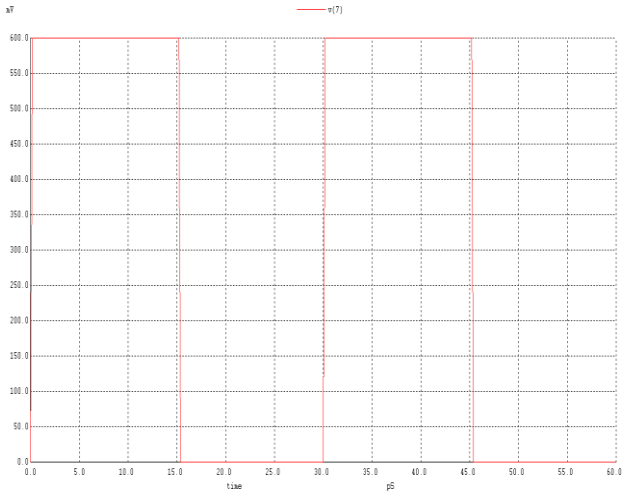


Figure 11(b) Second input to nano-MOSFET loaded nano-MOSFET NAND circuit for transient analysis

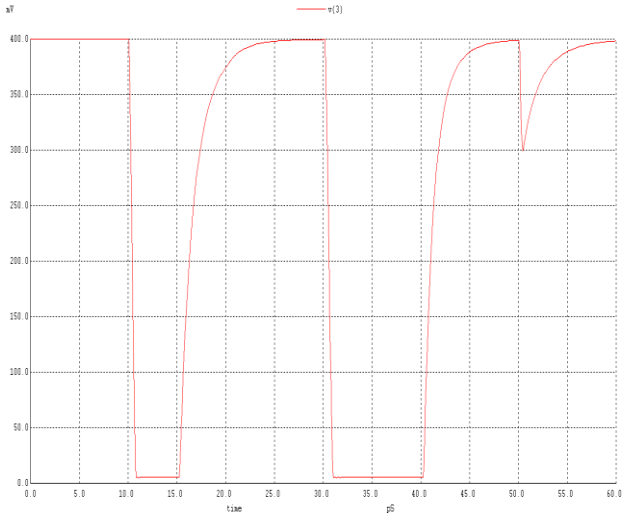


Figure 11(c) Output of nano-MOSFET loaded nano-MOSFET NAND circuit for transient analysis

The period of the 2 input signals to this NAND circuit is 20 ps and 30 ps. Rise time and fall time are taken between 10% and 90% of output voltage signal at rising edge and falling edge, respectively. Rise time is due to charging circuit whereas fall time is due to discharging circuit. Table 3(a) and 3(b) show the rise time, fall time and maximum operating frequency of this transient analysis by theoretical modeling calculations and from WinSpice simulation output. From [1], the DG MOSFET NOT propagation delay is 16 ps and from [10], the propagation delay for 45 nm MOSFET 2 input NAND is 8.719 ps. When compared with theoretical and simulated propagation delay, which are 3.818×10^{-14} s and 1.79×10^{-13} s, respectively, of 2 input NAND designed with 10 nm nano-MOSFET has a faster speed. Therefore, downscaling nano-MOSFET has lead to faster speed of logic circuits [9].

Table 3(a) Theoretical Calculation Value for NAND nano-transistor Loaded Circuit

Theoretical Modeling Calculations from NanoMOS Device Simulation Data (10% and 90% Points)				
Logic Gates	**Rise Time (tr)**	**Fall Time (tf)**	**Propagation Delay (tp)**	**Maximum Operating Frequency (fmax)**
NAND	1.341×10^{-12} s	2.246×10^{-14} s	3.818×10^{-14} s	7.331×10^{11} Hz

Table 3(b) WinSpice Simulation Value for NAND nano-transistor Loaded Circuit

WinSpice Simulation Results Using Model Level MOS6 (10% and 90% Points)				
Logic Gates	**Rise Time (tr)**	**Fall Time (tf)**	**Propagation Delay (tp)**	**Maximum Operating Frequency (fmax)**
NAND	2.727×10^{-12} s	68.18×10^{-14} s	1.79×10^{-13} s	2.933×10^{11} Hz

In nano-CMOS NAND circuit, n-type nano-MOSFET has W= 125 nm each and p-type nano-MOSFET has W= 250 nm each to counter-balance the difference in electron and hole mobility. In nano-MOSFET loaded NAND circuit, the n-type nano-MOSFET load has W= 125 nm and the bottom n-type nano-MOSFETs has W=250 nm each. This condition is need to meet

$$\left(\frac{W}{L}\right)_n \geq 2\left(\frac{W}{L}\right)_{Load}.$$

in order to reduce output low voltage V_{OL}. In pseudo nano-MOSFET NAND circuit, p-type nano-MOSFET has W= 125 nm and n-type nano-MOSFET has W= 250 nm. This condition is needed to meet the same criteria in above expression in order to reduce V_{OL}. Meanwhile,

in resistive loaded 748.8 Ω nano-MOSFET NAND circuit, 748.8 Ω resistance is the load and n-type nano-MOSFET has W= 250 nm [22].. In nano-MOSFET loaded NAND circuit, V_{OL} is theoretically calculated using

$$V_{OL}=\frac{2\times R_{on}}{(2\times R_{on})+R_{load}}\times V_{DD}$$

This theoretical value is 52.90 mV. When compared with WinSpice simulated value 9 mV, the ratio is 5.87. From theoretical modeling and also WinSpice simulation, output high voltage V_{OH} is 0.4 V. When at least one out of two nano-MOSFETs at the bottom of the circuit is at off state, and thereby at high impedance state, threshold voltage loss 0.2 V occurs at the top side nano-MOSFET load. Therefore, V_{OH} is 0.4 V.

To investigate the dynamic power during downscaling of nano-MOSFET, refer to Table 4.

Table 4 Dynamic Power for Four Different NAND Logic

	nano-CMOS NAND	nano-MOSFET loaded NAND	Pseudo nano-MOSFET NAND	Resistive loaded NAND
Dynamic Power (Watts)	1.29×10^{-10}	4.50×10^{-10}	8.63×10^{-11}	1.55×10^{-11}
Voltage Supply (Volts)	1	0.6	1	0.6
Frequency of switching (Hertz)	5×10^{7}	5×10^{7}	5×10^{7}	5×10^{7}

The equation used to obtain dynamic power is:

$$P(dyn) = a\ C\ f\ V_{DD}^2$$

Where a is the activity coefficient, C is the capacitance at output node, f is the frequency of switching and V_{DD} is the voltage supply. For two input NAND logic a=0.1875. Normally, in conventional bulk micrometer MOSFET logic, dynamic power is about μW. So, from Table 4, reduction in dynamic power is observed during down scaling. From [1], the power dissipation of DG MOSFET NOT is 10 μW and from [10], the power dissipation of 2 inputs NAND with 45 nm nano-MOSFET is 18.32 nW. When compared with power in Table 4, it is obvious that downscaling of nano-MOSFET has lead to reduction of dynamic power of NAND circuit implemented using 10 nm nano-MOSFET. Therefore, low power logic circuits are achieved when designed using 10 nm nano-MOSFET [2, 16].

4.0 CONCLUSION

Logical two inputs NAND circuit operation can be implemented by using nano-MOSFETs with four different logic families. Conventional bulk MOSFETs can be replaced by nano-MOSFETs to implement NAND transistor level circuits. In this paper, this development in semiconductor industry has been shown by simulation study using WinSpice and observing input timing diagrams and output timing diagrams. Correct logical NAND operations are observed from these simulation output. During downscaling of MOSFET to nanometer regime, dynamic power of logic NAND circuit is reduced. Low power high speed 2 input NAND logic has been achieved in this simuation project.

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